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LSK389

APPLICATION NOTE

DUAL MONOLITHIC JFET FOR ULTRA-LOW NOISE APPLICATIONS

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Features

- Low Wideband Noise
- Low *1/f* Noise
- High Transconductance
- Well-Matched Threshold Voltages
- High *gm*/Capacitance Ratio
- Industry's First 100% Noise-Tested JFET

Applications

- Low Noise Amplifiers
- Differential Amplifiers
- High Input Impedance Amplifiers
- Phono and Other Audio Preamps
- Condenser Microphone Preamps
- Electrometers
- Piezoelectric Sensor Preamps
- Front-end for Low-Noise Op Amps

Introduction

The LSK389 is the industry's lowest noise Dual N-Channel JFET, 100% tested, guaranteed to meet 1/*f* and broadband noise specifications, while eliminating burst (RTN or popcorn) noise entirely. The product displays high transconductance and very good matching. It is the JFET of choice for low noise applications, especially those requiring a differential amplifier input stage.

LSK389 Key Specifications

- 1.3 nV/√Hz input noise at 1 kHz, I_D = 2 mA
- 1.5 nV/√Hz at 10 Hz, I_D = 2 mA
- 14 mS transconductance at I_D = 2 mA
- Improved DC offset ±15 mV max.
- C_{ISS} = 25 pF typ.
- C_{RSS} = 5.5 pF typ.
- Breakdown voltage = 40 V min.
- 4 grades of I_{DSS} available (A, B, C, D)

N-Channel JFET Basics

The simplified equation below describes the DC operation of a JFET [1]. The term V_t is the threshold voltage. The term β is the transconductance coefficient of the JFET (not to be confused with BJT current gain). The terms V_t and β are key SPICE parameters that define basic JFET DC operation. The simple relationship below is valid for $V_{ds} > V_t$ and does not take into account the influence of V_{ds} that is responsible for output resistance of the device. The equation is valid only for positive values of $V_{gs} - V_t$.

$$I_d = \beta(V_{gs} - V_t)^2$$

At V_{gs} = 0, we have I_{DSS}, which is the maximum current that will flow when the device is in its saturation region, where V_{ds} is much larger than V_t:

$$I_{DSS} = \beta(V_t)^2$$

β can be seen from I_{DSS} and V_t to be:

$\beta = I_{DSS} / (V_t)^2$

The operating transconductance *gm* is easily seen to be:

$gm = 2 * \sqrt{\beta * I_d}$

This last relationship is important, because transconductance of the JFET is what is most often of importance to circuit operation [2]. For a given transconductance parameter β, *gm* is largely independent of I_{DSS} and V_t, and goes up as the square root of drain current. This is in contrast to a bipolar transistor where *gm* is proportional to collector current. The value of β for JFETs ranges from about 1e-3 to 100e-3.

These simplified equations do not take into account the effect that the parameter lambda has on output conductance G_{os} of the JFET. In other words, in the saturation region, the drain current does increase slightly as V_{ds} increases. G_{os} for the LSK389 is about 40 µS when I_d = 2 mA and V_{ds} = 10 V. This corresponds to about 25 kΩ. The equations also do not account for ohmic source resistance, which can reduce transconductance a bit, since it acts like source degeneration.

A typical LSK389 low noise JFET showed a measured I_{DSS} of 13.8 mA and transconductance of 14.6 mS at an operating current of 2 mA. Gate voltage at that operating point was –0.50 V. With a 1-kΩ load, the un-degenerated common-source LSK389 provides gain of 14.6. With a 10-kΩ load, the gain is 108, which is quite high for a single common source JFET amplifier stage. This amount of gain in an LSK389 first-stage can help make the most of the inherently low input-referred noise of the LSK389 in a multi-stage preamplifier. This stage has a 3-dB bandwidth of 700 kHz when driving a 10-pF load, for a gain-bandwidth product of 76 MHz.

JFET Noise

JFET noise results primarily from *thermal channel noise* [1, 3 - 6]. That noise is modeled as an equivalent input resistor r_n whose resistance is equal to approximately 0.6/*gm* [7]. If we model the effect of *gm* as *rs'* (analogous to *re'* for a BJT), we have r_n = 0.6*rs'*. This is remarkably similar to the equivalent voltage noise source for a BJT, which is the voltage noise of a resistor whose value is 0.5*re'*. The voltage noise of a BJT goes down as the square root of I_c because *gm* is proportional to I_c, and *re'* goes down linearly with I_c as well. However, the *gm* of a JFET increases only as the square root of I_d. As a result, JFET input voltage noise goes down as the one-fourth power of I_d. The factor 0.6/*gm* in modeling the equivalent input noise resistance is approximate, and SPICE modeling of some JFETs suggests that the number is closer to 0.67. That is the number that will be used here.

At I_d = 2.0 mA, *gm* for the measured LSK389 dual monolithic JFET described above is 14.6 mS, corresponding to a resistance *rs'* of 68.5 Ω. Multiplying by the factor 0.67, we have an equivalent noise resistance r_n of 45.9 Ω. Recognizing that a 1 kΩ resistor has thermal noise voltage of 4.2 nV/√Hz, and that thermal noise goes as the square root of resistance ratio, the 45.9 Ω resistance represents theoretical input-referred noise for the LSK389 of 0.9 nV/√Hz. JFET input voltage noise will also include a thermal noise contribution from ohmic gate and source resistances, but this is fairly small.

The noise measurement circuit shown in Figure 1 was implemented to measure the noise of the LSK389 at 2.0 mA. It comprises two stages of amplification implemented with the two JFETs in the LSK389. Total gain of the amplifier is 880. With the input of the amplifier shorted, the output was connected to an A-weighted noise measurement meter with an equivalent noise bandwidth (ENBW) of 13.5 kHz. The use of A weighting minimizes contributions from hum and provides a well-defined ENBW. Measured noise at the output of the amplifier was 120 µV. Dividing by the gain of 880, we have 136 nV. Dividing by the number of root Hz in an ENBW of 13.5 kHz (116/√Hz), we have 1.17 nV/√Hz. This was achieved with a completely un-shielded circuit using no extraordinary measures. Given other circuit and environmental noise contributors, it is likely that the LSK389 was performing at about 1 nV/√Hz.

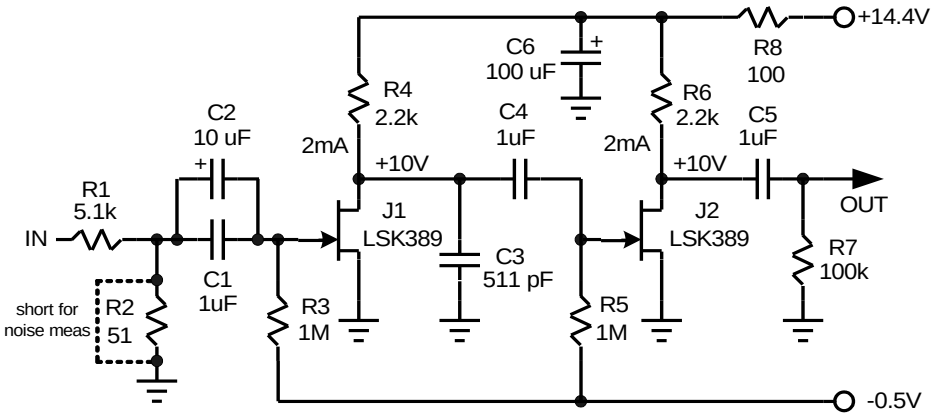

Figure 1: JFET noise measurement circuit

The theoretical thermal channel noise for a JFET operating at *gm* = 14.6 mS is 0.9 nV/√Hz, as can be calculated in the discussion below. However, a JFET also has ohmic resistances in the source, drain and gate, which can contribute thermal noise. By partial example, the source-drain resistance of the LSK389 measured above is 36 Ω when there is no bias. Under operating conditions, and depending on device geometry and doping profiles, a portion of this resistance remains as effective ohmic source resistance that can add thermal noise. Ohmic source resistance of only 10 Ω would contribute 0.4 nV/√Hz.

JFET input voltage noise is a function of drain current because it is a function of transconductance. It decreases as drain current increases, in accordance with the discussion below. Table 1 shows the gain and input noise of the noise measurement preamplifier as a function of the drain current of each JFET in the LSK389. The applied gate voltage for each condition is also listed for reference.

Table 1

I_d, mA	V_{gs}, V	Gain	Gain/stage	noise, nV/√Hz
0.5	0.62	200	14	1.72
1.0	0.57	450	21	1.44
2.0	0.50	880	30	1.17
4.0	0.39	1400	37	1.11
8.0	0.22	1980	45	1.07

It can be seen that the noise goes down at increased drain current, but not quite as fast as thermal channel noise theory below would predict. This is likely due to the contribution of thermal noise from ohmic gate and source resistances. The presence of source resistance can also be seen by the fact that when I_d is doubled, gain does not go up fully by √2. It is also notable that the LSK389 was running a little bit hot when drain current for each device was 8 mA and V_{ds} was 10 V, for total dissipation of 160 mW. Higher operating temperature increases noise and decreases transconductance. Operating the device at V_{ds} = 5 V will halve dissipation and reduce noise somewhat.

Although noise decreases with increased bias current, Table 1 shows that there is a point of diminishing returns. For example, two LSK389 devices in parallel, each operating at 4 mA, will deliver a 3-dB noise reduction compared to one device, reducing noise to about 0.8 nV/√Hz, superior to a single device operating at 8 mA, which will have noise on the order of 1.07 nV/√Hz.

JFET Noise Sources

In order to understand low-noise JFETs, it is helpful to briefly review the 5 major sources of noise in JFETs [1, 3, 4, 7].

1. Thermal channel noise
2. Gate current shot noise
3. *1/f* noise
4. Generation-recombination noise
5. Impact ionization noise

The first two sources of noise are largely fundamental to the device, while the remaining three sources are largely the result of device imperfections. Examples of such imperfections include lattice damage and charge traps.

Thermal Channel Noise

Thermal channel noise, as discussed above, is akin to the Johnson noise of the resistance of the channel [2]. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the

point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, and can vary with the individual device geometry [3]. It is often a bit smaller than 0.67.

Gate Shot Noise Current

JFET input current noise results from the shot noise associated with the gate junction leakage current. Shot noise increases as the square root of DC current passing through a semiconductor junction. A useful relationship is that I_{shot} = 0.57 pA/√Hz/√μA [7]. Alternately, I_{shot} = 0.57 fA/√Hz/√pA. Gate shot noise is white, and usually has no *1/f* component [8].

I_{shot} = 0.57 fA/√Hz/√pA

This noise is normally very small, on the order of fA/√Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Consider a circuit with a 100-MΩ resistive source impedance and a JFET with input noise current of 4 fA/√Hz at 25°C. Thermal noise of the 100-MΩ resistor will be 1330 nV/√Hz. The voltage noise resulting from the shot noise flowing in the source resistance will be 400 nV/√Hz. Leakage current doubles every 10°C, so at 65°C the leakage current goes up by a factor of 16 and the noise contributor will go up by a factor of 4 to about 1600 nV/√Hz. The two contributors are now comparable. Always bear in mind that the junction temperature will be higher than the ambient temperature, depending on device dissipation. For even higher source resistances in the GΩ range, the shot noise contributor could be comparable to, or greater than, the thermal noise contributor, even at room temperature.

Finally, consider a purely capacitive source of 50 pF, as from a condenser microphone, where there is theoretically no thermal noise contributor from the signal source (ignore biasing arrangements for the moment). At 32 Hz, the source impedance is 100 MΩ reactive and the shot noise contribution is still 400 nV/√Hz, far exceeding the voltage noise contribution of the JFET.

1/f Noise

At very low frequencies the input noise power of a JFET amplifier rises as the inverse of frequency. That is why this noise is referred to as *1/f* noise. When expressed as noise voltage, this means that the noise rises at a rate of 3 dB/octave as frequency decreases. In a good JFET, the *1/f* spot noise voltage at 10 Hz may be twice the spot noise at 1 kHz (up 6 dB) when expressed as nV/√Hz. The noise might typically be up by 3 dB at 40 Hz. *1/f* noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice [4]. Improved processing contributes to reduced *1/f* noise. In fact, the amount of *1/f* noise is sometimes considered as an indication of process quality.

By comparison, a good JFET IC op amp with input noise of 10 nV/√Hz at 1 kHz may have its noise up by 3 dB at 100 Hz and the spot noise at 10 Hz might be up by 10 dB to 32 nV/√Hz. At 1Hz that op amp may have spot noise on the order of 65 nV/√Hz.

Figure 2 is a plot of voltage noise versus frequency for a hypothetical JFET (not an LSK389). The *1/f* corner frequency is defined as the frequency where the *1/f* noise contribution equals the flat band noise. Put another way, it is where the –3 dB/octave *1/f* noise line intersects the flat band noise line. At this frequency, the voltage noise will be up by 3 dB.

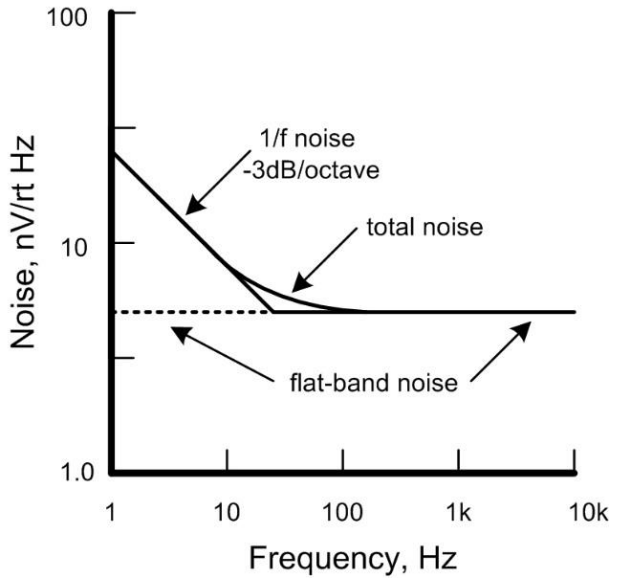

Figure 2: *1/f* noise voltage of a hypothetical JFET

Generation-recombination Noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as *G-R* noise [4]. This *excess noise* is discussed in the LSK489 application note [7]. Thanks to Linear Systems' advanced processing this source of noise is very low in the LSK389.

Impact Ionization Noise

An electron traveling in a strong electric field can be accelerated to the point where it has enough kinetic energy to knock another electron out of its valence band into the conduction band if it impacts an atom in the crystal lattice [4, 6, 8]. For convenience, the electron corresponding to normal current flow can be called a "seed" electron, since it starts the process. This collision creates a new hole-electron pair. This process is called impact ionization. The new hole and electron then act as additional charge carriers and add to the current flow. The new carriers may also be accelerated to the point where they themselves create an impact ionization event, so the process may be multiplied. This is what is called an avalanche effect. Impact ionization often occurs in a p-n junction that is under a high reverse bias voltage that creates a large electric field. Impact ionization noise is discussed in more detail in the LSK489 application note [7].

Single-ended Amplifier with JFETs in Parallel

Figure 3(a) shows a simple single-ended JFET amplifier stage. In a practical implementation, the –0.29-V bias voltage must be controlled by some form of feedback to maintain the desired operating point of 2.0 mA. It is well known that operating two JFETs in parallel will reduce input-referred noise by 3 dB. This, of course, requires that the JFETs be matched, as in the case of both JFETs in an LSK389 dual monolithic matched pair. This is straightforward in a single-ended amplifier application, as in (b). In (c), a parallel-connected JFET pair is combined with an op amp and negative feedback to implement an amplifier with a gain of 1000.

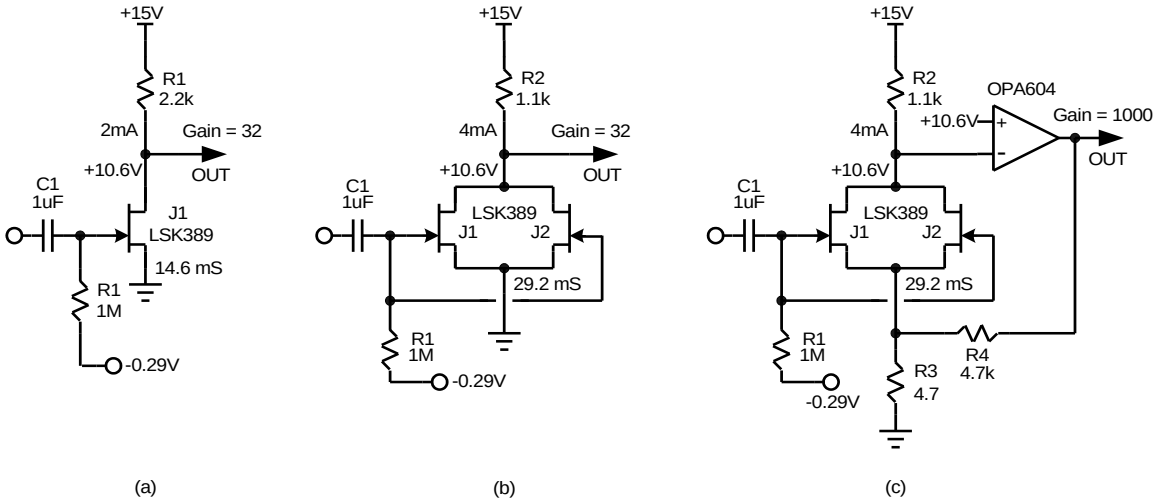

Figure 3: Single-ended JFET amplifier stages

Conversely, when an LSK389 is used as a differential pair, both JFETs are effectively in series as far as the signal is concerned (halving net transconductance), and input-referred noise increases by 3 dB over that of a single JFET in a single-ended arrangement, a significant noise disadvantage of the differential pair.

Given the use of an LSK389 in both cases, the single-ended amplifier using both devices in parallel is thus a full 6 dB quieter than the differential amplifier. This is a steep price to pay for differential operation. In both cases, the total current consumption is the same.

Simple Differential Pair Amplifier

Figure 4(a) shows a simple differential amplifier stage implemented with an LSK389. This non-feedback circuit provides a very high impedance differential input and a differential output. Its gain will, however, vary somewhat depending on the transconductance of the individual JFET.

Fortunately, transconductance of a given JFET type is much less variable than parameters like I_{DSS} and threshold voltage. Recall that

$$gm = 2 * \sqrt{\beta * I_d}$$

where the parameter β is similar for JFETs from the same process. Stabilizing the gain by the introduction of source degeneration resistors will seriously compromise the noise performance as a result of the thermal noise contributions from the source resistors.

If each JFET is operating at 2 mA, *gm* will be about 14 mS for each device. Differential gain will then be 2 * 14 mS * 2.2 k Ω = 61.6. Actual gain will be a bit lower due to the output conductance G_{os} of the JFETs. Input noise of the stage will be about 3 dB higher than that of each JFET, which will come to about 1.5 nV/√Hz. Noise contributions from the current source will be largely canceled by the differential nature of the circuit, but use of a low-noise current source is nevertheless recommended. Similarly, use of a current source with very high output impedance, such as one that is cascoded, is recommended in order to preserve good common mode rejection.

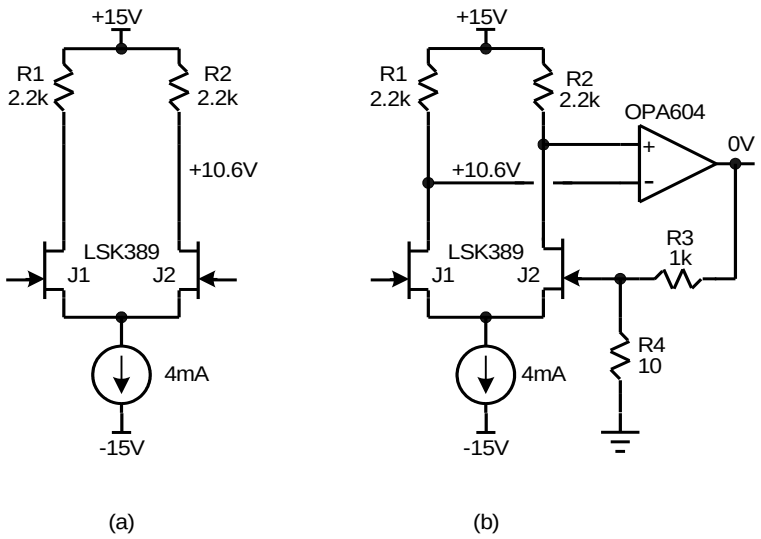

Figure 4: Simple LSK389 differential amplifiers

In Figure 4(b) the LSK389 is used as the input stage for a closed-loop feedback amplifier with a gain of 100. Most of the open loop gain for the amplifier is provided by the operational amplifier, which can be one of many different types, such as the OPA604. The main advantage of this arrangement is that the JFET input stage provides a low-noise front-end with extremely high input impedance. It provides enough initial gain to minimize noise contributions from the thermal noise of the load resistors and the input voltage noise of the following op amp stage.

The combination of the gain provided by the input stage and the op amp increases the loop gain and the unity gain frequency of the feedback amplifier. This means that caution must be exercised in choosing the closed loop gain to be large enough to keep the unity loop gain frequency from becoming so large as to introduce instability.

Cascoding and Driven Cascodes

Figure 5 (a), (b) and (c) show a differential pair that is cascoded 3 different ways. In (a), a conventional BJT cascode stage increases output impedance and eliminates Miller effect due to gate-drain capacitance in the JFETs. The cascode also allows the LSK389 to be used in circuits with higher voltages.

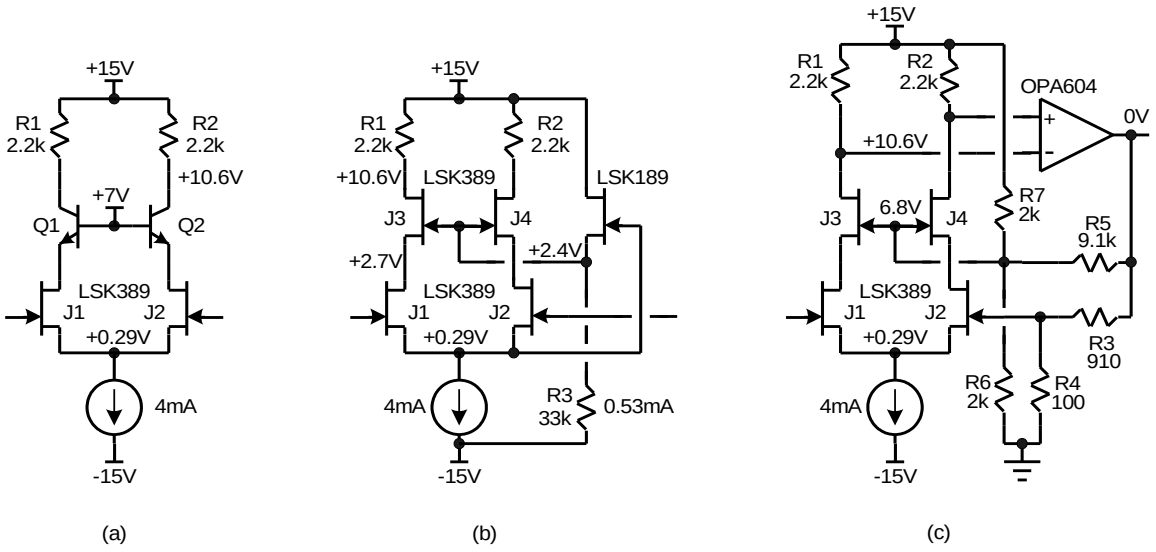

Figure 5: Cascoded differential amplifiers

Figure 5 (b) illustrates a bootstrapped cascode wherein the common mode signal present at the sources is fed to the gates of the JFET cascode transistors. This causes the drains of the JFETs to move with signal in the same way as the sources. This arrangement greatly reduces common mode distortion and also strongly suppresses the effect of drain-gate capacitance on the effective input capacitance of the stage. This can be important in some applications because of the moderate amount of drain-gate capacitance of the LSK389. An LSK189 JFET connected as a source follower is used in Figure 5 (b) to achieve the needed level shift of the voltage at the sources of J1 and J2. If greater V_{ds} for the differential pair is needed for more optimum operation, a Zener-based level shift arrangement, possibly using a P-channel LSK289, can be used. Bootstrapping is a form of positive feedback, so caution is advised at high frequencies. Such arrangements should always be simulated so that HF anomalies can be discovered and mitigated.

A third approach can be used in feedback amplifiers, as shown in Figure 5 (c). Here a replica of the feedback signal is used to drive the gates of the cascode transistors. I refer to this as a driven cascode [2]. The same cautions regarding bootstrapping mentioned above apply here as well.

Ultra-Low Noise Differential Amplifier Using Paralleled LSK389 JFETs

The ultra-low noise input amplifier is shown in Figure 6. It is a JFET-input, double folded cascode design without negative feedback [9]. Its gain is approximately 40 dB. Without negative feedback, there is no need for a feedback network with very low impedance (on the order of ohms) to keep the noise down. Such a feedback network can be difficult to drive. Moreover, without negative feedback, the input is naturally fully differential. The input JFET pair actually consists of four paralleled LSK389 JFET differential pairs, each pair with its own tail current source. This enables input-referred noise of 0.7 nV/√Hz to be achieved in a differential amplifier.

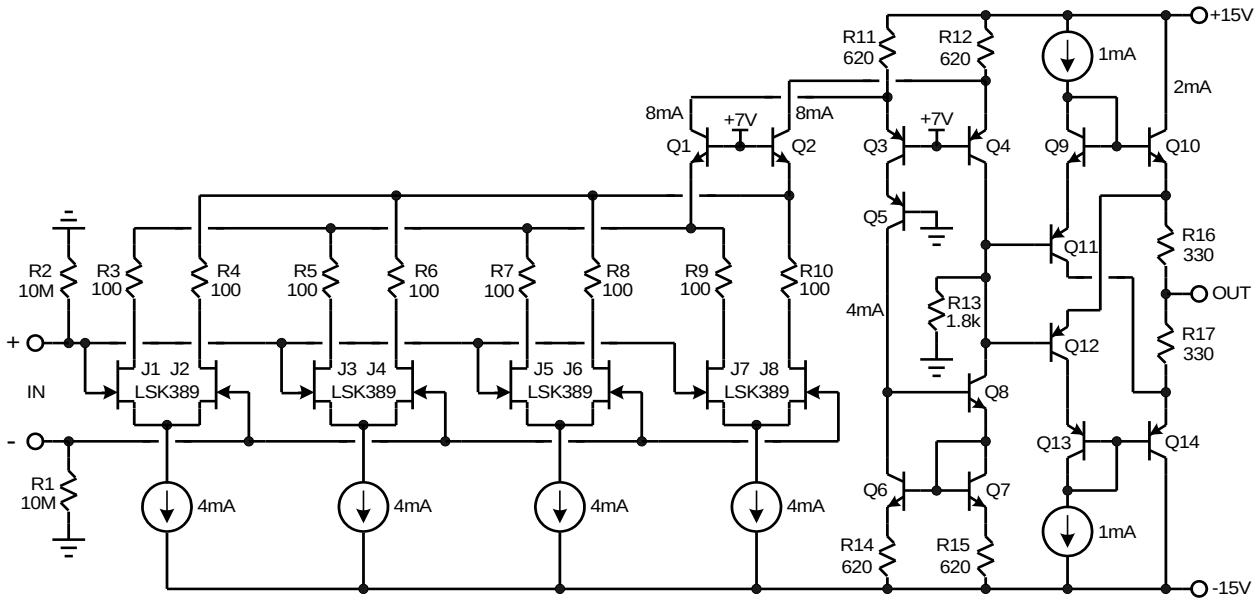

Figure 6: Ultra-Low noise differential amplifier

Paralleling of transistors is a well-known technique for reducing input voltage noise. Each time the number of transistors is doubled, a 3-dB improvement of S/N results. In the case here, 4 differential pairs are paralleled for a net improvement of 6 dB over a single differential pair. Simple paralleling of JFETs can lead to high-frequency instability and sub-optimal biasing due to differences in threshold voltage and I_{DSS} from pair to pair. If gate stopper resistors are used to mitigate the instability, noise is compromised. The key to paralleling JFET differential pairs is to literally parallel four pairs, each with its own tail current source. This decouples the sources among the pairs and allows each to find its own operating point. The decoupling of the sources also mitigates interaction among the pairs that can lead to instability. This, together with measures taken in the drain circuits, eliminates the need for gate stopper resistors.

This technique makes use of the fact that JFETs from the same process tend to have roughly the same transconductance if operated at the same current, even if the I_{DSS} and threshold voltages are not tightly matched. This means that each of the 4 pairs will contribute about the same amount of transconductance without close matching of the pairs.

The drains of the differential pairs are parallel-connected to the emitters of an NPN differential cascode stage. The low input impedance of the cascode helps reduce interactions among the parallel-connected drains that can lead to HF instability. Drain interactions are reduced by 100-Ω drain stopper resistors, which have no effect on noise.

A fifth degenerated differential pair using an LSK489 (not shown) can be used to inject a DC servo offset correction current at the emitters of Q1 and Q2 [9]. This approach provides a convenient and non-invasive way of injecting the correction current and adds negligible noise. Introducing the correction differentially ahead of the folded cascode results in less second harmonic distortion from JFET offset currents.

Gain is set to about 100 by the transconductance of the input pairs and shunt load resistor R13. Since the circuit operates without negative feedback, in some applications the gain may need to be trimmed. There may also be a modest temperature dependence of gain. The temperature dependence can be reduced if tail current sources with a positive temperature coefficient are employed. Doing so will tend to cancel the negative temperature coefficient of transconductance. Bandwidth of the amplifier is about 10 MHz. At an input level of 5 mV RMS, THD is only 0.005%, with no significant harmonics above the third. This level is about 20 dB higher than the nominal level of 500 µV produced by a moving coil cartridge.

Source Follower with JFET Current Source

A handy source follower buffer is shown in Figure 7. It consists of a source follower whose pull-down current of about 1.3 mA is generated by a JFET current source, where R3 sets the current. Notice that R3 has V_{gs} of J2 across it at J2's operating current. If J1 and J2 are matched and have the same V_{gs} at the same operating current, voltage-dropping resistor R2 will drop the V_{gs} of J1 if it is the same value as R3, and the overall buffer will have close to zero input-output DC offset. This is a perfect application for the LSK389.

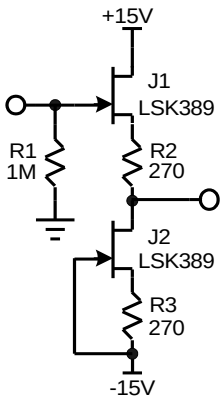

Figure 7: A source follower buffer with small DC offset

Substrate Bias Considerations

Figure 8 shows the connection arrangement inside the LSK389 dual monolithic JFET pair. Note that both transistors in the pair share a common substrate, and that substrate diodes exist between the gates and the substrate. The anodes of these substrate diodes are connected to the gates and the cathodes are connected to the substrate. These diodes are reverse biased under normal operating conditions. The substrate is brought out to pins 3 and 7 in the 8-pin SOIC package. The substrate is connected to the can in the metal TO-71 6L package.

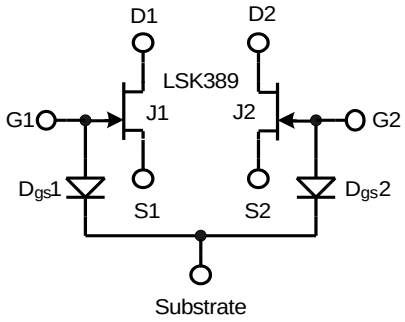

Figure 8: LSK389 including substrate diodes

The substrate diodes from the gates to the common substrate must sometimes be considered, but in most cases, the substrate is left floating. These diodes have a breakdown voltage in excess of 40 V. The leakage current of the substrate diodes, although quite small, can affect the net gate leakage current.

I_{DSS} Grades

The LSK389 is available in four I_{DSS} grades, A to D, with the following I_{DSS} ranges:

- LSK389A: 2.6 – 6.5 mA
- LSK389B: 6 – 12 mA
- LSK389C: 10 – 20 mA
- LSK389D: 17 – 30 mA

Conclusion

The LSK389 enables ultra-low noise amplifiers with very high input impedance and virtually no input bias current. Moreover, fully differential inputs with very high impedance can be implemented, which can be very important for low noise applications.

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