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LS844

APPLICATION NOTE

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N-Channel Dual JFETs Make High-Performance Complementary Input Stages Possible

Introduction

For circuits designed to work with high impedance sources, ranging from electrometers to microphone preamplifiers, the use of a low-noise, high-impedance device between the input and the op amp is needed in order to optimize performance.

At first glance, one of Linear Systems' most popular parts, the LSK389 ultra-low-noise dual JFET would appear to be a good choice for such an application. The part's high input impedance (1 TΩ) and low noise (1 nV/√Hz at 1kHz and 2mA drain current) enables power transfer while adding almost no noise to the signal. But further examination of the LSK389's specification shows an input capacitance of over 20pF. This will cause intermodulation distortion as the circuit's input signal increases in frequency if the source impedance is high. This is because the JFET junction capacitances are nonlinear. This will be especially the case where common source amplifier arrangements allow the Miller effect to multiply the effective value of the gate-drain capacitance. Further, the LSK389's input impedance will fall to a lower value as the frequency increases relative to a part with lower input capacitance.

A better design choice is Linear Systems' LS844. Though the LS844 has slightly higher noise (2.5 nV/√Hz vs. 1.0 nV/√Hz) its much lower input capacitance of only 4pF means that it will maintain its high input impedance as the frequency of the input signal rises. More importantly, using the lower-capacitance LS844 will create a circuit that is much less susceptible to intermodulation distortion than one using the LSK389.

The LS844's lower gate-to-drain capacitance enables more effective, elegant audio circuit designs. The relatively high capacitance of the LSK389 often requires designers to use a cascode circuit to provide the ability

to handle higher bandwidths without intermodulation distortion. The cascode does this by eliminating the Miller effect that can multiply the effective gate-drain capacitance and its associated nonlinear effects. However, the cascode adds complexity and noise contributed by the cascode transistors.

The LS844 is an N-channel dual low-noise, low-capacitance, tightly matched monolithic field effect transistor. It features:

- 3ms transconductance at 2mA drain current
- 1000 GΩ input impedance
- 60V breakdown voltage
- gate-drain capacitance of only 1.5pF
- 4pF input capacitance
- 2.5 nV/√Hz noise at 1kHz

- best low-noise/low-capacitance combination in the industry
- lowest input capacitance per unit gate length in the industry
- lowest noise for a given gate length in the industry
- tight V_{gs} matching at operating bias

The LS844 is particularly well suited to low-noise, high-gain audio and instrumentation circuits operating from battery voltages up to 60 volts. 48V phantom-powered circuits, like those used in microphone preamplifiers, are especially benefited by the features of the LS844. Low operating V_{gs}, high *gm*, tight matching, low noise and low capacitance make it well-suited to numerous audio and instrumentation applications.

Sensors, which play such an important role in today's world, benefit greatly from the performance delivered by the LS844. Such sensor technologies include piezo, quartz, condenser, electret, and MEMs devices. These devices benefit from the LS844's combination of low input capacitance and low noise. Electrometer applications also benefit from these characteristics.

JFET operation

The simplified equation below describes the DC operation of a JFET. The term β is the transconductance coefficient of the JFET.

$I_d = \beta(V_{gs} - V_T)^2$

At $V_{gs} = 0$, we have I_{dss}:

$I_{dss} = \beta(V_T)^2$

β can be seen from I_{dss} and V_T to be:

$\beta = I_{dss} /(V_T)^2$

The operating transconductance *gm* is easily seen to be:

$$gm = 2 * \sqrt{\beta} * I_d$$

This last relationship is important, because transconductance of the JFET is what is most often of importance to circuit operation. For a given transconductance parameter β, *gm* is largely independent of I_{dss} and V_T, and goes up as the square root of drain current. This is in contrast to a bipolar transistor where *gm* is proportional to collector current. The value of Beta for the LS844 is about 1.2e-3.

JFET amplifier noise

JFET noise results primarily from *thermal channel noise*. That noise is modeled as the Johnson noise of an equivalent input resistor r_n whose resistance is equal to approximately 0.67/*gm*. If we model the effect of *gm* as *rs'* (analogous to *re'* for a BJT), we have $r_n = 0.67rs'$. Johnson noise is proportional to the square root of resistance, and is about 4 nV/√Hz at a resistance of 1k. A JFET with gm = 3mS will have *rs'* = 333Ω and r_n = 200Ω. Theoretical noise will thus be about √ (200/1000) * 4 nV/√Hz = 1.8 nV/√Hz.

The noise relation for a JFET is remarkably similar to the shot noise source for a BJT, which is the voltage noise of a resistor whose value is *re'*/2. The voltage noise of a BJT goes down as the square root of increased I_c because *gm* is proportional to I_c and *re'* goes down linearly as well. However, the *gm* of a JFET increases only as the square root of I_d. As a result, JFET input voltage noise goes down as the ¼ power of I_d.

The LS844 noise advantage

In order to understand the LS844's noise advantage it is helpful to briefly review the 4 major sources of noise in JFETs.

- Thermal channel noise
- Gate current shot noise
- 1/f noise
- Generation-recombination noise

The first two sources of noise are largely fundamental to the device, while the second two sources are largely the result of device imperfections. Examples of such imperfections include lattice damage and charge traps. A major reduction in G-R noise is key to the LS844's superior noise performance.

Thermal channel noise

Thermal channel noise, as discussed above, is akin to the Johnson noise of the resistance of the channel. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, can vary with the individual device geometry, and is often a bit smaller than 0.67. However, it is unusual for the constant to be less than 0.5.

Gate shot noise current

JFET input current noise results from the shot noise associated with the gate input junction leakage current. This noise is normally very small, on the order of fA per √Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Shot noise increases as the square root of DC current. A useful relationship is that I_{shot} = 0.57pA/√Hz/√μA [1]. Alternately, I_{shot} = 0.57fA/√Hz/√pA.

Consider a circuit with a 100MΩ source impedance and a JFET at 25°C with input noise current of 4 fA/√Hz. The resulting voltage noise will be 400 nV/√Hz. Leakage current doubles every 10°C, so at 65°C this noise contributor will be about 1600 nV/√Hz. For comparison, the Johnson noise of a resistive 100MΩ source is about 1300 nV/√Hz.

1/f noise

At very low frequencies the input noise power of a JFET rises as the inverse of frequency. That is why this noise is referred to as 1/f noise. When expressed as noise voltage, this means that the noise rises at a rate of 3dB/octave as frequency decreases. In a good JFET, the 1/f spot noise at 10Hz may be twice the spot noise at 1kHz (up 6dB) when expressed as nV/√Hz.

The noise might typically be up by 3dB at 40Hz. 1/f noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice.[2] The improved processing of the LS844 contributes to reduced 1/f noise.

By comparison, a good JFET op amp with input noise of 10 nV/√Hz at 1kHz may have its noise up by 3dB at 100Hz and the spot noise at 10Hz might be up by 10dB. At 1Hz that op amp may have spot noise on the order of 65 nV/√Hz.

Generation-recombination noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as G-R noise. This *excess noise* is governed by fluctuation in the number of carriers in the channel and the lifetime of the carriers. G-R noise manifests itself as drain current noise. When referred back to the input by the transconductance of the JFET, it is expressed as a voltage noise.

Like 1/f noise, G-R noise results from process imperfections that have created crystal lattice damage or charge trap sites. In contrast, however, G-R noise is not limited to low frequencies. In fact, it is flat up to fairly high frequencies, usually well above the audio band. The G-R noise power spectral density function is described in [2] as:

$$\overline{S_{G\text{-}R(f)}}/N^2 = [(\Delta N)^2/N^2] * [4\tau/(1 + (2\pi f\tau)^2]$$

where $\overline{(\Delta N)^2}$ is the variance of the number of carriers N, and τ is the carrier lifetime.

Above a certain frequency, the G-R noise power decreases as the square of frequency. When expressed as noise voltage, this means that it decreases at 6 dB/octave. The point where the G-R noise is down 3dB can be referred to as the G-R noise corner frequency. That frequency is governed by the carrier lifetime, and in fact is equal to the frequency corresponding to a time constant that is the same as the carrier lifetime.[2] We have,

$$f_{G\text{-}R} = 1/2\pi\tau$$

where τ is the carrier lifetime. Leeman Alan

The 6 dB/octave high-frequency roll-off of G-R noise is only an approximation because there are normally numerous sites contributing to G-R noise and the associated carrier lifetimes may be different. As a result, the G-R noise corner frequency is poorly defined and the roll-off exhibits a more shallow slope than 6 dB/octave over a wider range of frequencies. The inflection in the JFET's noise vs. frequency curve may thus be somewhat indistinct. The important take-away here is that excess G-R noise can often exceed the thermal channel noise contribution and thus dominate voltage noise performance of a JFET.

JFET voltage noise spectrum and contributors

The idealized noise spectral density graph in Figure 1 illustrates how the three voltage noise contributors act to create the overall noise versus frequency curve for a JFET. In the somewhat exaggerated case illustrated, G-R noise dominates thermal channel noise.

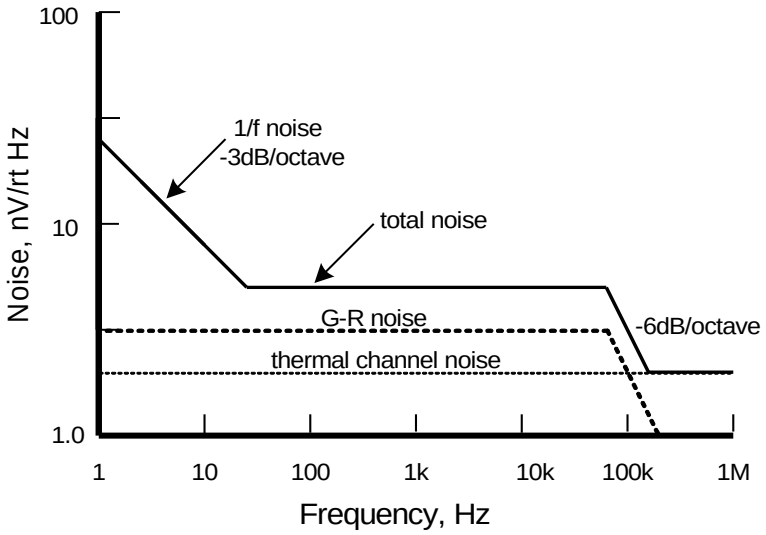

Figure 1: JFET Voltage Noise

LS844 Noise improvement

The LS844 noise advantage derives from process improvements that reduce device imperfections. Those imperfections create G-R noise and 1/f noise. Such process imperfections include crystal lattice damage and charge trap sites. Put simply, most JFETs are not as quiet as they can be. The process improvements made in the LS844 have reduced both 1/f noise and G-R noise.

The common substrate

The LS844 is a monolithic dual JFET in which the substrate is shared between the two integrated JFET devices. The two gates are isolated from the common substrate through reverse-biased substrate diodes as shown in Figure 2. The anodes of these diodes are connected to the gates while the cathodes are connected to the common substrate. The substrate is not normally accessible, and it harmlessly floats as a result.

In some applications it is important to take these isolation diodes and the common substrate into consideration. The 6-pin versions of the LS844 simply
float the substrate, while the 8-pin SOIC package brings
out the substrate for possible connection by the user. In some applications the floating substrate can be a very weak source of crosstalk between the gates. In other applications, the DC voltage to which the substrate floats may be of interest. The gate-substrate capacitance, which is a function of gate-substrate reverse bias, may influence performance in some applications. In some applications it may be useful to connect the substrate to a fixed DC voltage. Another possibility is to bootstrap the substrate with signal to yet further reduce the capacitive effects of the substrate diodes.

Limits on the operating bias voltages of the two sections of the dual JFET must be considered. This is usually not an issue when the dual JFET is employed as a differential pair, but may be an issue in some other circuit arrangements.

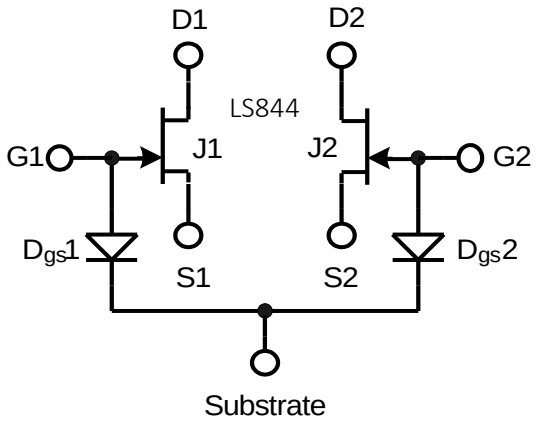

Figure 2: LS844 Common Substrate

JFET Buffers

Figure 3 shows the LS844 connected as a simple unity-gain source follower buffer. In (a) an output voltage offset equal to V_{gs} will result. If a dual JFET like the LS844 is used, the circuit in (b) can be used. J2 acts as the pull-down current source. Because of the tight matching between J1 and J2, the same V_{gs} will appear across R2 and R3, resulting in an output voltage with nearly zero offset. A circuit like this built with a randomly selected LS844 exhibited offset of only 5mV. R3 can be conveniently trimmed to adjust for zero offset. In (c) the gate bias resistor R1 has been bootstrapped to provide higher input resistance. R4 and R5 help stabilize the output voltage to near 0V. Here resistor R2 creates the same voltage offset in the gate of J2 as exists in the gate circuit of J1.

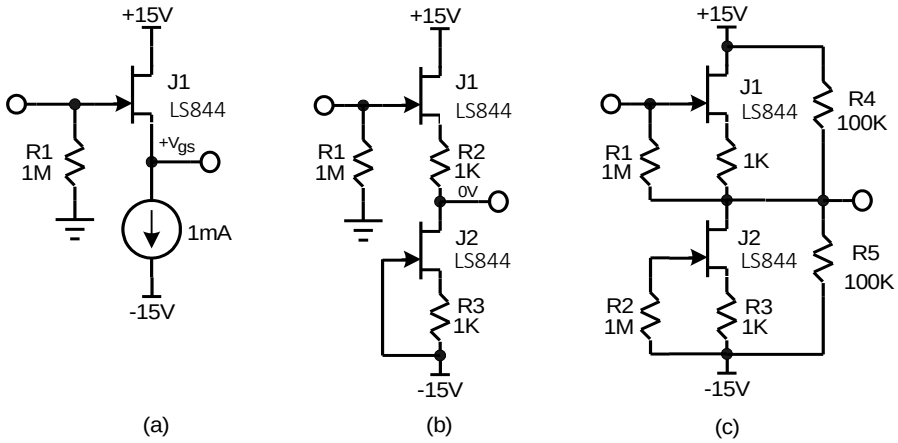

Figure 3: LS844 Source Followers

Figure 4(a) illustrates a differential buffer with low output impedance and low distortion. The key to this design is that each JFET is connected in a complementary feedback pair (CFP) configuration with a PNP transistor, greatly augmenting its effective transconductance and providing distortion-reducing local negative feedback. Notice that the PNP transistors are actually connected as a differential pair, providing additional common-mode rejection. For a given choice of R3 and R4, the value of the current sources can be chosen to make the common-mode DC offset at the output fairly small. If the current sources are controlled by common-mode feedback from the outputs, common-mode offset can be made very small.

Figure 4(b) shows how the differential JFET buffer can be used to build an audio power amplifier with very high impedance differential inputs by buffering the relatively low input impedance presented by the power amplifier connected as a differential amplifier.

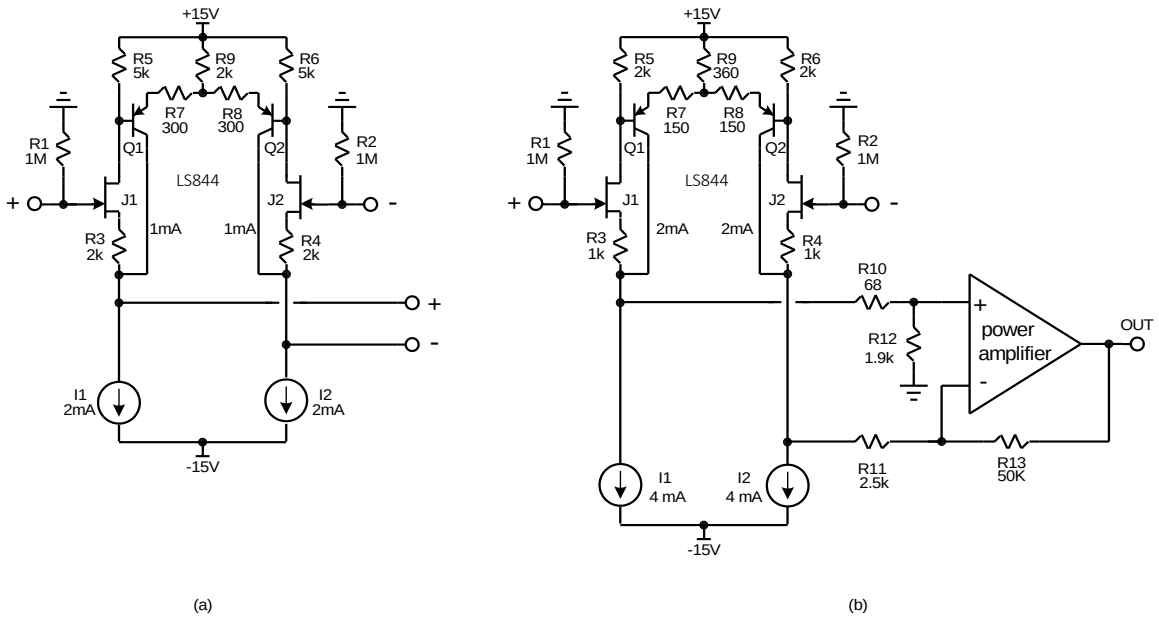

Figure 4: Differential CFP FET Buffer

JFET hybrid op amps

It is often desirable to combine the low noise and simplicity of a good BJT op amp with the high input impedance of a JFET input. IC JFET op amps offer many advantages over BJT op amps, including the absence of input bias current and input noise current. However, they inevitably have greater input voltage noise, often no better than about 8 nV/√Hz. Low-noise BJT op amps easily achieve input voltage noise levels of 2.5 nV/√Hz. It is more difficult to implement good JFETs in a bipolar IC process. For this reason it is sometimes advantageous to employ a discrete JFET input stage in front of a high-performance bipolar op amp.

Figure 5 shows several ways in which a high-impedance JFET input can be added to a BJT op amp so as to reap the advantages of both technologies. In (a) a pair of source followers is simply put in front of the op amp, eliminating the BJT input bias current and input noise current. This arrangement has the disadvantage that the input noise of the op amp adds to that of the JFETs.

In (b) a JFET differential pair with a gain of 10X is placed in front of the op amp. The gain of the JFET stage swamps out the noise contribution of the op amp and increases total open-loop gain by 20dB. If a unity-gain compensated op amp is used, the arrangement must be used with closed loop gain greater than 10 for stability. In this case, a 20dB gain stage can be made that has the same high open-loop gain as the op amp were it used by itself in a unity-gain configuration. In some cases the extra pole created at the input of the op amp may require more conservative frequency compensation.

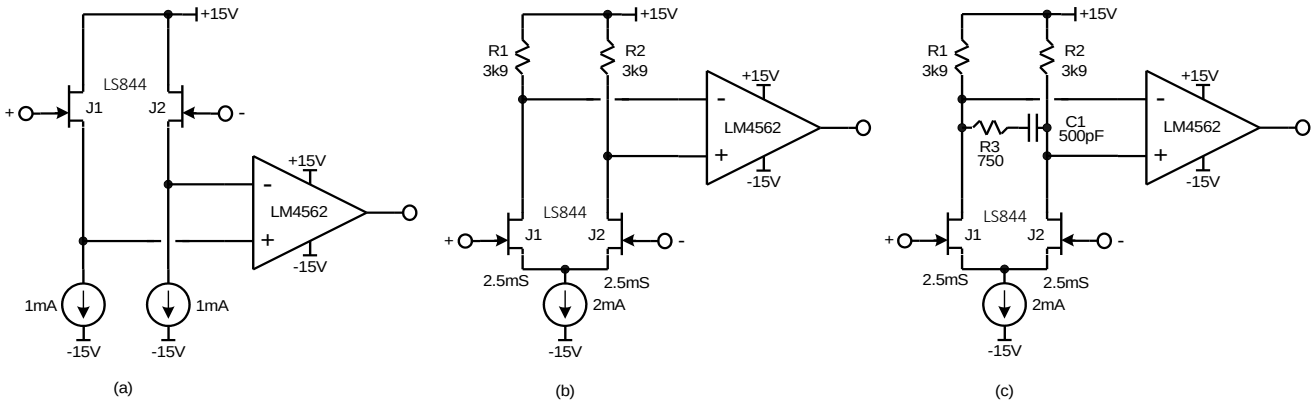

Figure 5: JFET Op Amps

In (c), a compensation arrangement is shown that allows the circuit of (b) to be configured for closed loop gain as low as unity. This is accomplished by R3 and C1, which add a pole-zero pair that decreases open-loop gain by 20dB at high frequencies well before the unity loop gain frequency is reached. The overall effect is like that of so-called two-pole compensation (TPC) sometimes used in feedback amplifiers to achieve higher loop gain at lower frequencies.

There is, however, a very important caveat with this arrangement when used at low closed-loop gain: the circuit is susceptible to latch-up. If the op amp output drives the gate of J2 to the point where it runs out of drain voltage headroom, the circuit may latch to the positive rail. Such behavior is much more likely when the feedback network provides little attenuation as in circuits with unity or low closed-loop gain.

Cascoded JFETs

Single-ended and differential JFET amplifier stages are often cascoded in order to add voltage headroom, reduce Miller effect or to increase output impedance of the stage. The cascode device can be either a BJT or another JFET. If the cascode device is a JFET, all of the signal current from the amplifying JFET passes through the cascode device(s) and no noise is added to the signal. If the cascode device is a BJT, some noise will be added as a result of base current noise flowing from the base to the cascode reference voltage. This adds noise to the signal. However, this noise must be put into perspective in comparison with the noise of the amplifying JFET. This can be evaluated by simulation. It is important that the BJT cascode transistor be a low-noise device with high beta.

Figure 6 shows some simple circuits where the amplifying JFET is cascoded. Sometimes it is necessary to cascode a JFET in order to achieve higher bandwidth by eliminating the Miller effect multiplication of the gate-drain capacitance, even in cases where C_{rss} is already low as with the LS844. Cascoding may also be necessary when higher-voltage rails are used or when it is desirable to keep the drain-source voltage of the amplifying JFETs small to minimize dissipation or noise.

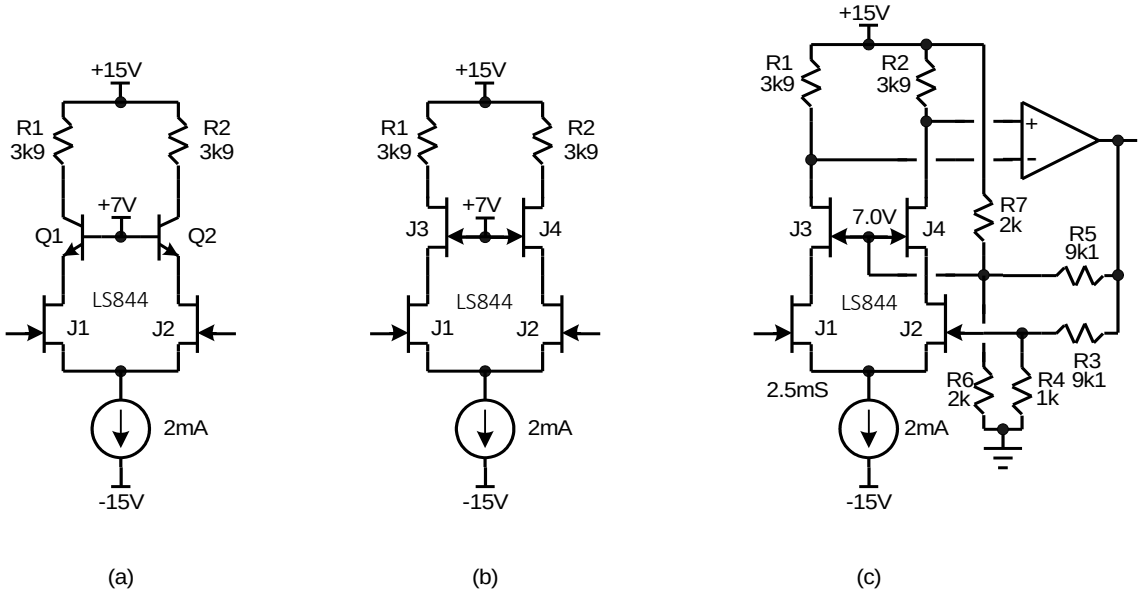

Figure 6: JFET Cascodes

Figure 6(a) shows a conventional arrangement where bipolar transistors are used for the cascade function. Some shot noise from the base current is added to the signal. In (b), JFETs are used for the cascodes, largely eliminating any noise penalty from the use of a cascode.

The circuit in (c) bootstraps the drains of J1 and J2 so as to nearly eliminate the effective input capacitance from C_{rss}. This is done by driving the gates of cascodes J3 and J4 with a replica of the feedback signal that is fed to the gate of J2. This is referred to as a *driven cascode*. Although the cascode circuits illustrated here are all differential cascodes, all of the principles and techniques apply to single-ended cascode circuits as well.

Phono preamp

The LS844 is especially attractive for use in high-performance moving magnet (MM) phono preamplifiers. It can achieve very low noise while presenting very high input impedance to the MM cartridge. The absence of input bias current in the JFET design eliminates input noise current from which BJT designs suffer. Resistance to EMI and a soft overload characteristic make the JFET choice even more attractive.

The MM cartridge source impedance rises at higher frequencies due to the resonance formed by the cartridge inductance (on the order of 300-600 mH) and the load capacitance. This resonance usually lies around 18-22kHz and can have substantial Q. At the resonance frequency, the impedance can rise to almost the nominal load resistance of 47k.

This raises the possibility of cartridge interaction with the nonlinear input capacitance of the amplifier. The low input capacitance of the LS844 JFET pair reduces cartridge interaction and high-frequency intermodulation distortion. Moving magnet cartridges are usually designed to work with a specific loading capacitance on the order of 200pF, so an input stage with capacitance on the order of 20pF, like that of an LSK389, may create a significant disturbance, especially given that the JFET input capacitance can be nonlinear.

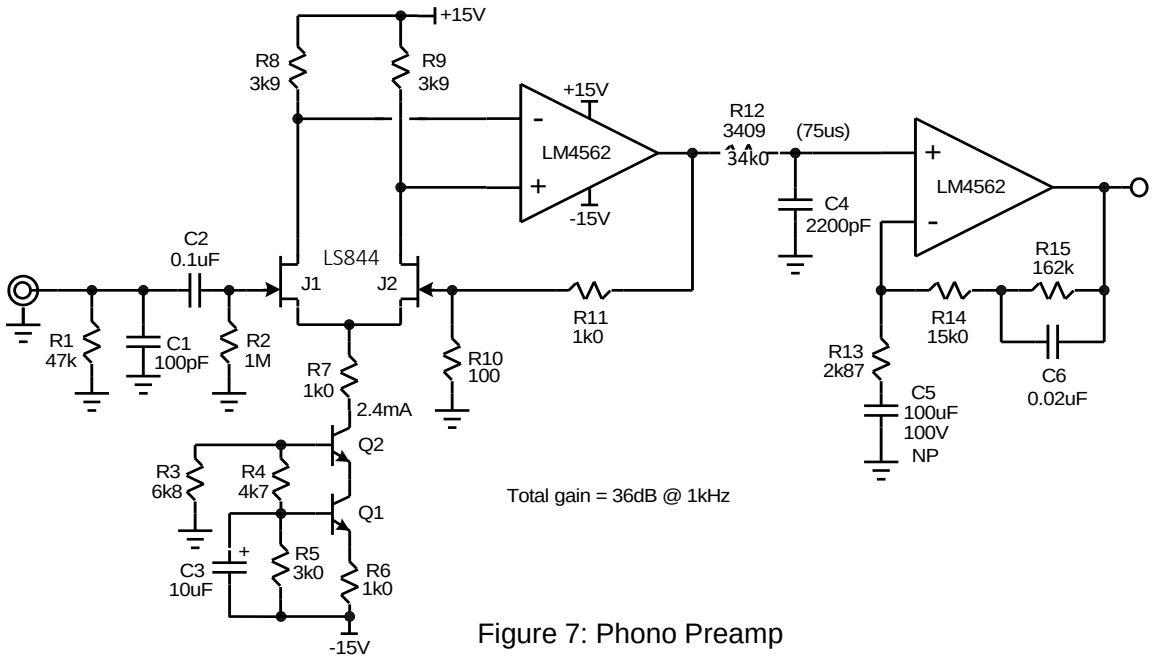

Figure 7: Phono Preamp

Figure 7 illustrates a phono preamp design that incorporates the LS844 to achieve low noise and high input impedance. The circuit consists of a hybrid JFET-bipolar op amp that uses the LS844 as its low-noise input stage. The low-distortion, low-noise LM4562 completes the hybrid operational amplifier, which is configured for a flat gain of 21dB. The 75us high-frequency corner of the RIAA equalization characteristic is implemented by R12 and C4. The remainder of the RIAA equalization implements time constants at 3180 and 318µs. It is implemented with the second half of the LM4562 op amp and the surrounding feedback network. Total gain of the preamp is 36dB at 1kHz. The LS844 JFET input stage provides exceptional immunity to EMI.

The author's VinylTrak phono preamp [3] uses a similar arrangement, but the front-end stage is a discrete 20-dB amplifier without negative feedback. That design provides a true high-impedance differential input and very soft overload characteristics. The small signal levels from a moving magnet phono cartridge allow distortion in the no-feedback arrangement to be very low.

Dynamic microphone preamp

The requirements for a dynamic microphone preamp are not unlike those of a phono preamp, since the voltage levels and source impedance are similar. Low input voltage and current noise is important. The microphone preamp does not require equalization, but it must accept a balanced input and have a very large controllable gain range. The LS844's combination of low noise and low input capacitance make it an ideal device for this application. Its strong resistance to EMI effects and its soft overload characteristics further enhance sound quality.

The LS844 front-end can be implemented as a differential amplifier without negative feedback. This provides a true high-impedance differential input with exceptionally soft overload characteristics. The input stage consists of a degenerated differential a pair of JFETs, each with a current source connected to the source. The gain of this stage is set by a variable resistance connected from source to source. Drain load resistors create a differential output that is fed to an op amp configured as a differential amplifier. In such a design, the relatively low transconductance of the JFETs limits the amount of gain that can be obtained.

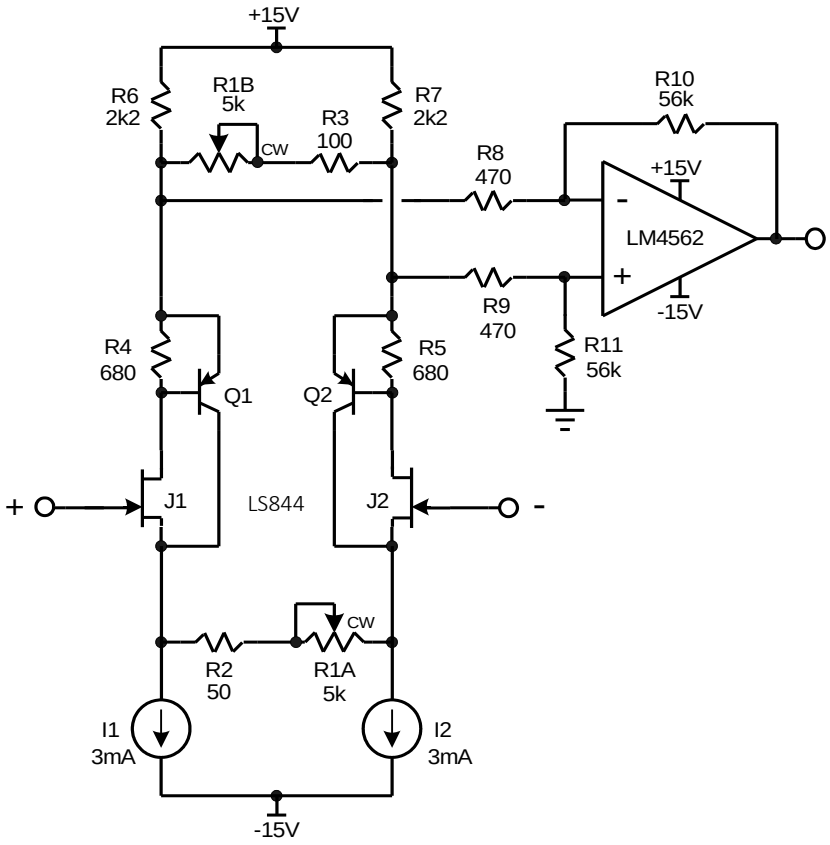

Figure 8: Dynamic Mic Preamp

An improved design is shown in Figure 8. Each JFET is configured as a complementary feedback pair (CFP) by adding a PNP transistor in the drain circuit. This arrangement increases the effective transconductance of the JFET by a factor of about 50 and provides local distortion-reducing feedback.

The JFETs are biased at 1mA and the BJTs are biased at 2mA. Gain control over a wide range is difficult to achieve with a single variable resistance in the source circuit, so a second pot ganged with the first is added in a differential shunt arrangement in the drain circuit. A gain adjustment range of 6-60dB is achieved with a single knob, and is usably distributed with respect to pot rotation even when using linear pots. The use of log-taper pots can provide an even more uniform distribution of attenuation vs. rotation.

Input noise is only 5 nV/√Hz at the highest gain setting and harmonic distortion is no more than 0.012% at an output level of 5V peak. At a nominal line level of 1V rms, THD is 0.003% at a 60dB gain setting and falls below 0.001% at gain settings less than +50dB. Even though the circuit appears differential and symmetrical, distortion is dominated by the much more benign second harmonic. This is due to the asymmetry created in the drain circuit by the differential op amp configuration. It results in different signal amplitude at the drains of J1 and J2. Distortion above the 3rd harmonic is virtually absent.

Condenser microphone preamp

The LS844's combination of low noise and low input capacitance make it an ideal device for the input stage of condenser and electret microphones.

A condenser microphone typically consists of a condenser microphone capsule and a built-in amplifier. The output of the condenser microphone is then fed to the input of a conventional dynamic microphone preamp located in the mixing console. The condenser microphone capsule comprises a diaphragm capacitor that is charged to 40-60V. It produces a voltage when the acoustic vibrations of the diaphragm change the capacitance while charge is conserved. The capacitance may be as small as 5pF but is often in the neighborhood of 50pF. The output impedance of the capsule is thus extremely high, and the microphone preamp functions mainly as a buffer, since the output voltage of the capsule is fairly high in comparison to the output voltage of a dynamic microphone.

The extremely high capacitive source impedance of the capsule means that the amplifier must present an extremely high load resistance in order to preserve low frequency response. This resistance may be on the order of 1-10 GΩ. For the same reason, the preamplifier input capacitance must be very low, especially if it is nonlinear like that of a semiconductor junction. The low input capacitance of the LS844 is an advantage here. In fact, in condenser microphone preamplifiers the drain of the JFET is usually bootstrapped with signal to further reduce the effect of C_{rss}. While most condenser microphone preamps use a single-ended JFET input stage, the differential amplifier arrangements made possible by the dual monolithic LS844 can provide lower distortion in the presence of the fairly high input voltages that can be present with a condenser microphone capsule under high SPL conditions.

The small gate input current of a JFET can come into play in circuits like a condenser microphone preamplifier. The input is AC-coupled and the gate is biased with a resistor as large as 10GΩ so as to provide extremely high input impedance. The JFET's gate input current flows into the resistor, creating a positive voltage offset. The maximum operating value of gate current for the LS844 is 25pA at 25°C (2pA typ.).

This gate input current will create an offset of +250mV. Moreover, the gate leakage current will double every 10°C. Consider a condenser microphone lying in the hot sun reaching a temperature of 45°C. Maximum gate current could reach 100pA, with a resulting input offset voltage of +1V. Such an offset can be disruptive to some circuits. Offset voltage created by gate current flowing in the very large gate return resistor can be controlled by a DC servo connected to the return end of that resistor.

The voltage gain of the preamp may often be on the order of 20dB or less. In fact, for more sensitive capsules and high sound levels, attenuation of the signal may be necessary. A useful approach to such attenuation is to employ an input pad that creates a capacitance voltage divider with an attenuation of perhaps 20dB. A 5pF capsule with a 47pF shunt capacitance will enjoy such a level of attenuation. The low noise of the LS844 means that the input attenuator can be engaged over a wider operating dynamic range. Finally, the condenser microphone electronics must be powered by so-called “phantom” powering. Only a few milliamperes are available, so low-power electronics are a must.

Piezo accelerometer charge amplifier

Figure 9 shows a Piezo accelerometer charge amplifier. In this design, the gain is set by a shunt feedback arrangement that uses capacitors instead of resistors. The gain is equal to the ratio of the transducer capacitance to the feedback capacitance C1. This amplifier incorporates an extremely high gate return resistance of 10GΩ.

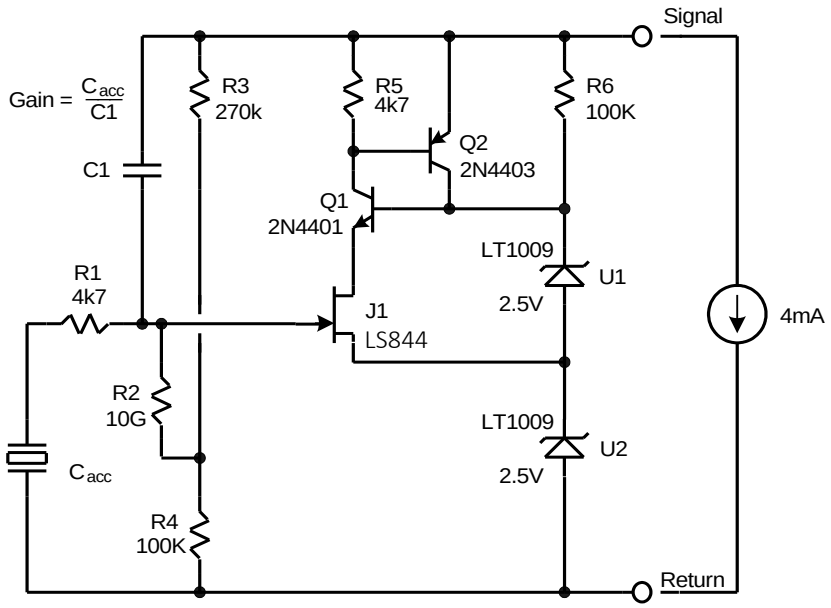

Figure 9: Piezo Accelerometer Charge Amplifier

Discrete JFET amplifier

Figure 10 shoes a discrete JFET amplifier that employs a folded cascode and a diamond buffer output stage. This is much like the low-noise discrete input stage of the author's VinylTrak phono preamplifier [3]. As shown the amplifier is operated open-loop at a gain of about 10, as determined by shunt resistor R14. The amplifier in this configuration offers a true balanced high-impedance

input, exceptional resistance to EMI and a very soft overload characteristic.

The amplifier can also be used as an operational amplifier with fairly high open-loop gain if R14 is removed and suitable feedback compensation is added. In any configuration, the use of the folded cascode architecture offers wide bandwidth.

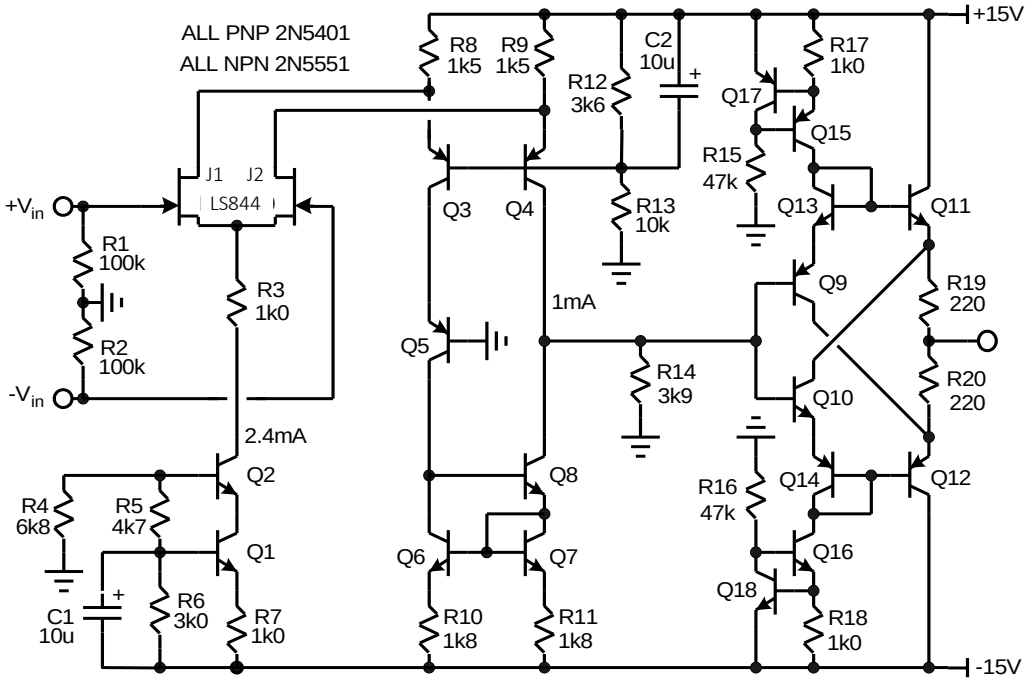

Figure 10: JFET Discrete Amplifier

Power amplifier with JFET input

The input stage for an audio power amplifier is often a long-tailed differential pair (LTP) implemented with bipolar transistors. Dual JFETs like the LS844 provide a better alternative. Many believe that the sound is better, possibly due to its much softer overload characteristic. Others believe that its superior resistance to EMI is important. The absence of input bias current for the JFET often has advantages in DC offset control and selection of input stage operating impedances.

While the noise characteristics of a power amplifier are often not as critical as those of a preamp, it is still important to achieve low noise because there is no volume control in the power amplifier to reduce noise from the input stage under normal listening conditions. This is particularly so when the amplifiers are used with high-efficiency loudspeakers. For this reason the use of a low-noise JFET like the LS844 is desirable.

Figure 11 shows a simple100 watt audio power amplifier with a JFET input stage incorporating an LS844 differential pair. Input noise is only 6 nV/√Hz. The 60V breakdown of the LS844 allows the use of a JFET input without a cascode for amplifiers with nominal rail voltages of up to 50V, assuming that the rail voltages do not exceed 60V under worst case light-loading and high mains voltage conditions.

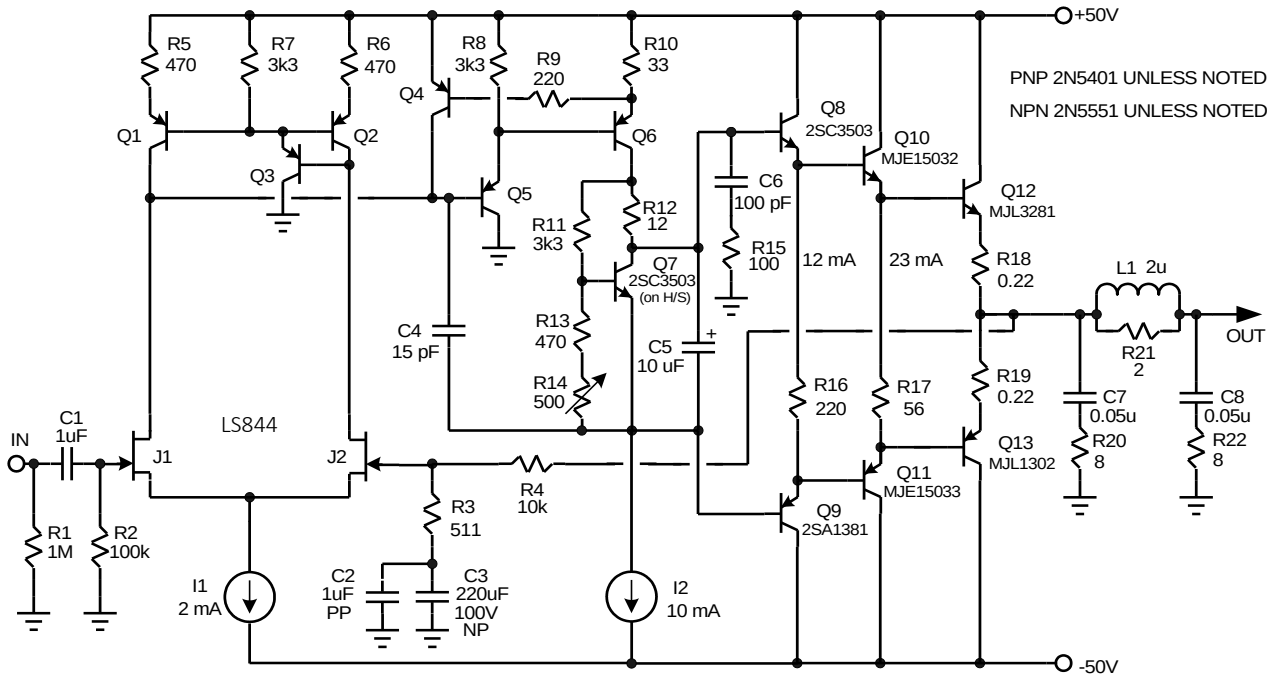

Figure 11: Power Amplifier

Assuming that the rail voltages do not fall to under 45V under full power into an 8Ω load, the amplifier is capable of output power in excess of 100 watts into 8 ohms (corresponding to a peak output voltage of 40V). For simplicity, details of the current sources and output protection circuits are not shown. The design of audio power amplifiers like this can be found in the book *Designing Audio Power Amplifiers*, written by the author. Useful information can also be found on the author's web page at www.cordellaudio.com [4].

Conclusion

With its low noise, low input capacitance and tight matching, the LS844 is ideal for numerous audio and instrumentation applications. Its low capacitance also make it a good candidate for many high-frequency circuits.

References

[1]. Designing Audio Power Amplifiers, Bob Cordell, McGraw-Hill, 2010.

[2]. Alicja Konczakowska and Bogdan M. Wilamowski, *Noise in Semiconductor Devices*, Chapter 11 in *Industrial Electronics Handbook*, vol. 1, *Fundamentals of Industrial Electronics*, 2nd edition, CRC Press 2011.

[3]. Bob Cordell, *VinylTrak – A full-featured MM/MC phono preamp*, Linear Audio, vol. 4, September 2012, www.linearaudio.net.

[4]. Web site www.cordellaudio.com.