LINEAR SYSTEMS

Linear Systems

2024 DATA BOOK

Quality Through Innovation Since 1987

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Linear Systems'
2024 Data Book

Testimonials

"One of the main reasons we offer a lifetime warranty for our products is because we can count on Linear Systems. The Linear Systems' LSK389B J-FET is so reliable that in the rare event a faulty unit is discovered, it's the very last variable we check. The LSK389B J-FET simply doesn't fail!"

Rodger Cloud
www.cloudmicrophones.com

"I believe that selecting Linear Systems' LSJ74 for our Halo Integrated Amplifier has contributed to the unprecedented number of rave reviews and awards it's received. Parasound's product development team commends Linear Systems for providing customer support that is top-notch."

Richard Schram
www.parasound.com

"Our QCL instrument has the lowest noise commercially available and is used for pharmaceutical process quality control and trace gas emissions monitoring. Noise testing the instrument is critical to ensuring performance. Our test equipment uses the Linear Systems' LSK389 JFET. The precision of the LSK389 makes verifying the precision of our instruments possible."

Lisa Mueller
www.teamwavelength.com

Introduction

Welcome to the 2024 edition of the Linear Systems Data Book. Here we present all our devices in one single document to give you a complete overview of our portfolio. We hope that makes it even easier for you to find the right product for your design. Our extensive portfolio offers high-quality discrete components serving a wide range of markets including automated test equipment, professional audio, medical electronics, military and test & measurement. Our products are housed in some of the most advanced, industry-leading small packages, as well as robust industry standard packages giving designers many options. Alongside quality and efficiency, Linear Systems' customers value reliability and a constant supply they can trust. We produce consistently reliable discrete components and we work at every step to safeguard the long-term availability of our manufacturing processes and products, to ensure secure supply for all our customers. In addition, Linear Systems has an on-site testing facility to conduct a full range of production and post-production testing. Specialized capabilities include: Hi-temperature product testing and the highest capacity sub-nanovolt noise production testing capability in the world. We have a long history in the business and broad range of experience. Linear Systems ensures dedicated in-house technical support – from simplifying selection via quick-reference material to in-person technical meetings with our engineering team. All to help you choose the best devices for the most efficient design.

This Data Book provides all Linear Systems' datasheets in one spot. The Table of Contents includes product category, part number and part description, so you can browse the entire product line with ease. There is also a dedicated section on packages, highlighting the latest package innovations and packing options.

Ordering Information and Sampling Policy

Linear Systems does not impose minimum order requirements when ordering directly from the factory. We understand customers may only need a few parts for prototyping, repairs, student projects or DIY designs. Our parts are available to all. We do, however, offer incremental price breaks for increased purchase quantity. Linear Systems also supports customers who require very large quantities for mass production. In this case special high-quantity pricing may be negotiated for bulk purchases of 100,000 plus pieces.

Do you use the LTspice® electronic circuit simulator? The majority of Linear Systems' parts are included in the latest edition of the LTspice® embedded library. Customers often try our products through the Allspice-simulator before ordering.

Would you like to receive samples? Samples including detailed data logs are available upon request.

Interested in a part not listed on our website, or do you need a custom part? Linear Systems offers many non-standard electrical screening and package options.

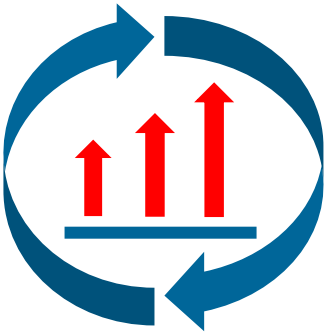
Linear Systems' friendly staff are here to help. For any kind of assistance you can reach us by calling (510) 490-9160 or email us at support@linearsystems.com.

Our Commitment:

Quality and Reliability

Quality is Everything

Linear Systems is ISO 9001:2015 certified. All our processes and manufacturing facilities are subject to regular internal audits.



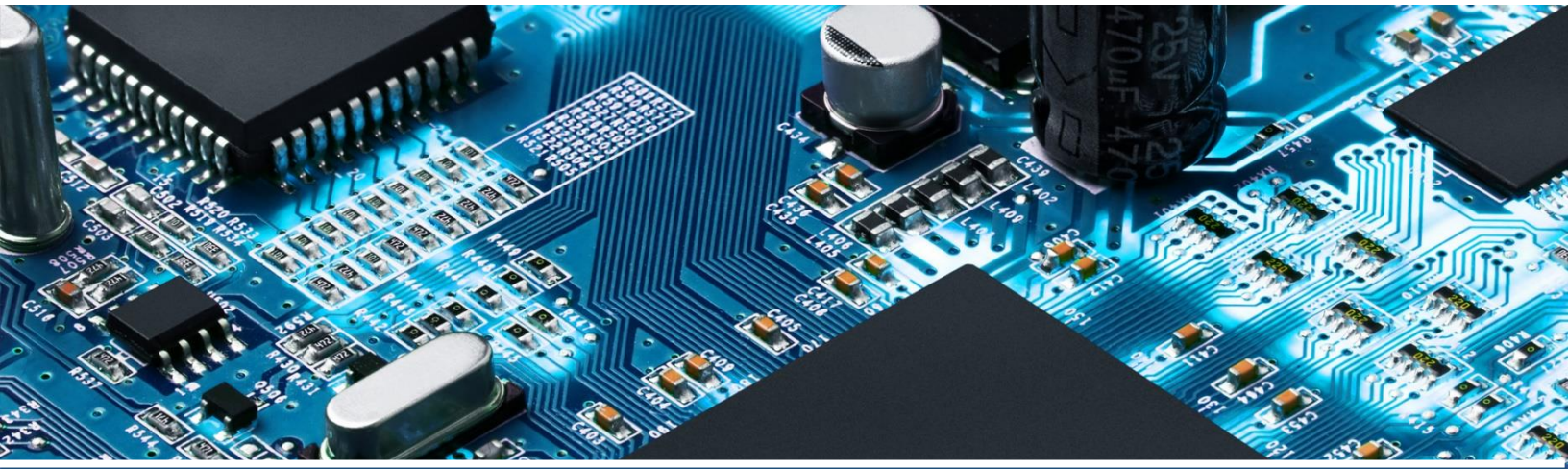
Continuously Improve

Linear Systems' Continuous Improvement Program (CIP) ensures that existing processes are strategically reviewed while each new development builds on past learning. The result is that best practices are always employed.

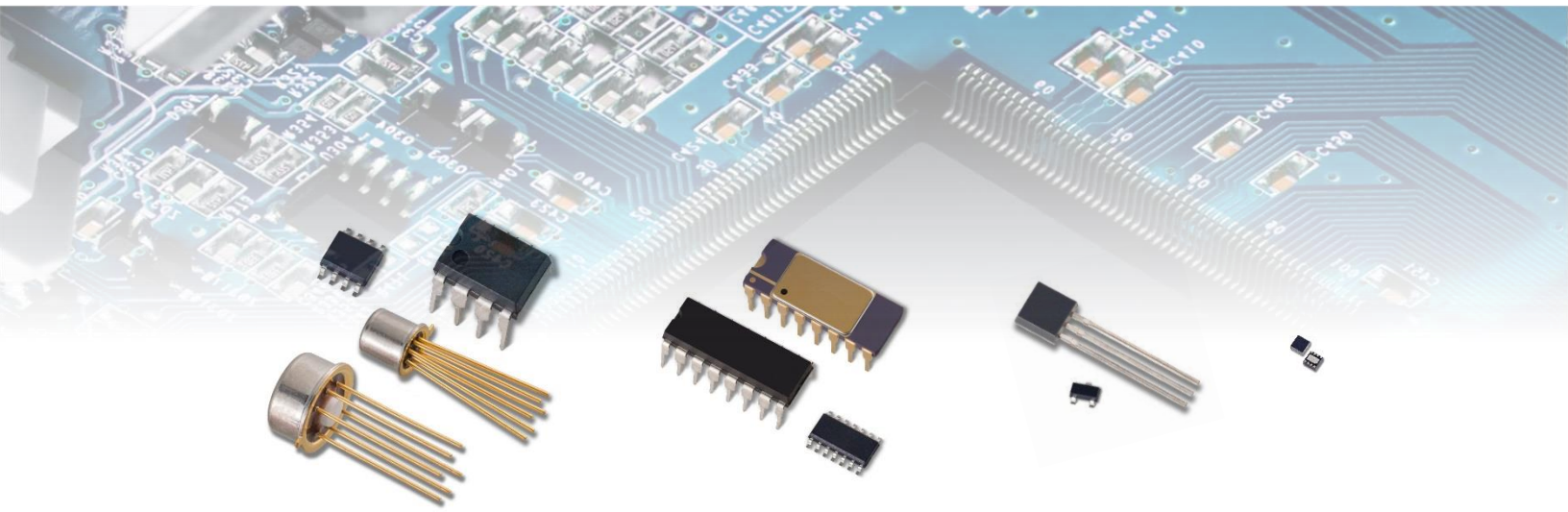
Zero Defect

Zero defect is our goal. To ensure continuous improvement, failure analysis and the determination to find root causes is performed at all stages of development and production by adoption of quality-analysis tools and methods.

LINEAR SYSTEMS **Quality Through Innovation Since 1987**



DISCRETE COMPONENT PRODUCT LINE

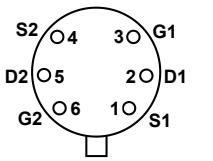


LSK389 A/B/C/D

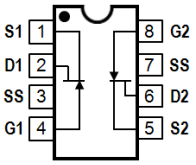
Ultra-Low Noise Monolithic Dual N-Channel JFET Amplifier

INDUSTRY'S FIRST 100% TESTED LOWEST NOISE JFET

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



TO-71 6L
Top View



SOIC 8L
Top View

Features

- Ultra-Low Noise: e_n = 1.3nV/√Hz (typ), f = 1.0kHz and NBW = 1.0Hz
- Ultra-Low Noise: 1.5nV/√Hz (typ), f = 10Hz and NBW = 1.0Hz
- Tight Matching: $|V_{GS1-2}|$ = 15mV max
- High Breakdown Voltage: BV_{GSS} = 40V max
- High Gain: G_{fs} = 20mS (typ)
- Low Capacitance: 25pF (typ)
- Improved Second Source Replacement for 2SK389

Benefits

- Improved System Noise Performance
- Unique Monolithic Dual Design Construction of Interleaving Both JFETs on the Same Piece of Silicon
- Excellent Matching and Thermal Tracking
- Great for Maximizing Battery Operated Applications by Providing a Wide Output Swing
- A High Signal to Noise Ratio as a Result of the LSK389's Low and Tightly Matched Gate Threshold Voltages

Applications

- Audio Amplifiers and Preamps
- Discrete Low-Noise Operational Amplifiers
- Battery-Operated Audio Preamps
- Audio Mixer Consoles
- Acoustic Sensors
- Sonic Imaging
- Instrumentation Amplifiers
- Microphones
- Sonobouys
- Hydrophones
- Chemical and Radiation Detectors

Description

The LSK389 is the industry's lowest noise Dual N-Channel JFET, 100% tested, guaranteed to meet 1/*f* and broadband noise specifications, while eliminating burst (RTN or popcorn) noise entirely. The LSK389 Series, Monolithic Dual N-Channel JFETs were specifically designed to provide users a better performing, less time consuming and cheaper solution for obtaining tighter IDSS matching, and better thermal tracking, than matching individual JFETs. The LSK389's features incorporate four grades of IDSS: 2.6-6.5mA, 6.0-12.0mA, 10.0-20.0mA and 17-30mA, with an IDSS match of 10 percent, a gate threshold offset of 15mV, a voltage noise (en) of 1.3nV/√Hz typical at f = 1.0kHZ, with a Gain of 20mS typical, and 25pF of capacitance typical. The LSK389 provides a wide output swing, and a high signal to noise ratio as a result of the LSK389's tightly matched and low gate threshold voltages. The 40V breakdown provides maximum linear headroom in high transient program content amplifiers.

Additionally, the LSK389 provides a low input noise to capacitance product that has nearly zero popcorn noise. The narrow ranges of the IDSS electrical grades combined with the superior matching performance of the LSK389's monolithic dual construction promote ease of device tolerance in low voltage applications, as compared to matching single JFETs. Available in surface mount SOIC 8L and thru-hole TO-71 6L packages.

Contact the factory for tighter noise and other specification selections. For equivalent single N-Channel version, please refer to the LSK170 datasheet.

Electrical Characteristics @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-40	---	---	V	V_{DS} = 0, I_D = -100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-0.3	---	-1.6	V	V_{DS} = 10V, I_D = 0.1µA
I_{DSS}	Drain to Source Saturation Current	LSK389A	2.6	---	6.5	mA	V_{DS} = 10V, V_{GS} = 0
		LSK389B	6	---	12		
		LSK389C	10	---	20		
		LSK389D	17	---	30		
I_{GSS}	Gate to Source Leakage Current		---	-100	-300	pA	V_{GS} = -25V, V_{DS} = 0
I_{G1G2}	Gate to Gate Isolation Current		---	±1.0	±50	nA	V_{G1-G2} = ±45V, I_D = I_S = 0A
G_{fs}	Full Conduction Transconductance		8	20	---	mS	V_{DS} = 10V, V_{GS} = 0, *f* = 1kHz
e_n	Noise Voltage		---	1.3	1.9	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		---	1.5	4.0	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		---	25	---	pF	V_{DS} = 10V, V_{GS} = 0, *f* = 1MHz,
C_{RSS}	Common Source Reverse Transfer Cap.		---	5.5	---	pF	V_{DG} = 10V, I_D = 0, *f* = 1MHz,

Matching Characteristics @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	---	6.0	15	mV	V_{DS} = 10V, I_D = 1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.9	1.0	1.1	n/a	V_{DS} = 10V, V_{GS} = 0V

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

LSK389A

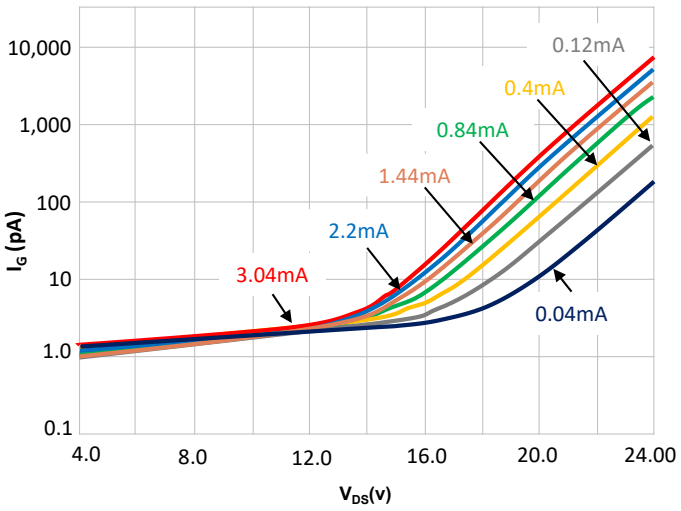


Figure 1. Gate Current (I_G) vs. V_{DS} vs. I_D

LSK389B

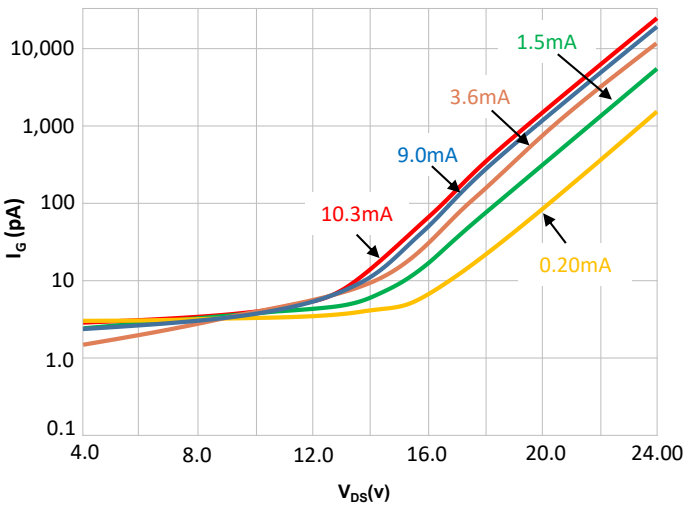


Figure 2. Gate Current (I_G) vs. V_{DS} vs. I_D

LSK389C

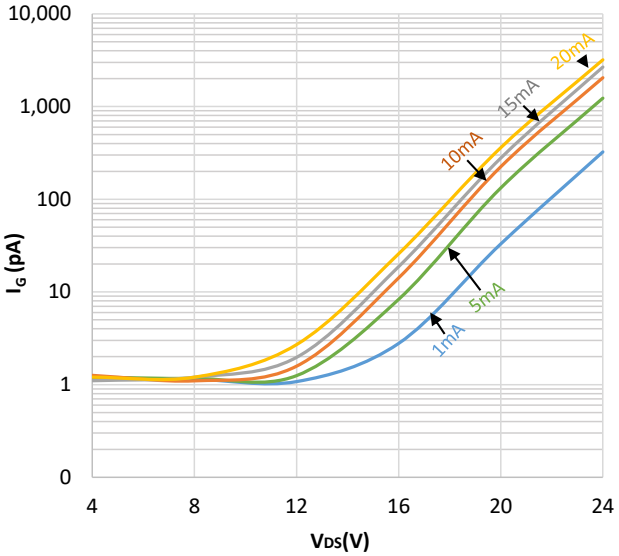


Figure 3. Gate Current (I_G) vs. V_{DS} vs. I_D

LSK389D

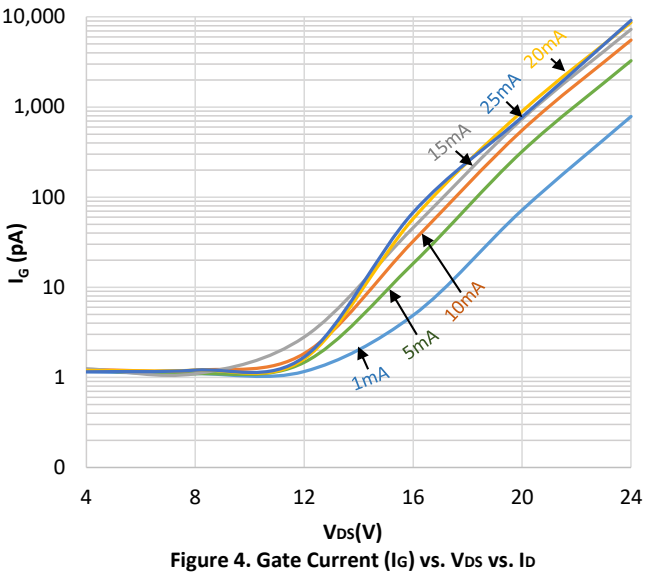


Figure 4. Gate Current (I_G) vs. V_{DS} vs. I_D

Typical Characteristics Continued

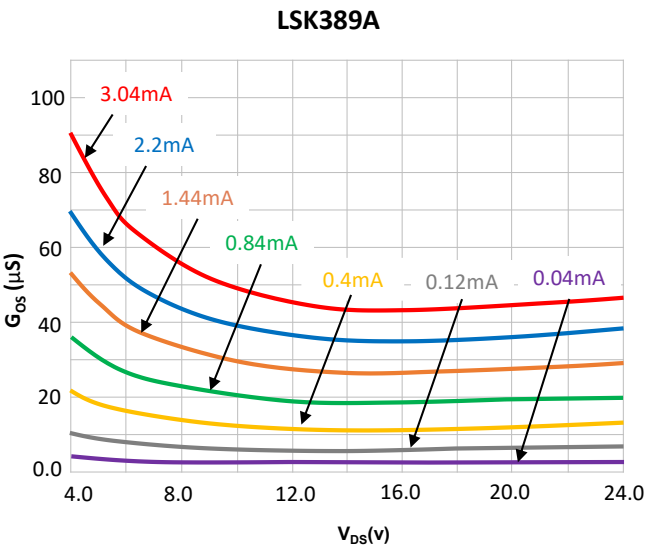


Figure 5. Output Conductance - G_{OS} vs. V_{DS} vs. I_D

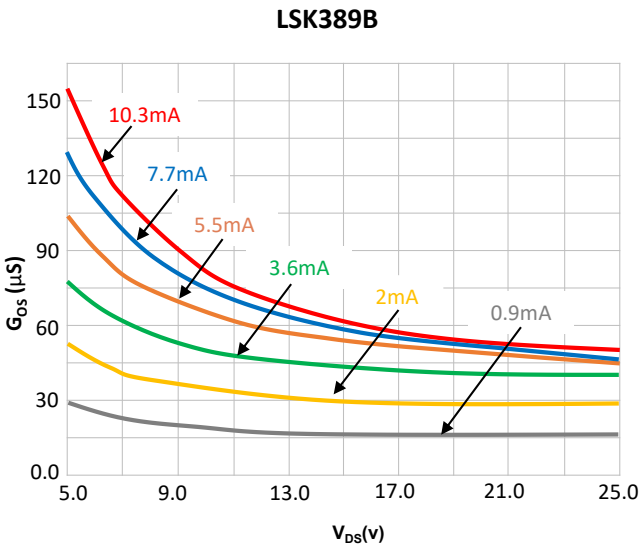


Figure 6. Output Conductance - G_{OS} vs. V_{DS} vs. I_D

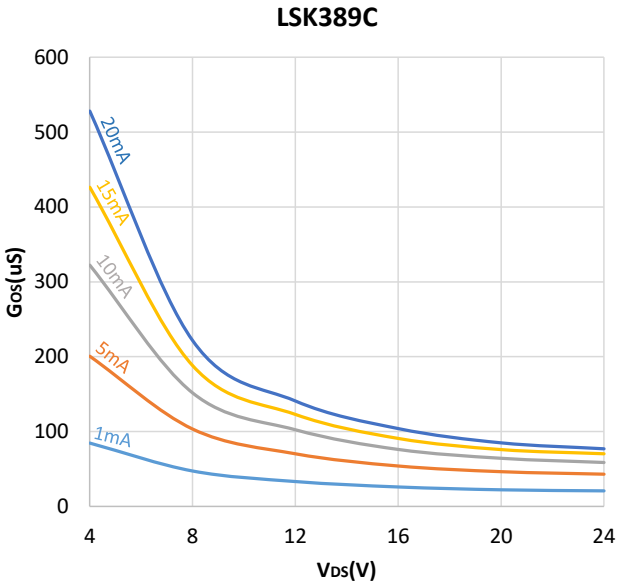


Figure 7. Output Conductance - Gos vs. VDS vs. ID

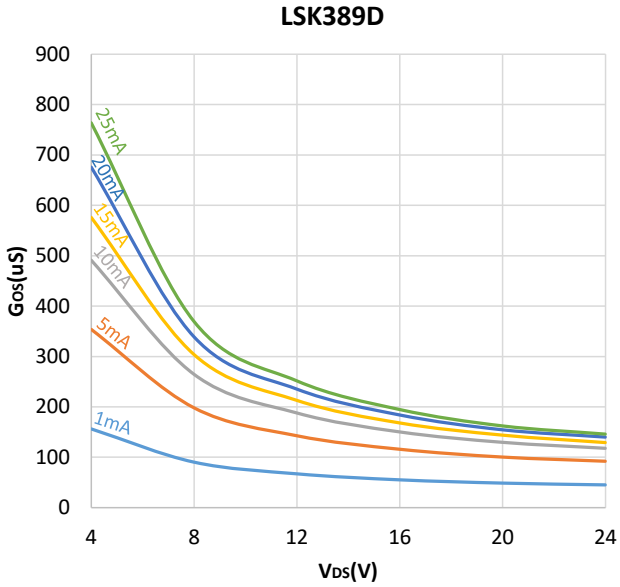


Figure 8. Output Conductance - Gos vs. VDS vs. ID

Typical Characteristics Continued

LSK389A

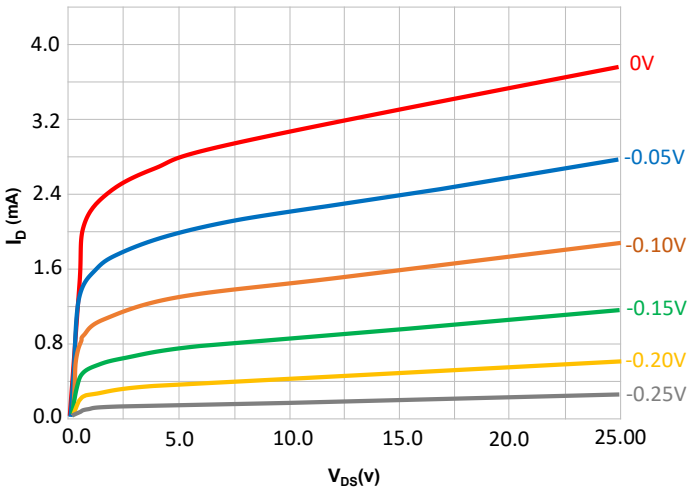


Figure 9. I_D vs. V_{DS} vs. V_{GS}

LSK389B

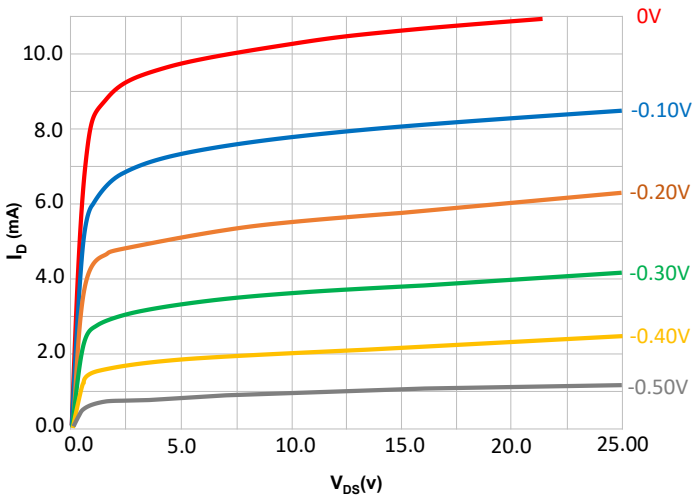


Figure 10. I_D vs. V_{DS} vs. V_{GS}

LSK389C

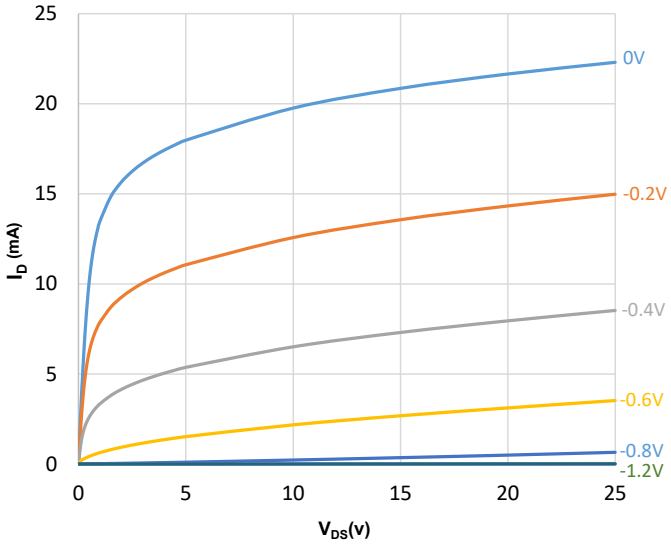


Figure 11. I_D vs. V_{DS} vs. V_{GS}

LSK389D

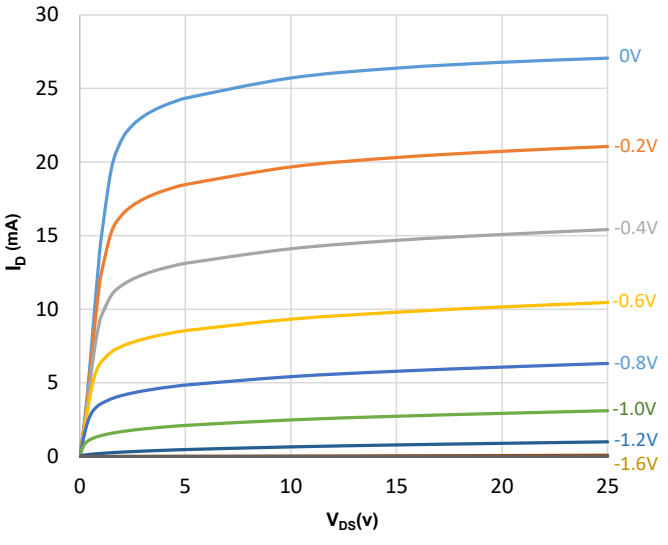


Figure 12. I_D vs. V_{DS} vs. V_{GS}

Typical Characteristics Continued

LSK389A

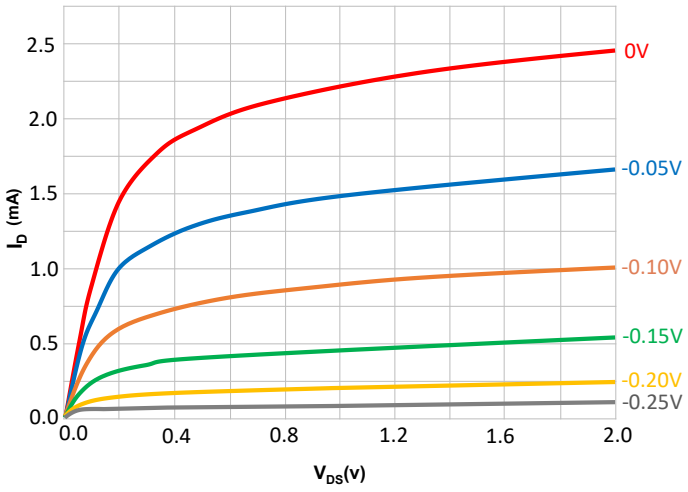


Figure 13. I_D vs. V_{DS} vs. V_{GS}

LSK389B

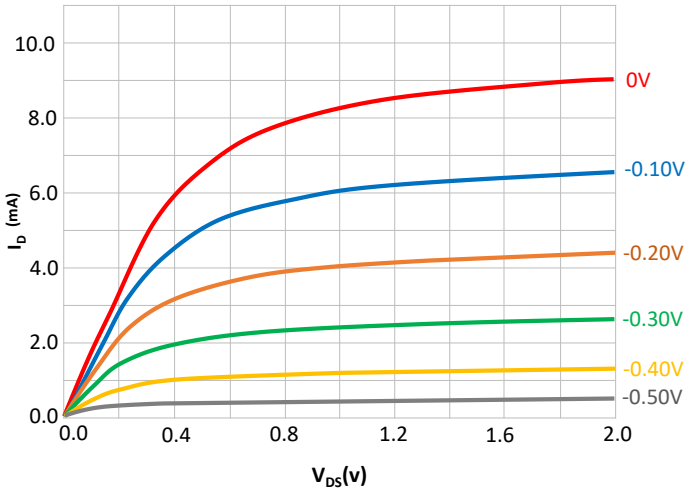


Figure 14. I_D vs. V_{DS} vs. V_{GS}

LSK389C

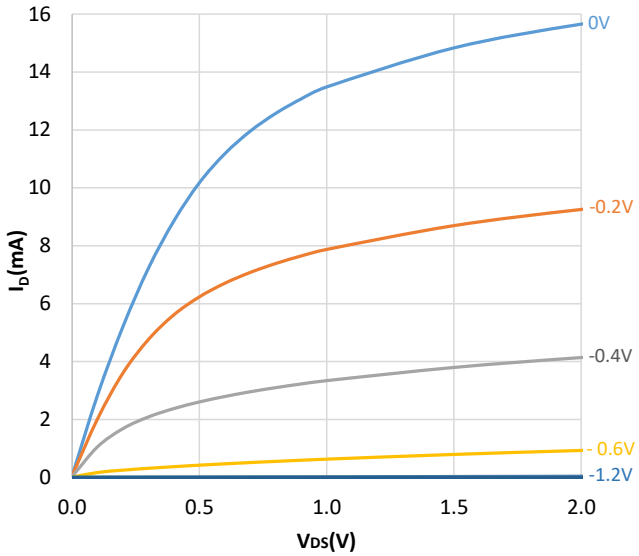


Figure 15. ID vs. VDS vs. VGS

LSK389D

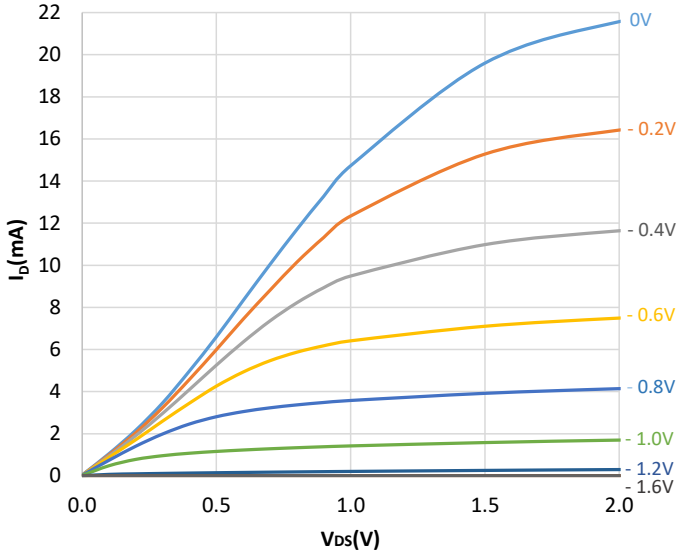


Figure 16. ID vs. VDS vs. VGS

Typical Characteristics Continued

Common Source Forward Transconductance vs. Drain Current
LSK389A & B

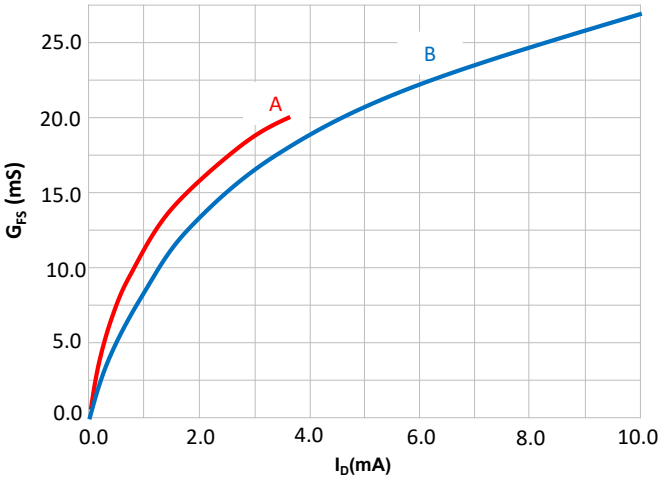


Figure 17. G_{FS} vs. I_D

Common Source Forward Transconductance vs. Drain Current
LSK389C & D

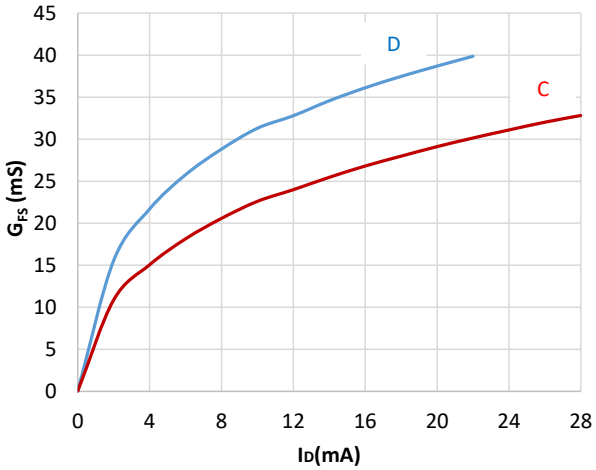


Figure 18. GFS vs. ID

LSK389A & B

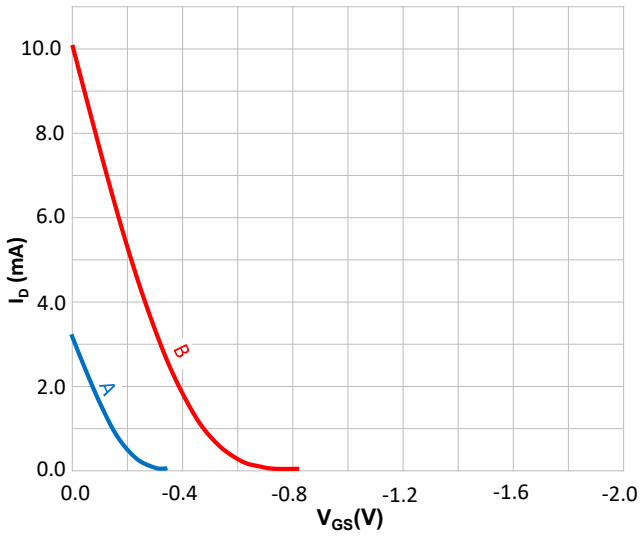


Figure 19. I_D vs. V_{GS}

LSK389C & D

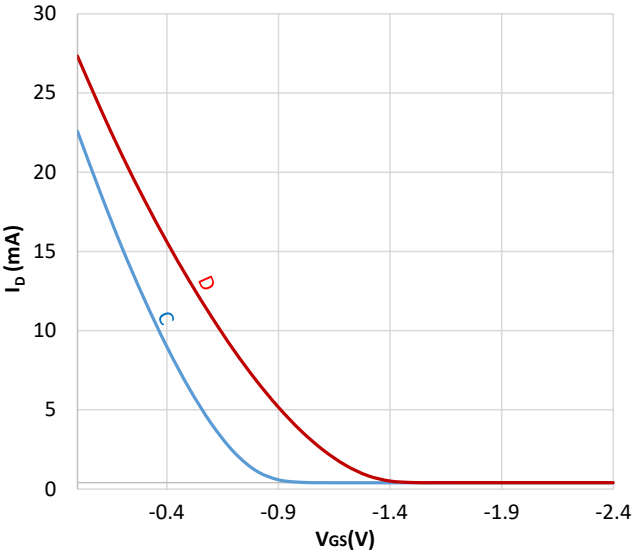


Figure 20. ID vs. VGS

Typical Characteristics

Drain Current Transconductance vs. Gate-Source Cutoff Voltage

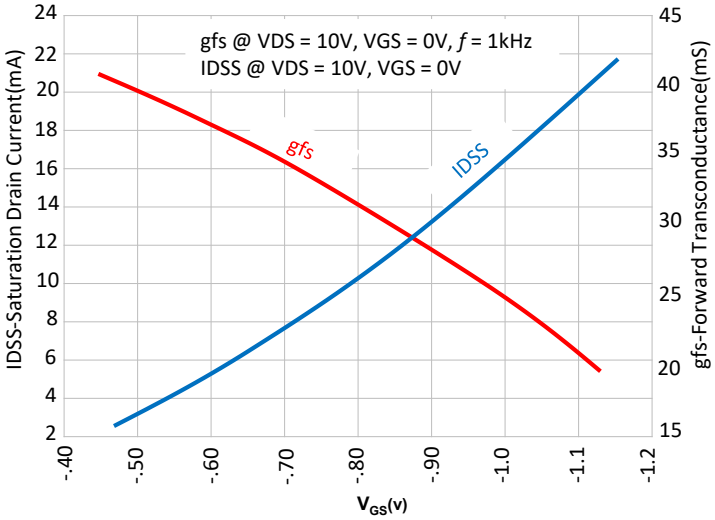


Figure 21. V_{GS} (cutoff) vs. I_{Dss} vs. G_{FS}

Equivalent Input Noise Voltage vs. Frequency

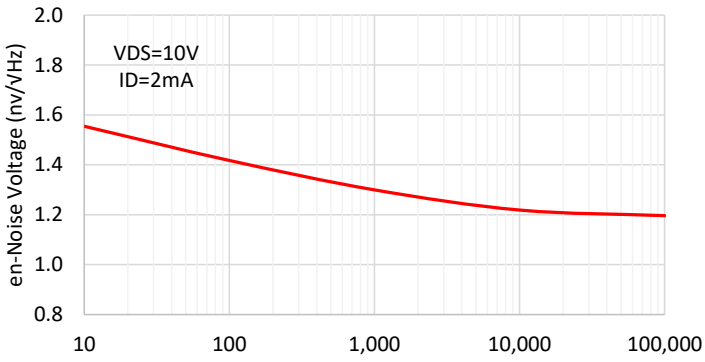
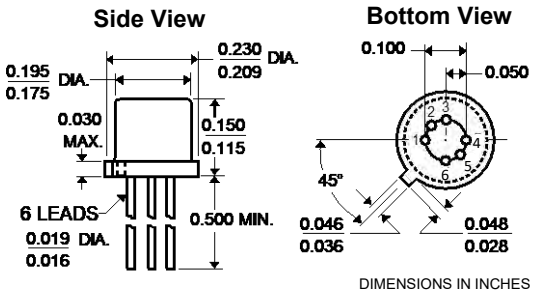


Figure 22.
f - Frequency (Hz)

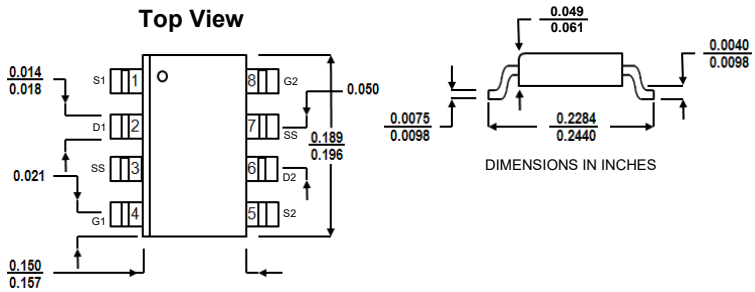
Package Dimensions

TO-71 6 Lead



DIMENSIONS IN INCHES

SOIC 8 Lead



DIMENSIONS IN INCHES

SS: SUBSTRATE, LEAVE THESE PINS FLOATING (N/C)

Ordering Information

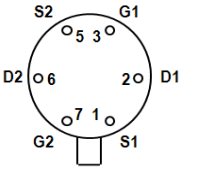
Standard Part Call-Out
LSK389A/B/C or D TO-71 6L RoHS
LSK389A/B/C or D SOIC 8L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
LSK389A/B/C or D TO-71 6L RoHS SELXXXX
LSK389A/B/C or D SOIC 8L RoHS SELXXXX

LSK489A/B

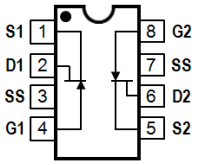
Low Noise, Monolithic Dual N-Channel JFET Amplifier

INDUSTRY'S LOWEST INPUT CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

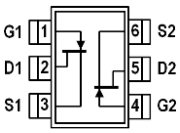
Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	300mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 60V
Gate to Drain	V_{GDS} = 60V
Features	
Low Noise (f = 1kHz, NBW = 1Hz)	e_n = 1.8nV/√Hz
Low Input Capacitance	Ciss = 4pF



TO-71
Top View



SOIC-A
Top View



SOT-23
Top View

* For equivalent single version, see LSK189

Features
- Low Noise: e_n = 1.8nV/√Hz (typ), *f* = 1kHz, NBW = 1Hz
- Very Low Common Source Input Capacitance of C_{ISS} = 4pF – typ
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage I_{GSS} and I_G
- High CMRR 102 dB

Benefits
- Tight Differential Voltage Match vs. Current
- Improved Op Amp Speed Settling Time Accuracy
- Minimum Input Error Trimming Error Voltage
- Lower Intermodulation Distortion Due to Low Input Capacitance

Applications
- Wideband Differential Amplifiers
- High Speed Temperature Compensated Single Ended Input Amplifier
- High Speed Comparators
- Impedance Converters
- Sonobouys and Hydrophones
- Acoustic Sensors

Description
The LSK489 is the industry's lowest input capacitance and low-noise monolithic dual N-Channel JFET. Low input capacitance substantially reduces intermodulation distortion. In addition, these dual JFETs feature tight offset voltage and low drift over temperature range, and are targeted for use in a wide range of precision instrumentation and sensor applications. The LSK489 is available in surface mount plastic SOIC 8L and SOT-23 6L, as well as thru-hole metal TO-71 6L packages. For an equivalent single N-Channel version refer to the LSK189 datasheet. LSK489 TO-71 6L and SOIC 8L are fit, form and pin compatible to the same LSK389 product.

The LSK489 provides a dramatic increase in capabilities for a wide range of low-noise applications. The most significant aspect of the LSK489 is how it combines a noise level nearly as low as the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. The slightly higher noise of the LSK489, versus the LSK389, is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production. Also notice that the LSK489 and LSK389 TO-71 and SOIC packages are the same and pin compatible, therefore, they can be used interchangeably.

Like the Linear Systems LSK389, the LSK489 features a unique design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking, as well a low-noise profile having nearly zero popcorn noise. I_{DSS} range is divided into two segments providing designers improved resolution, which are A grade (ΔI_{DSS} = 6mA) and B grade (ΔI_{DSS} = 7mA). Contact Linear Systems for improved En, I_{DSS}, V_{GS}(off), ΔV_{GS} or any other limits. Based on new limits, LS will assign a new SELXXXX code to be used in shipments.

Matching Characteristics @ 25°C (unless otherwise stated)

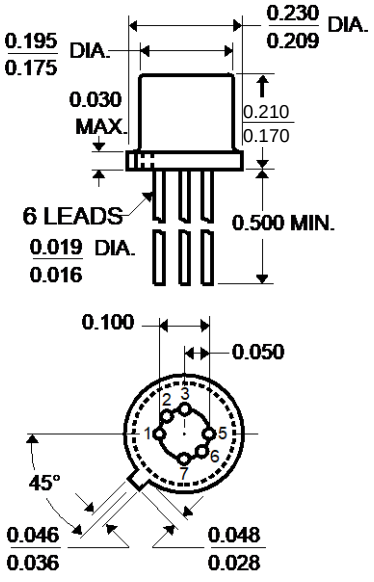
Symbol	Characteristic	Min.	Typ.	Max	Units	Conditions
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	-	8	20	mV	V_{DS} = 10V, I_D = 1mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9	-	1.0	-	V_{DS} = 10V, V_{GS} = 0V
CMRR	**Common Mode Rejection Ratio** $-20 \log \lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	95	102	-	dB	V_{DS} = 10V to 20V, I_D = 200µA
e_n	Noise Voltage	-	1.8	-	nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage	-	3.5	-	nV/√Hz	V_{DS} = 15V, I_D = 2.0mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance	-	4	-	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance	-	2	-	pF	

Electrical Characteristics @ 25°C (unless otherwise stated)

Symbol	Characteristic		Min.	Typ.	Max	Units	Conditions
BV_{GSS}	Gate to Source Breakdown Voltage		-60	-	-	V	V_{DS} = 0, I_D = -1nA
$V_{(BR)G1 - G2}$	Gate to Gate Breakdown Voltage		±30	±45	-	V	I_G= ±1µA, I_D=I_S=0 A (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-1.5	-	-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.5	-	-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}	Drain to Source Saturation Current	LSK489A	2.5	5.5	8.5	mA	V_{DG} = 15V, V_{GS} = 0
		LSK489B	8.0	11.5	15.0		
I_G	Gate Operating Current		-	-2	-25	pA	V_{DG} = 15V, I_D = 200µA
			-	-0.8	-10	nA	T_A = 125°C
I_{GSS}	Gate to Source Leakage Current		-	-	-100	pA	V_{DG} = -15V, V_{DS} = 0
G_{fs}	Full Conductance Transconductance		1500	-	-	µS	V_{DG} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Transconductance		1000	1500	-	µS	V_{DG} = 15V, I_D = 500µA
G_{OS}	Full Output Conductance		-	-	40	µS	V_{DG} = 15V, V_{GS} = 0
G_{OS}	Output Conductance		-	1.8	2.7	µS	V_{DG} = 15V, I_D = 200µA

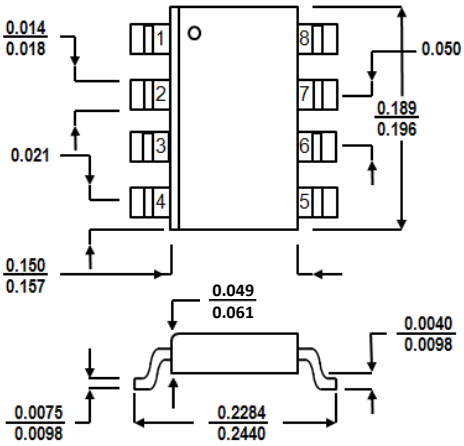
Package Dimensions

TO-71
Six Lead



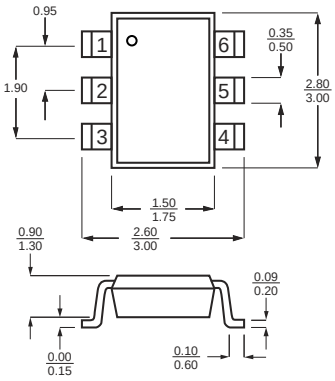
DIMENSIONS IN INCHES

SOIC-A
8 Lead



DIMENSIONS IN INCHES

SOT-23
Six Lead

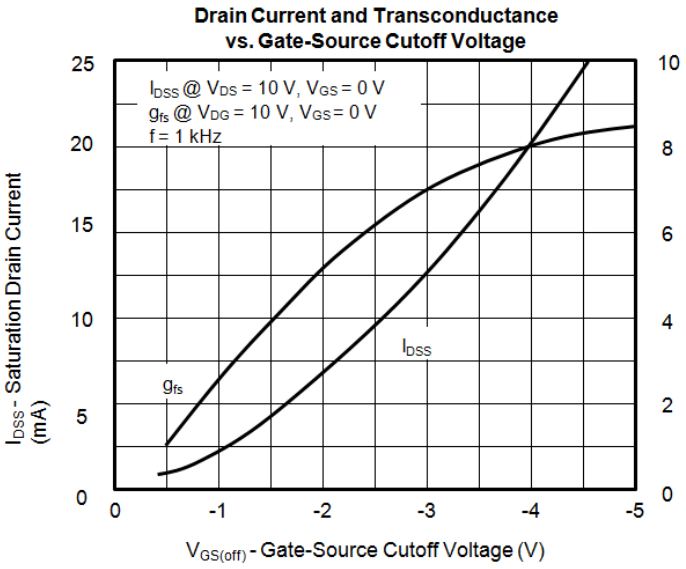


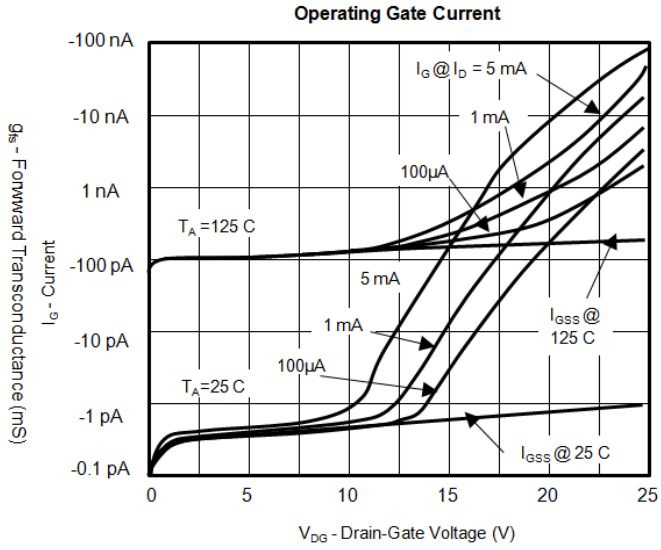
DIMENSIONS IN MILLIMETERS

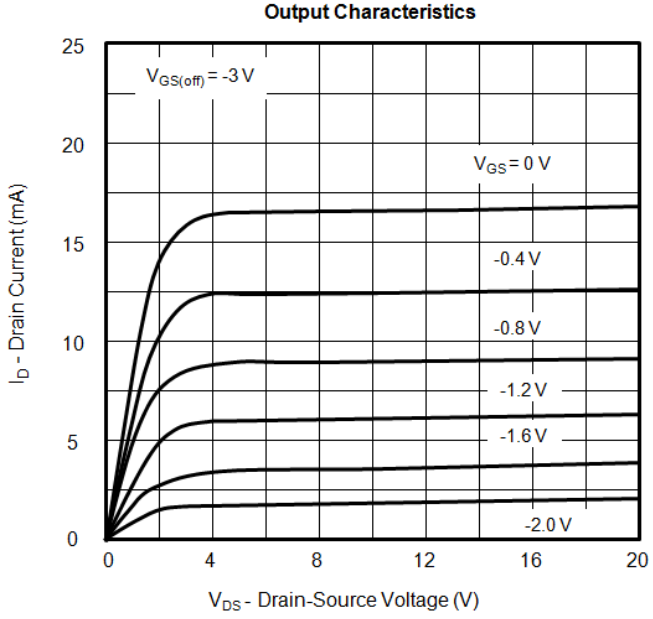
Notes

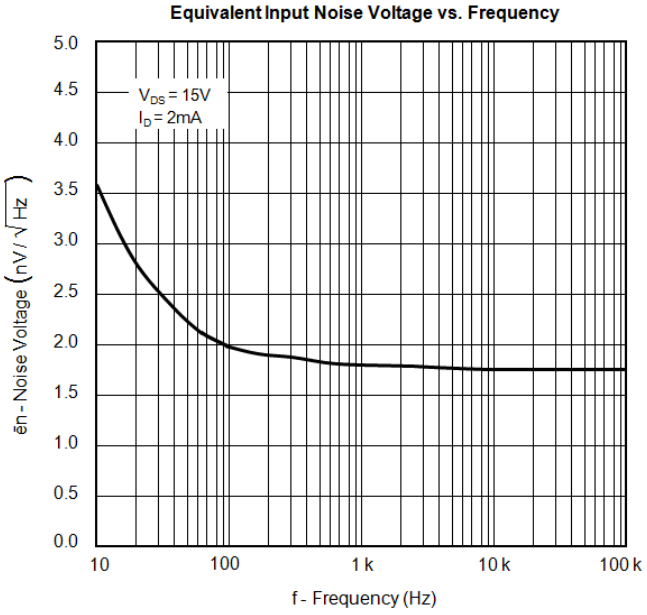
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2ms.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Typical Characteristics

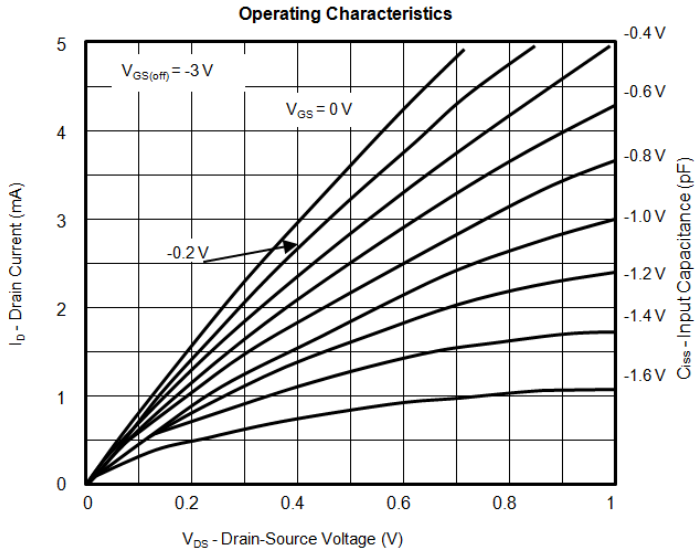


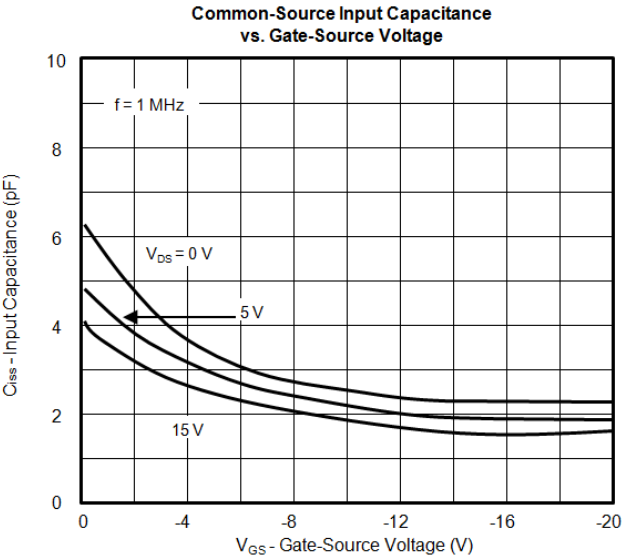


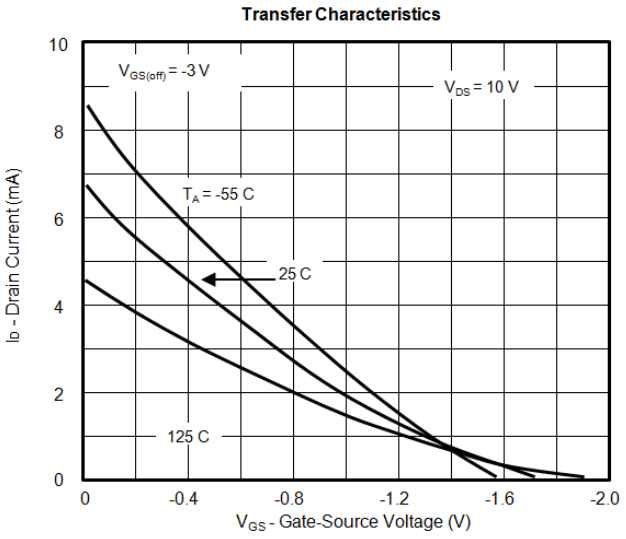


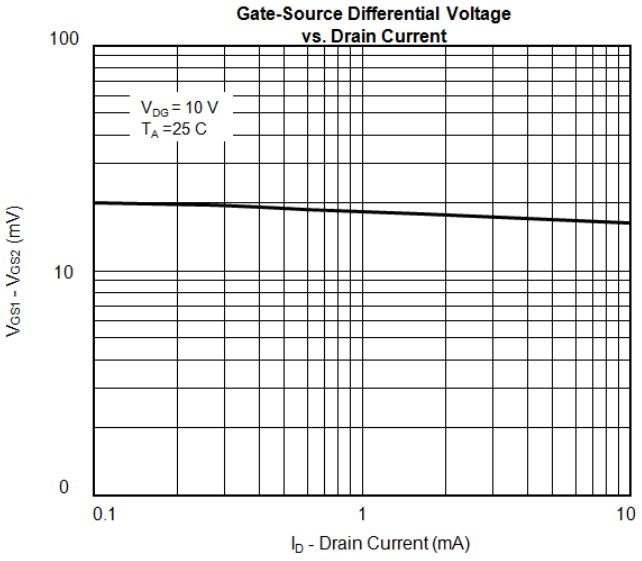


Typical Characteristics (Cont'd)



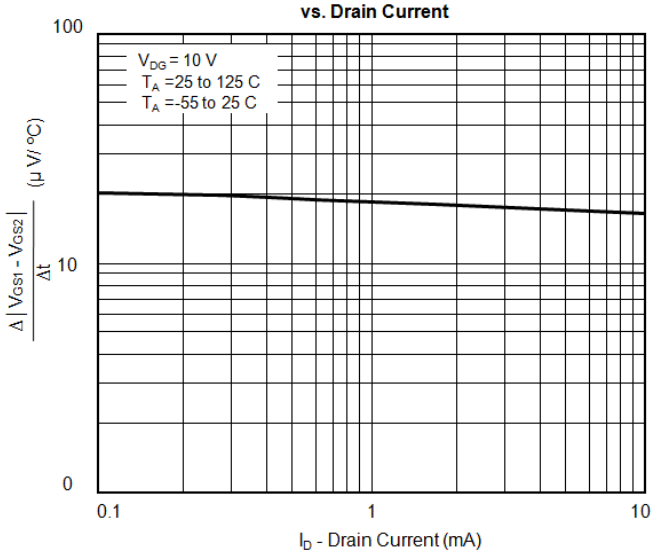




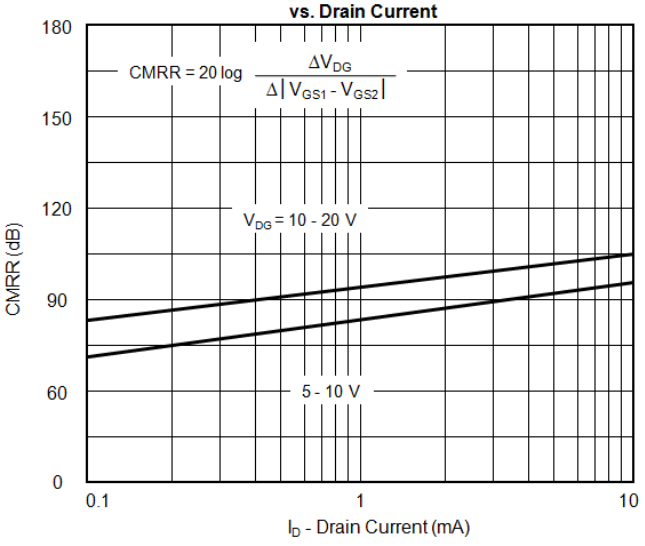


Typical Characteristics (Cont'd)

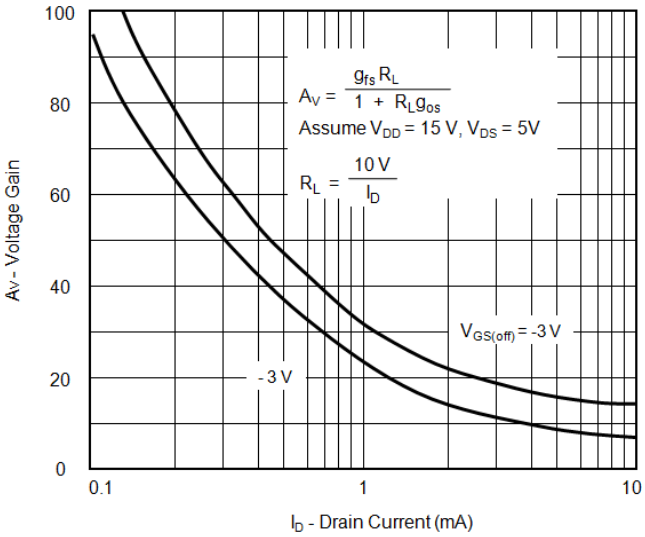
Voltage Differential with Temperature vs. Drain Current



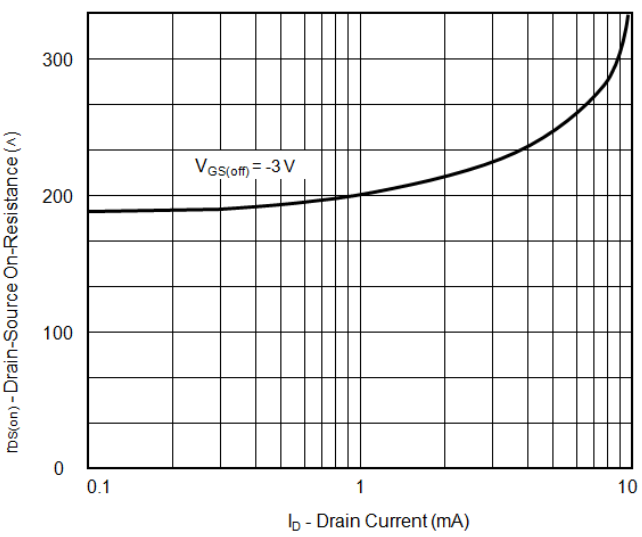
Common Mode Rejection Ration vs. Drain Current



Circuit Voltage Gain vs. Drain Current

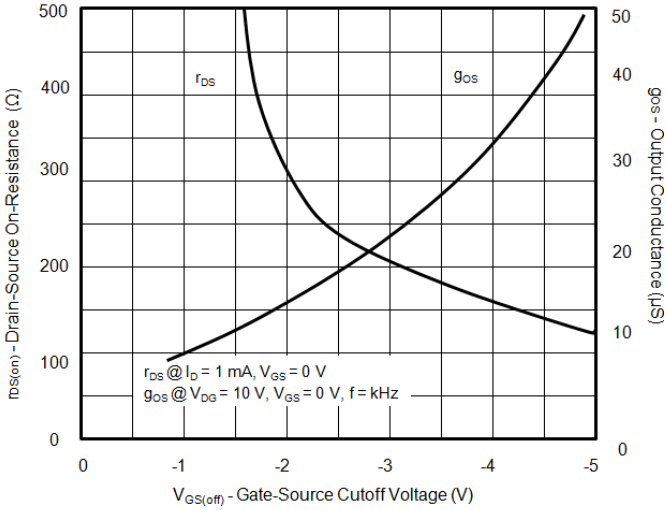


On-Resistance vs. Drain Current

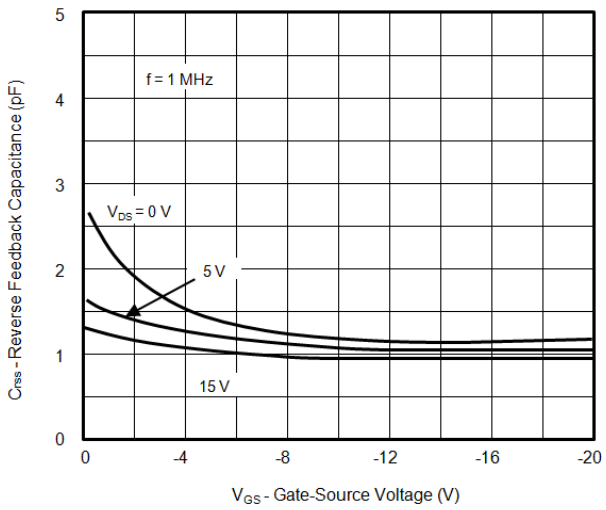


Typical Characteristics (Cont'd)

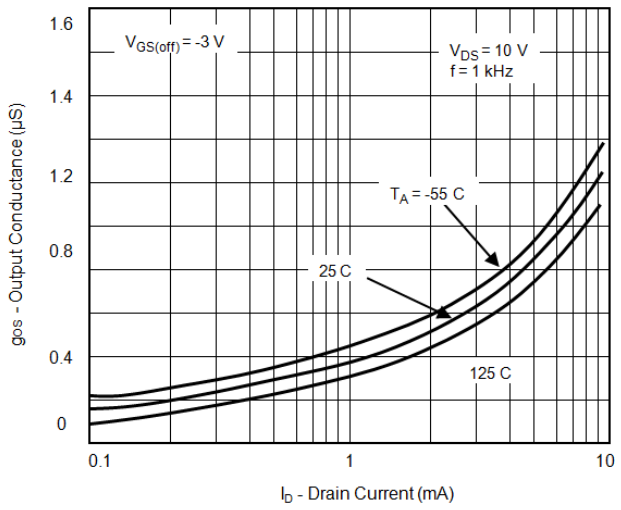
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



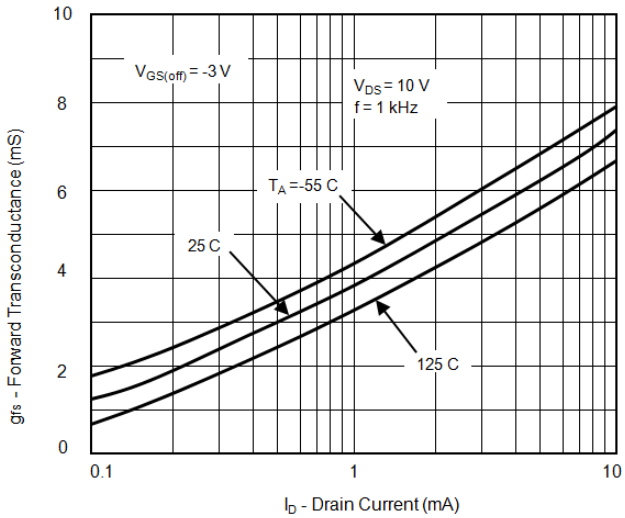
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Output Conductance vs. Drain Current



Common-Source Forward Transconductance vs. Drain Current



LINEAR SYSTEMS

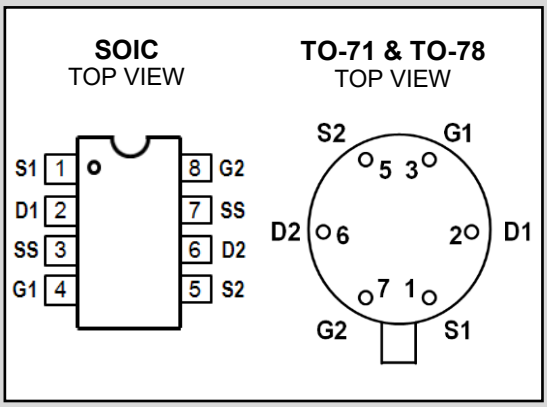
Over Three Decades of Quality Through Innovation

LS840 LS841 LS842

LOW NOISE LOW DRIFT LOW CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW NOISE	e_n=8nV/Hz TYP.
LOW LEAKAGE	I_G=10pA TYP.
LOW DRIFT	I V_{GS1-2}/TI=5µV/ºC max.
LOW OFFSET VOLTAGE	IV_{GS1-2}I=2mV TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55°C to +150°C
Operating Junction Temperature		-55°C to +150°C
Maximum Voltage and Current for Each Transistor[1]		
-V_{GSS}	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation		
Device Dissipation[2] @ Free Air - Total		400mW T_A=+25°C

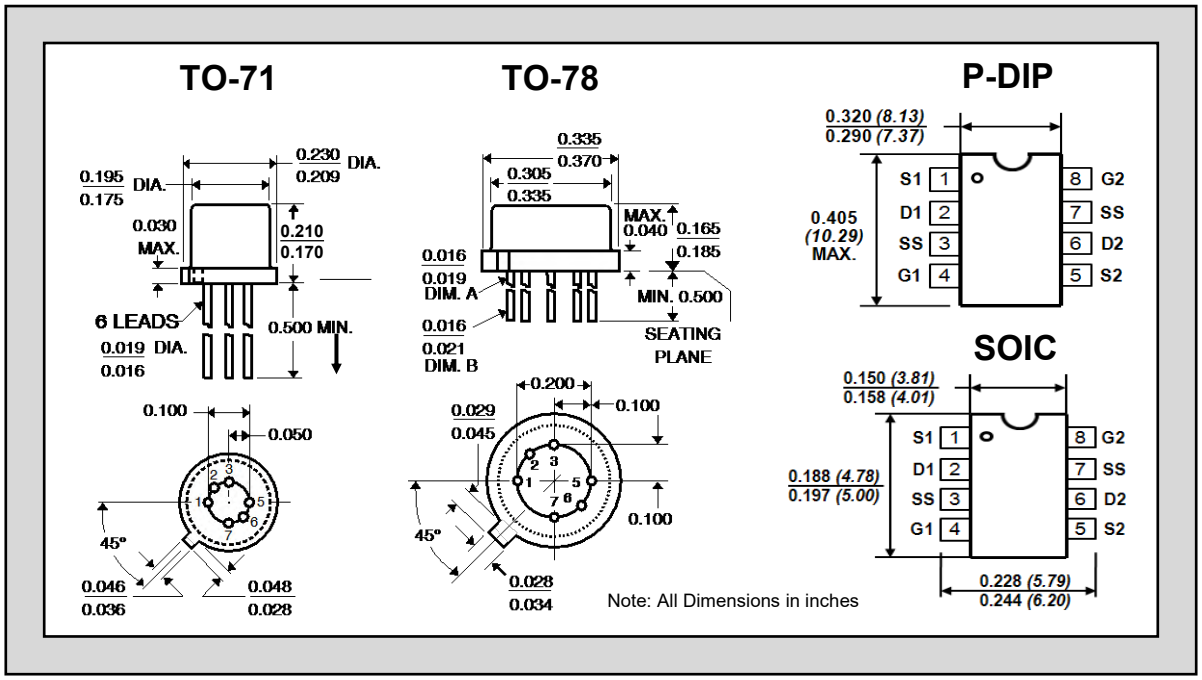


ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS840	LS841	LS842	UNITS	CONDITIONS
I V_{GS1-2} / TI max.	Drift vs. Temperature	5	10	40	µV/ºC	V_{DG} = 20V I_D = 200µA T_A = -55ºC to +125ºC
IV_{GS1-2}I max.	Offset Voltage	5	10	25	mA	V_{DG} = 20V I_D = 200µA

SYMBOL	CHARACTERISTIC[3]	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	V_{DS}= 0 I_D= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±60	--	--	V	I_{GGO}= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	1000		4000	µS	V_{DG}= 20V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Conduction	500		1000	µS	V_{DG}= 20V I_D= 200µA
$\frac{G_{fs1}}{G_{fs2}}$	Transconductance Ratio	0.97		1.0		V_{DG}= 20V I_D= 200µA; Note 4
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DG}= 20V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio	0.95		1.0		
	GATE-SOURCE					
V_{GS}(off)	Pinchoff Voltage	-1	-2	-4.5	V	V_{DS}= 20V I_D= 1nA
V_{GS}	Operating Range	-0.5	--	-4	V	V_{DS}= 20V I_D= 200µA
	GATE CURRENT					
-I_G	Operating	--	10	50	pA	V_{DG}= 20V I_D =200µA
-I_G	High Temperature	--	--	50	nA	V_{DG}= 20V I_D =200µA T_A=+125ºC
-I_G	Reduced VDG	--	5	--	pA	V_{DG}= 10V I_D =200µA
-I_{GSS}	At Full Conduction	--	--	100	pA	V_{DG}= 20V V_{DS} =0

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
	OUTPUT CONDUCTANCE							
G_{OSS}	Full Conduction	--	--	10	µS	V_{DG}= 20V	V_{GS}= 0	
G_{OS}	Operating	--	0.1	1	µS	V_{DG}= 20V	I_D= 200µA	
$\lvert G_{OS\ 1-2} \rvert$	Differential	--	0.01	0.1	µS			
	COMMON MODE REJECTION							
CMRR	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	--	100	--	dB	V_{DS}= 10 to 20V		I_D=200µA
CMRR		--	75	--	dB	V_{DS}= 5 to 10V		I_D=200µA
	NOISE							
NF	Figure	--	--	0.5	dB	V_{DS}= 20V f= 100Hz	V_{GS}= 0 NBW= 6Hz	R_G=10M
e_n	Voltage	--	--	10	nV/Hz	V_{DS}= 20V NBW= 1Hz	I_D= 200µA	f= 1KHz
e_n	Voltage	--	--	15	nV/Hz	V_{DS}= 20V NBW= 1Hz	I_D= 200µA	f= 10Hz
	CAPACITANCE							
C_{ISS}	Input	--	4	10	pF	V_{DS}= 20V	I_D=200µA	
C_{RSS}	Reverse Transfer	--	1.2	5	pF			
C_{DD}	Drain-to-Drain	--	0.1	--	pF	V_{DG}= 20V	I_D= 200µA	



NOTES:

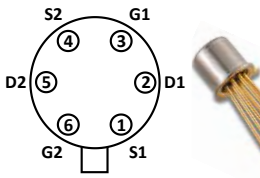
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/ºC above 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.
4. Assumes smaller number in the numerator.

LS843 Series

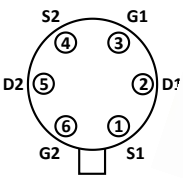
Low Noise, Monolithic Dual N-Channel JFET Amplifier

LOW INPUT CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

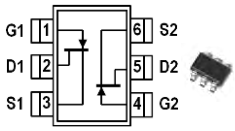
FEATURES		
Ultra-Low Noise	e_n=2.5nV/Hz @1kHz TYP.	
Low Leakage	I_G=15pA TYPs.	
Low Drift	I V_{GS1-2}/TI=5µV/ºC max.	
Ultra-Low Offset Voltage	IV_{GS1-2}I=1mV max.	
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55º to +150°C
Operating Junction Temperature		-55º to +150°C
Maximum Voltage and Current for Each Transistor[1]		
-V_{GSS}	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	50mA
Maximum Power Dissipation[2]		
Device Dissipation[2] @ Free Air - Total		400mW T_A=+25°C



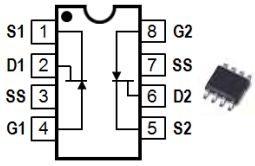
TO-71 6L
Top View



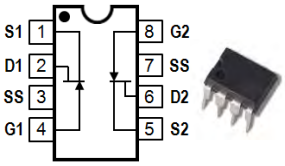
TO-78 6L
Top View



SOT-23 6L
Top View



SOIC-A 8L
Top View



PDIP 8L
Top View

* For equivalent single version, see LSK189

Features

- Low Noise: e_n = 2.5nV/√Hz (typ), *f* = 1kHz, NBW = 1Hz
- Very Low Common Source Input Capacitance of C_{ISS} = 3pF – typ and 8pF- max
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage I_{GSS} and I_G
- High CMRR 102 dB

Benefits

- Tight Differential Voltage Match vs. Current
- Improved Op Amp Speed Settling Time Accuracy
- Minimum Input Error Trimming Error Voltage
- Lower Intermodulation Distortion

Applications

- Wideband Differential Amplifiers
- High Speed Temperature Compensated Single Ended Input Amplifier Amps
- High Speed Comparators
- Impedance Converters
- Sonobouys and Hydrophones
- Acoustic Sensors

Description

The LS843 Series is the industry's lowest input capacitance and low-noise monolithic dual N-Channel JFET. Low input capacitance substantially reduces intermodulation distortion. In addition, these dual JFETs feature tight offset voltage and low drift over temperature range, and are targeted for use in a wide range of precision instrumentation and sensor applications.

The LS843 Series is available in surface mount plastic SOIC 8L, PDIP 8L and SOT-23 6L packages. Additionally, it is offered in thru-hole metal cans; the TO-71 6L and TO-78 6L package.

For an equivalent single N-Channel version refer to the LSK189 datasheet. LS843 Series TO-71 6L and SOIC 8L are fit, form and pin compatible to the same LSK389 product.

The LS843 Series provides an increase in capabilities for a wide range of low-noise applications.

The most significant aspect of the LS843 Series is how it combines a noise level comparable with the LSK389 while having much lower gate-to-drain capacitance, 4pF versus the 25pF. The slightly higher noise of the LS843 Series, versus the LSK389, is not significant in most instances, while the much lower capacitance enables designers to produce simpler, more elegant circuit designs with fewer devices that cost less in production.

Like the Linear Systems LSK389, the LS843 Series features a unique design construction of interleaving both JFETs on the same piece of silicon to provide excellent matching and thermal tracking, as well a low-noise profile having nearly zero popcorn noise.

Electrical Characteristics @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS843	LS844	LS845	UNITS	CONDITIONS
I V_{GS1-2} / TI max.	Drift vs. Temperature	5	10	25	µV/ºC	V_{DG}= 10V I_D= 500µA T_A= -55ºC to +125ºC
IV_{GS1-2}I max.	Offset Voltage	1	5	15	mV	V_{GS}= 10V I_D= 500µA

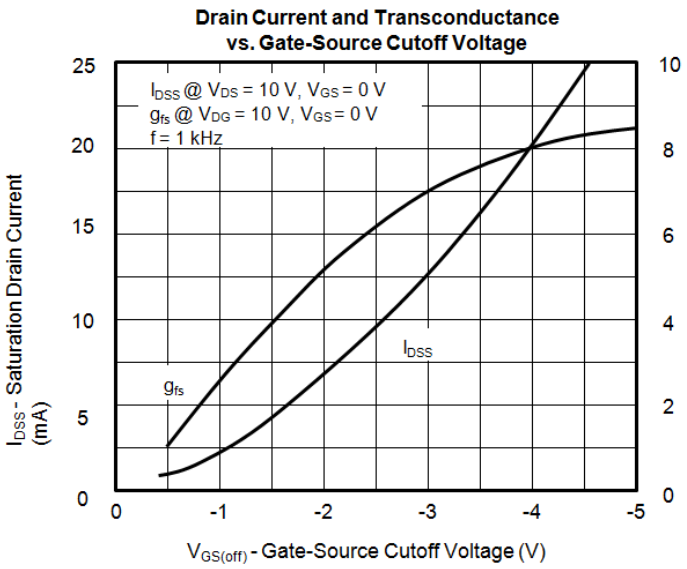
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	V_{DS}= 0 I_D= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±60	--	--	V	I_{GGO}= ±1µA I_D= 0 I_S= 0
G_{fss}	**TRANSCONDUCTANCE** Full Conduction	1500	--	--	µS	V_{DS}= 15V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Conduction	1000	1500	--	µS	V_{DS}= 15V I_D= 500µA
$\lvert G_{fs1-2}/G_{fs1} \rvert$	Mismatch	--	0.6	3	%	
I_{DSS}	**DRAIN CURRENT** Full Conduction	1.5	5	15	mA	V_{DS}= 15V V_{GS}= 0
$\lvert I_{DSS1-2}/I_{DSS} \rvert$	Mismatch at Full Conduction	--	1	5	%	
V_{GS}(off)	**GATE VOLTAGE** Pinchoff Voltage	-1	--	-3.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}	Operating Range	-0.5	--	-3.5	V	V_{DS}= 15V I_D= 500µA
$-I_G$	**GATE CURRENT** Operating	--	15	50	pA	V_{DG}= 15V I_D= 500µA
$-I_G$	High Temperature	--	--	50	nA	V_{DG}= 15V I_D= 500µA T_A=+125ºC
$-I_G$	Reduced VDG	--	5	30	pA	V_{DG}= 3V I_D= 500µA
$-I_{GSS}$	At Full Conduction	--	--	100	pA	V_{GS}= 15V V_{GS}= 0
G_{OSS}	**OUTPUT CONDUCTANCE** Full Conduction	--	--	40	µS	V_{DS}= 15V V_{GS}= 0
G_{OS}	Operating	--	2.0	2.7	µS	V_{DS}= 15V I_D= 200µA
$\lvert G_{OS\ 1-2} \rvert$	Differential	--	0.02	0.2	µS	

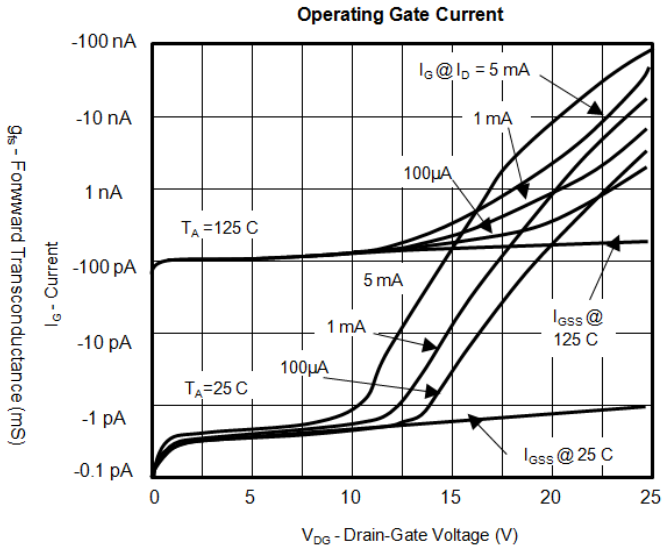
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2} / \Delta V_{DS} \rvert$	90	100	--	dB	V_{DS}= 10 to 20V I_D= 500µA
CMRR		--	85	--	dB	V_{DS}= 5 to 10V I_D= 500µA
NF	**NOISE** Figure	--	--	0.5	dB	V_{DS}= 15V V_{GS}= 0 R_G= 10MΩ f= 100Hz NBW= 6Hz
e_n	Voltage	--	--	7	nV/Hz	V_{DS}= 15V I_D= 500µA f= 1kHz NBW= 1Hz
e_n	Voltage	--	--	11	nV/Hz	V_{DS}= 15V I_D= 500µA f= 10Hz NBW= 1Hz
C_{ISS}	**CAPACITANCE** Input	--	--	8	pF	V_{DS}= 15V I_D= 500µA f= 1mHz
C_{RSS}	Reverse Transfer	--	--	3	pF	
C_{DD}	Drain-to-Drain	--	0.5	--	pF	V_{DD}= 15V I_D= 500µA f= 1mHz

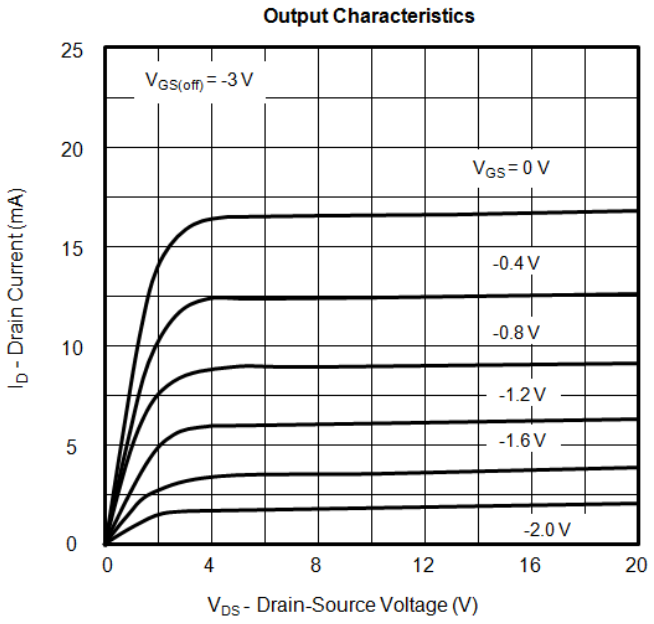
Notes:

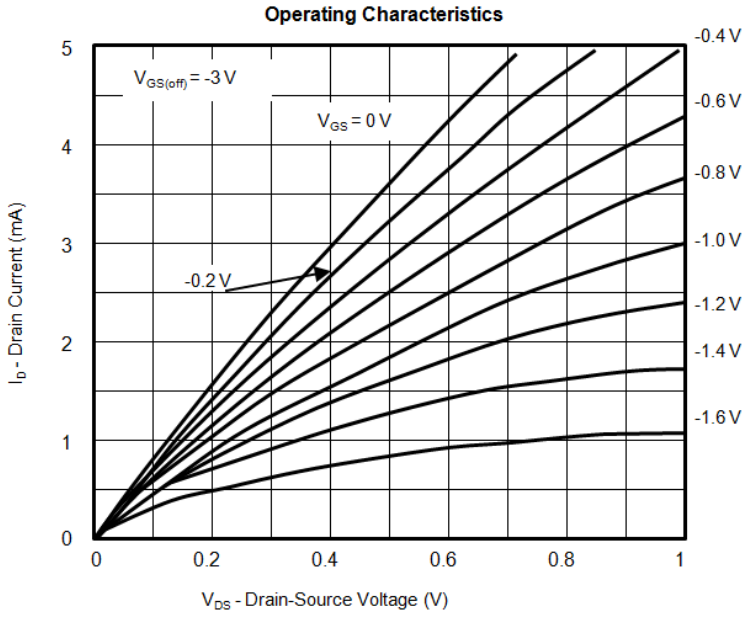
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width ≤2ms.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Typical Characteristics



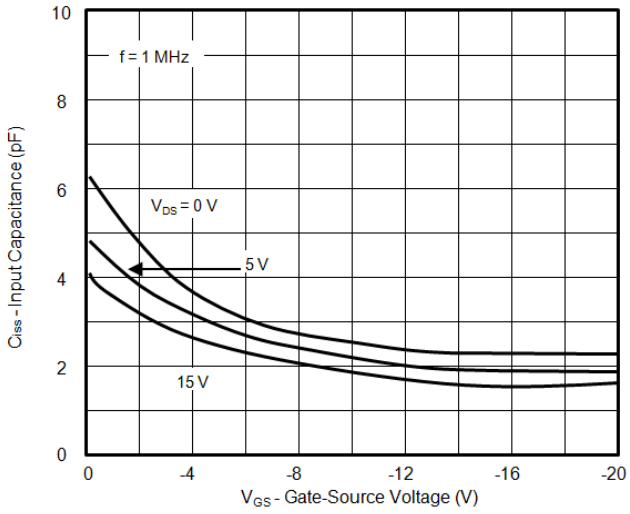




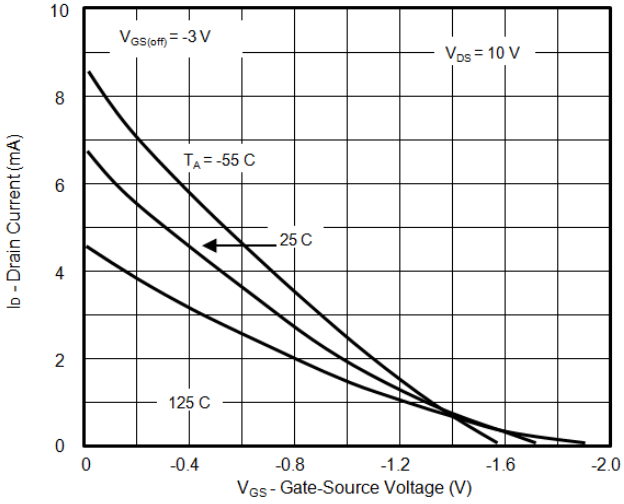


Typical Characteristics Continued

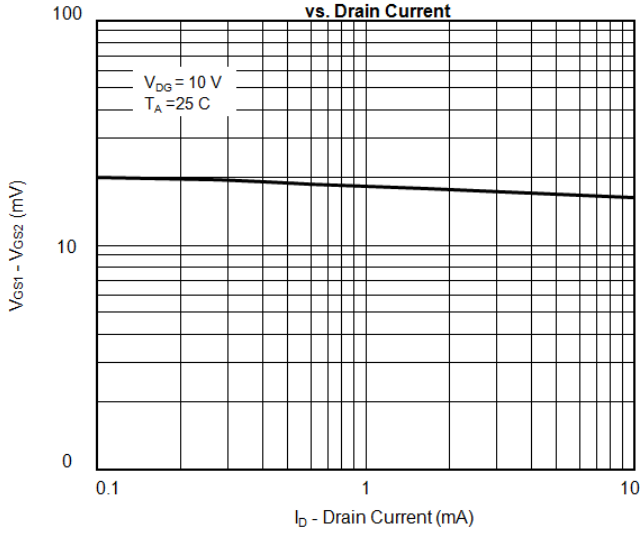
Common-Source Input Capacitance vs. Gate-Source Voltage



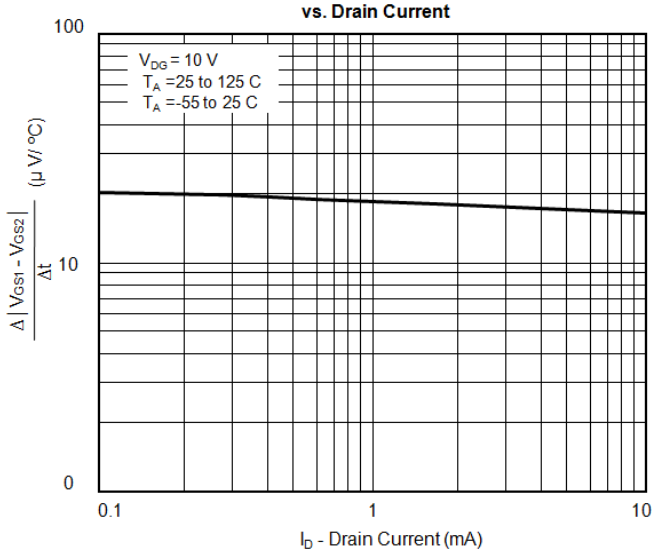
Transfer Characteristics



Gate-Source Differential Voltage vs. Drain Current

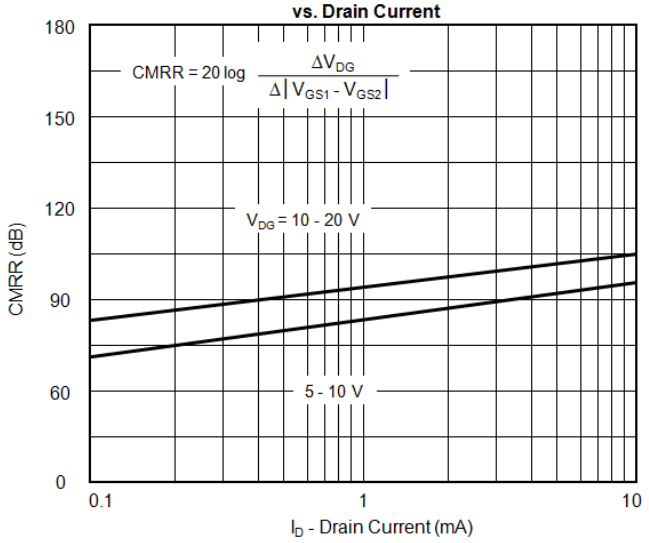


Voltage Differential with Temperature vs. Drain Current

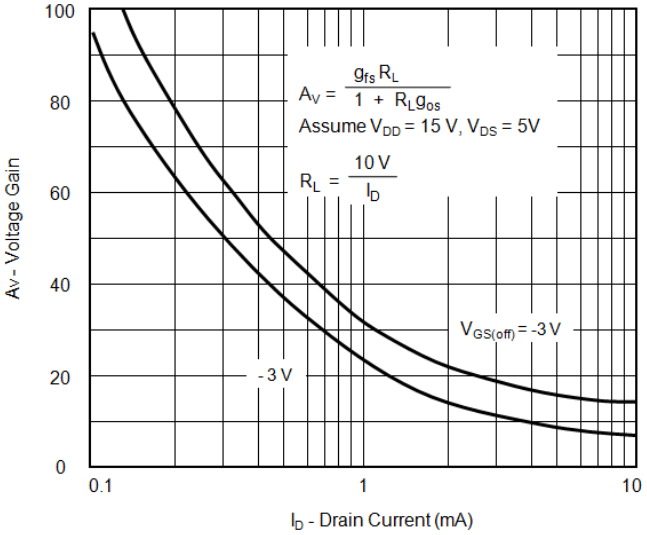


Typical Characteristics Continued

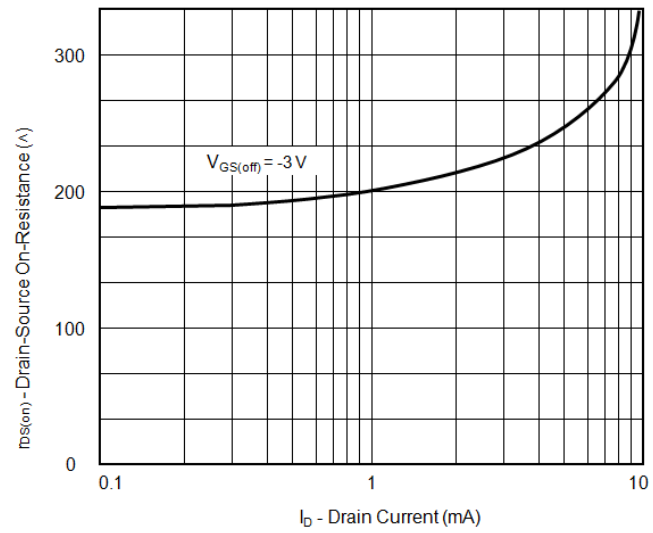
Common Mode Rejection Ration vs. Drain Current



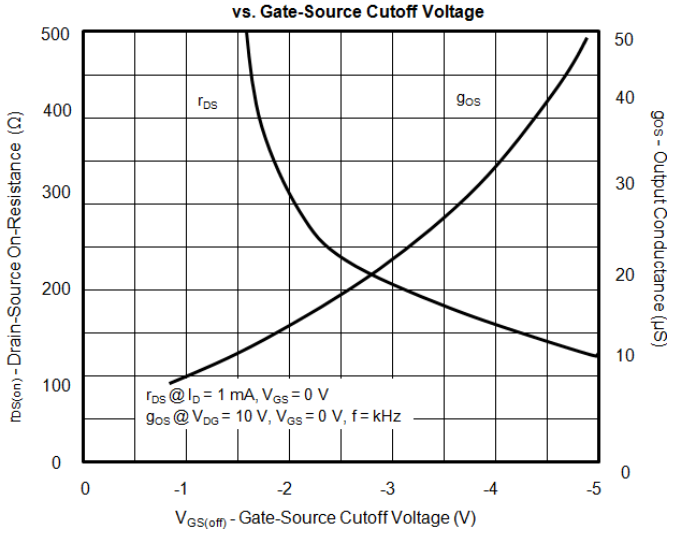
Circuit Voltage Gain vs. Drain Current



On-Resistance vs. Drain Current

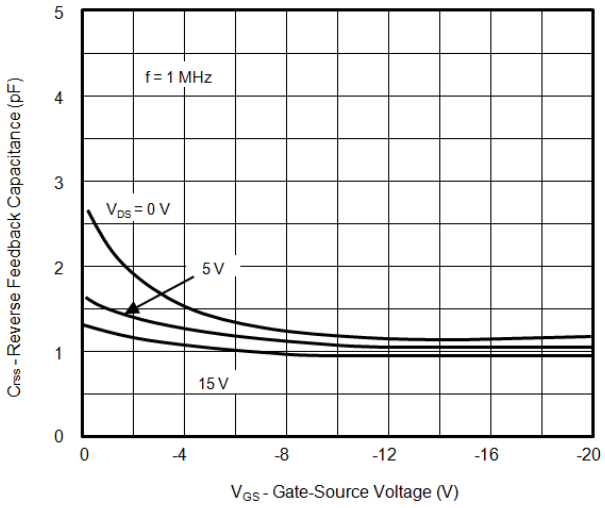


On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage

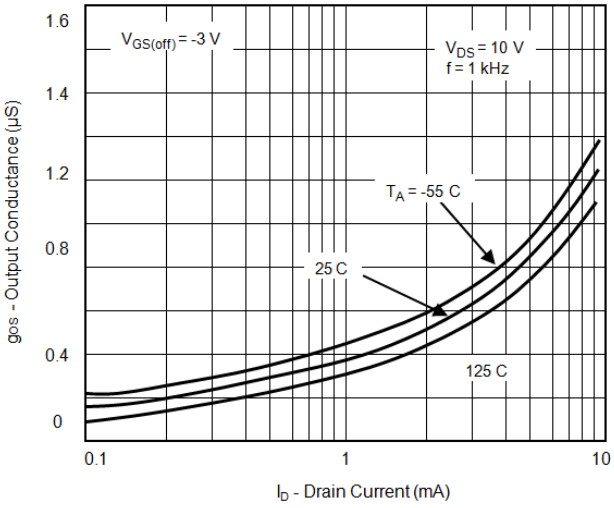


Typical Characteristics Continued

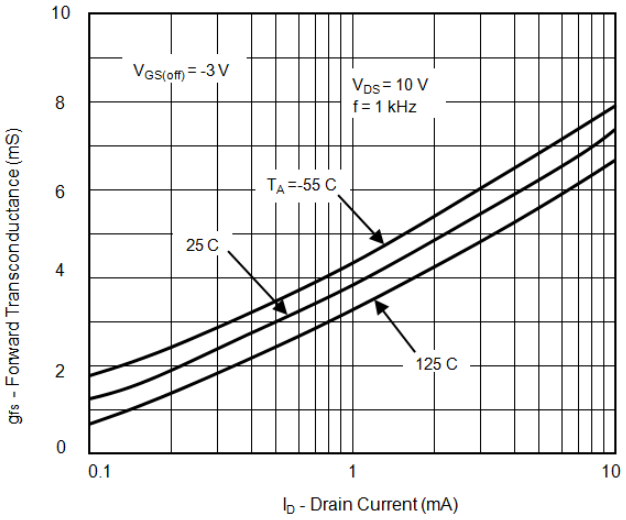
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Output Conductance vs. Drain Current

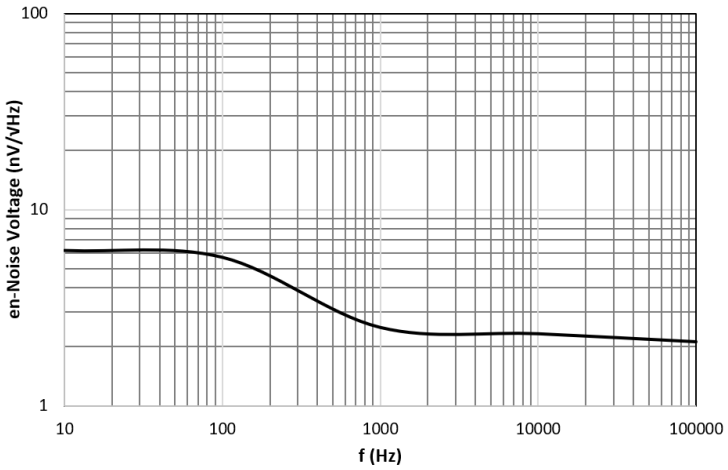


Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

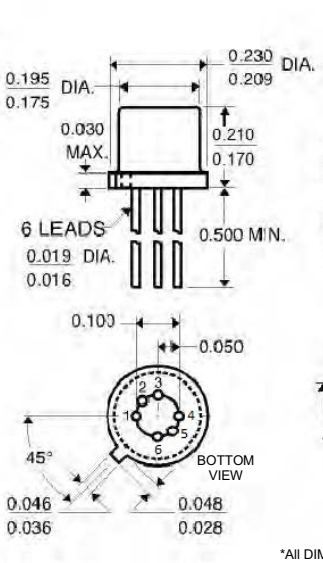
VDS=15V
ID=2mA



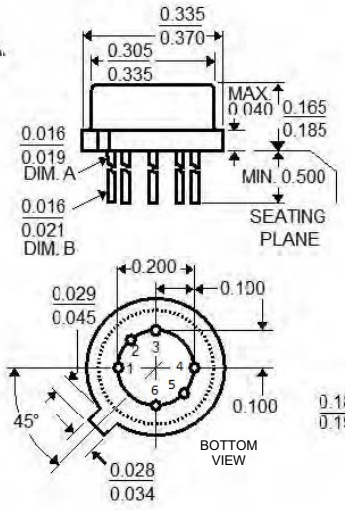
LS843 Series

Package Dimensions:

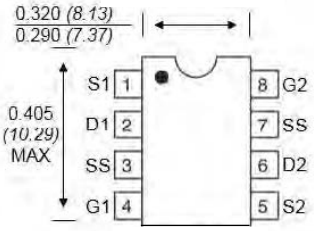
TO-71
6 Lead



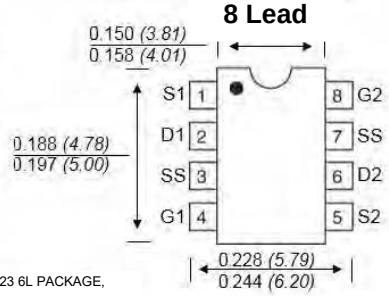
TO-78
6 Lead



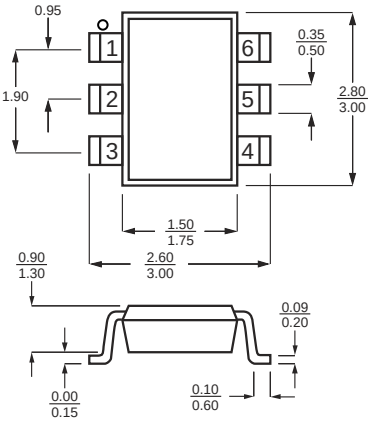
PDIP
8 Lead



SOIC
8 Lead



SOT-23
6 Lead



*All DIMENSIONS IN INCHES EXCEPT FOR THE SOT-23 6L PACKAGE, WHICH IS IN MILLIMETERS

Ordering Information:

Standard Part Call-Out		
LS843 TO-71 6L RoHS	LS844 TO-71 6L RoHS	LS845 TO-71 6L RoHS
LS843 TO-78 6L RoHS	LS844 TO-78 6L RoHS	LS845 TO-78 6L RoHS
LS843 SOT-23 6L RoHS	LS844 SOT-23 6L RoHS	LS845 SOT-23 6L RoHS
LS843 SOIC 8L RoHS	LS844 SOIC 8L RoHS	LS845 SOIC 8L RoHS
LS843 PDIP 8L RoHS	LS844 PDIP 8L RoHS	LS845 PDIP 8L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)		
LS843 TO-71 6L RoHS SELXXXX	LS844 TO-71 6L RoHS SELXXXX	LS845 TO-71 6L RoHS SELXXXX
LS843 TO-78 6L RoHS SELXXXX	LS844 TO-78 6L RoHS SELXXXX	LS845 TO-78 6L RoHS SELXXXX
LS843 SOT-23 6L RoHS SELXXXX	LS844 SOT-23 6L RoHS SELXXXX	LS845 SOT-23 6L RoHS SELXXXX
LS843 SOIC 8L RoHS SELXXXX	LS844 SOIC 8L RoHS SELXXXX	LS845 SOIC 8L RoHS SELXXXX
LS843 PDIP 8L RoHS SELXXXX	LS844 PDIP 8L RoHS SELXXXX	LS845 PDIP 8L RoHS SELXXXX

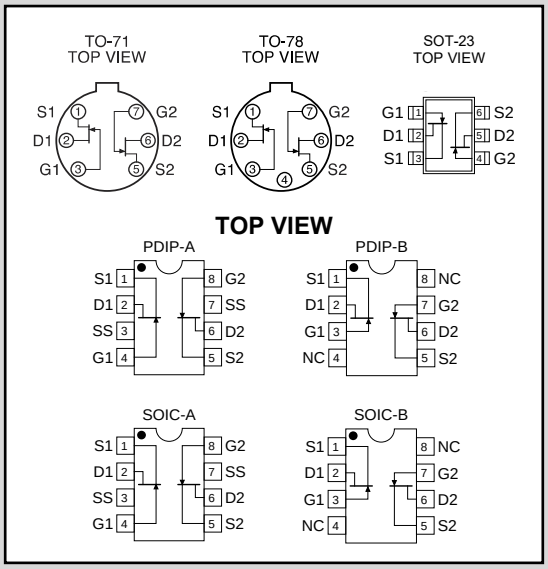
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS5911 LS5912 LS5912C

IMPROVED LOW NOISE WIDEBAND MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
Improved Replacement for SILICONIX, FAIRCHILD, & NATIONAL: 2N5911 & 2N5912	
LOW NOISE (10kHz)	e_n ~ 4nV/√Hz
HIGH TRANSCONDUCTANCE (100MHz)	g_{fs} ≥ 4000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation (Total)[4]	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V



MATCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			10		15		40	mV	V_{DG} = 10V, I_D = 5mA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate to Source Voltage Change with Temperature			20		40		40	µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55 to +125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio		0.95	1	0.95	1	0.95	1		V_{DS} = 10V, V_{GS} = 0V Notes 2, 3
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current			20		20		20	nA	V_{DG} = 10V, I_D = 5mA T_A = +125°C
$\frac{g_{fs1}}{g_{fs2}}$	Forward Transconductance Ratio		0.95	1	0.95	1	0.95	1		V_{DS} = 10V, I_D = 5mA *f* = 1kHz[3]
CMRR	Common Mode Rejection Ratio	85							dB	V_{DG} = 5V to 10V I_D = 5mA

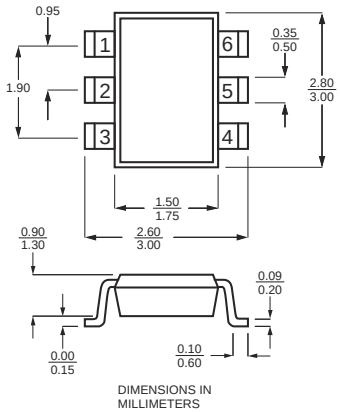
STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown		-25		-25		-25		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-5	-1	-5	-1	-5		V_{DS} = 10V, I_D = 1nA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7								I_G = 1mA, V_{DS} = 0V
V_{GS}	Gate to Source Voltage		-0.3	-4	-0.3	-4	-0.3	-4		V_{DG} = 10V, I_G = 5mA
I_{DSS}	Drain to Source Saturation		7	40	7	40	7	40	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-1		-50		-50		-50	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current	-1		-50		-50		-50		V_{DG} = 10V, I_D = 5mA
IG1G2	Gate to Gate Isolation Current			±1		±1		±1	uA	V_{G1}-V_{G2}=±25VI_D = I_S = 0

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

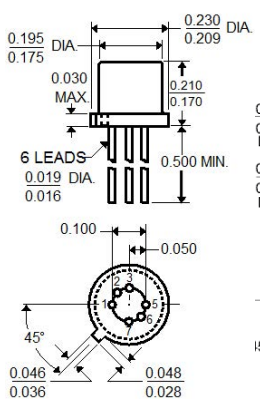
SYM.	CHARACTERISTIC		TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	f = 1kHz		4000	10000	4000	10000	4000	10000	μS	V_{DG} = 10V, I_D = 5mA
		f = 100MHz	7000								
g_{os}	Output Conductance	f = 1kHz			100		100		100		
		f = 100MHz	120								
C_{iss}	Input Capacitance				5		5		5	pF	V_{DG} = 10V, I_D = 5mA f = 1MHz
C_{rss}	Reverse Transfer Capacitance				1.2		1.2		1.2		
NF	Noise Figure				1		1		1	dB	V_{DG} = 10V, I_D = 5mA f = 10kHz, R_G = 100KΩ
e_n	Equivalent Input Noise Voltage	f = 100Hz	7		20		20		20	nV/√Hz	V_{DG} = 10V, I_D = 5mA f = 100Hz
		f = 10kHz	4		10		10		10	nV/√Hz	V_{DG} = 10V, I_D = 5mA f = 10kHz

SOT-23

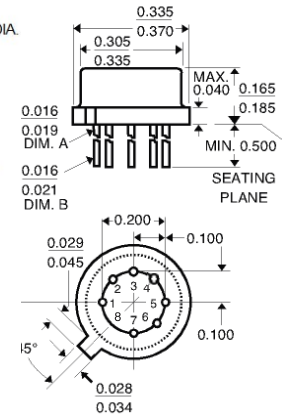


DIMENSIONS IN MILLIMETERS

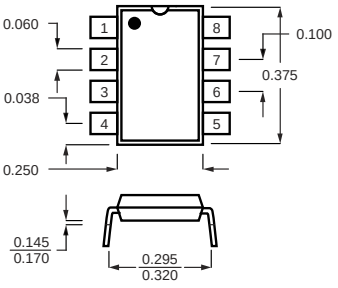
TO-71



TO-78

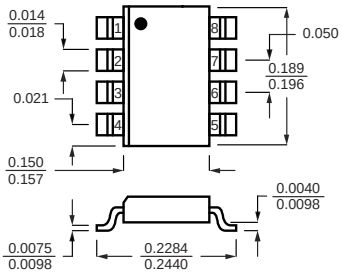


PDIP



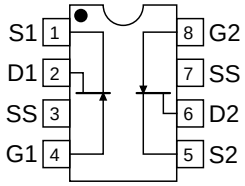
DIMENSIONS IN INCHES

SOIC

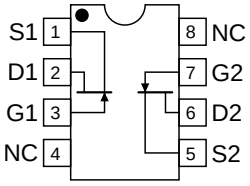


DIMENSIONS IN INCHES

PDIP-A



PDIP-B



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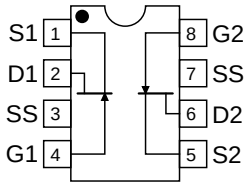
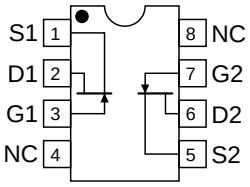


SOIC-B



Please contact the factory regarding the availability of optional packages.

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator.
4. Derate 4mW/°C above 25°C.

LINEAR SYSTEMS

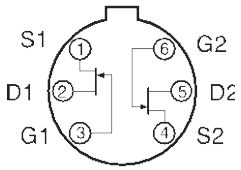
Improved Standard Products®

U/SST440, 441

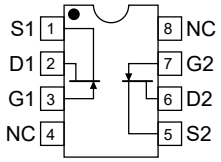
WIDEBAND HIGH GAIN MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
Direct Replacement for SILICONIX U/SST440 & U/SST441	
HIGH CMRR	CMRR ≥ 85dB
LOW GATE LEAKAGE	I_{GSS} ≤ 1pA
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation @ TA = 25°C	
Continuous Power Dissipation (Total)	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V
Gate to Gate	±50V

U SERIES
TO-71
TOP VIEW



SST SERIES
SOIC
TOP VIEW



MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage	U/SST440			10	mV	V_{DG} = 10V, I_D = 5mA
		U/SST441			20		
$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate to Source Cutoff Voltage Change with Temperature			20		µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55 to +125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio[3]			0.98			V_{DS} = 10V, V_{GS} = 0V
$\frac{g_{fs1}}{g_{fs2}}$	Forward Transconductance Ratio[2]			0.97			V_{DS} = 10V, I_D = 5mA, *f* = 1kHz
CMRR	Common Mode Rejection Ratio			85		dB	V_{DG} = 5 to 10V, I_D = 5mA

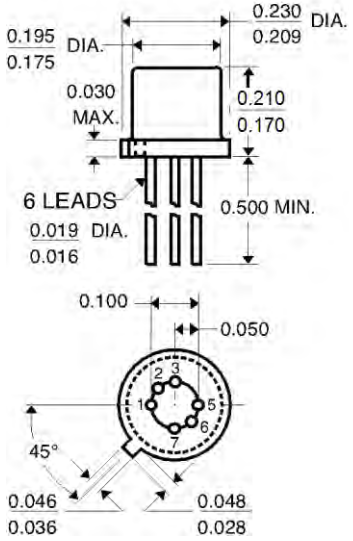
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	-3.5	-6	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Gate to Source Saturation Current[2]	6	15	30	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current		-1	-500	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current		-1	-500		V_{DG} = 10V, I_D = 5mA

ELECTRICAL CHARACTERISTICS CONTINUED @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs}	Forward Transconductance	4.5	6	9	mS	V_{DS} = 10V, I_D = 5mA, *f* = 1kHz
g_{os}	Output Conductance		70	200	µS	
C_{iss}	Input Capacitance		3		pF	V_{DS} = 10V, I_D = 5mA, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance		1			
e_n	Equivalent Input Noise Voltage		4		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 10kHz

TO-71
Six Lead



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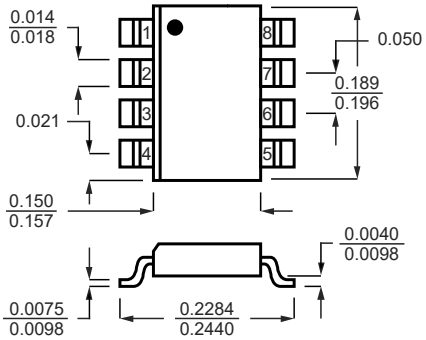


NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator.

LINEAR SYSTEMS

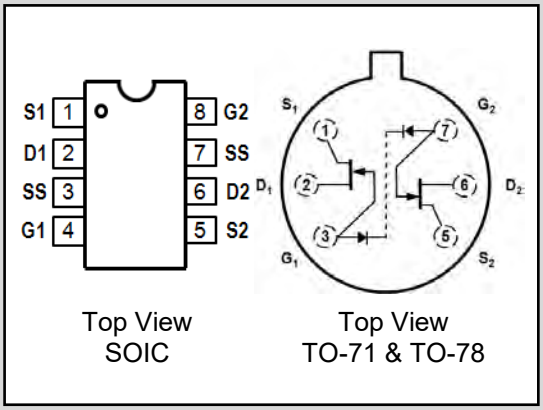
Over 30 Years of Quality Through Innovation

LS830 LS831 LS832 LS833

ULTRA LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW DRIFT	$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ = 5µV/ºC max.
ULTRA LOW NOISE	I_G=80fA TYP.
LOW NOISE	e_n=70nV/√Hz TYP.
LOW CAPACITANCE	C_{ISS}=3pf max.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation @ TA = 25ºC		
Continuous Power Dissipation (Total)		500mW



Top View SOIC

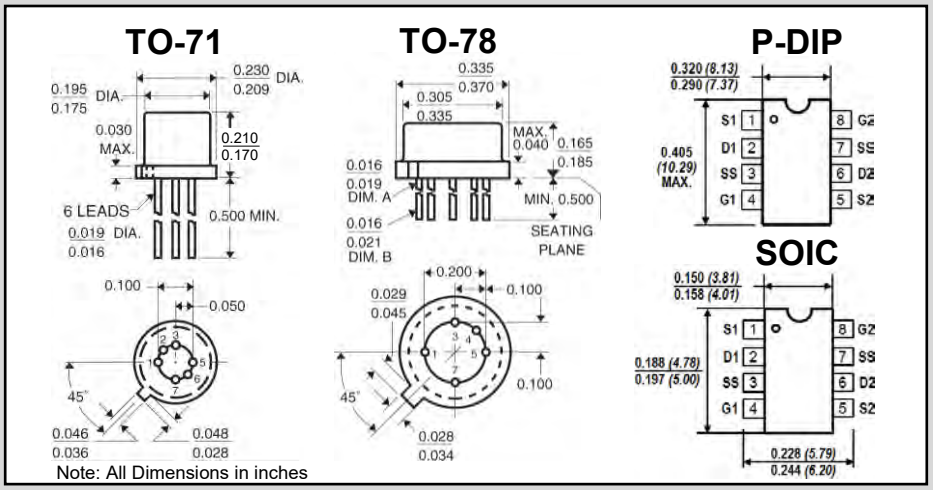
Top View TO-71 & TO-78

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_G= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_G= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
g_{fss}	Full Conduction	70	300	500	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
g_{fs}	Typical Operation	50	100	200	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert g_{fs1-2}/g_{fs} \rvert$	Differential	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	µA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1-2}/I_{DSS} \rvert$	Differential at Full Conduction	--	2	5	%	

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS830	LS831	LS832	LS833	UNITS	CONDITIONS
$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ max.	Drift vs. Temperature	5	10	20	75	µV/ºC	V_{DG} = 10V I_D = 30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	25	25	25	25	mV	V_{DG} = 10V I_D = 30µA
$-I_G$ typical	Operating	0.1	0.1	0.1	0.5	pA	
$-I_G$ typical	High Temperature	0.1	0.1	0.1	0.5	nA	TA= +125ºC
I_{GSS} typical	At Full Conduction	0.2	0.2	0.2	1.0	pA	V_{GS} = 20V, V_{GS} = 0V
I_{GSS} typical	High Temperature	0.5	0.5	0.5	1.0	nA	V_{GS} = 0 V_{GS} = 20V TA= +125ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
	GATE-SOURCE							
$V_{GS}(off)$	Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V	I_D= 1nA	
V_{GS}	Operating Range	--	--	-4	V	V_{DG}= 10V	I_D= 30µA	
	GATE CURRENT							
I_{GGO}	Gate-to-Gate Leakage	--	1	--	pA	V_{GG}= ±20V	$I_D = I_S$ = 0A	
	OUTPUT CONDUCTANCE							
g_{OSS}	Full Conduction	--	--	5	µS	V_{DG}= 10V	V_{GS}= 0	
g_{OS}	Operating	--	--	0.5	µS	V_{DG}= 10V	I_D= 30µA	
$\lvert g_{OS\ 1\text{-}2} \rvert$	Differential	--	--	0.1	µS			
	COMMON MODE REJECTION							
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V		I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V		I_D=30µA
	NOISE							
NF	Figure	--	--	1	dB	V_{DS}= 10V f= 100Hz	V_{GS}= 0 NBW= 6Hz	R_G=10MΩ
e_n	Voltage	--	20	70	nV/√Hz	V_{DG}= 10V NBW= 1Hz	I_D= 30µA	f= 10Hz
	CAPACITANCE							
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 10V	I_D= 30µA	



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired

LINEAR SYSTEMS

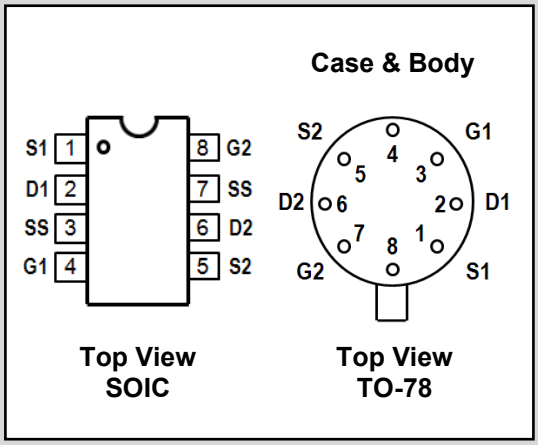
Improved Standard Products®

LS5905 LS5906 LS5907 LS5908 LS5909

LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ =5μV/°C max.
ULTRA LOW LEAKAGE	I_G=150fA TYP.
LOW PINCHOFF	V_P=2V TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor[1]		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10μA
Maximum Power Dissipation		
Device Dissipation @ TA=25ºC - Total		500mW[2]

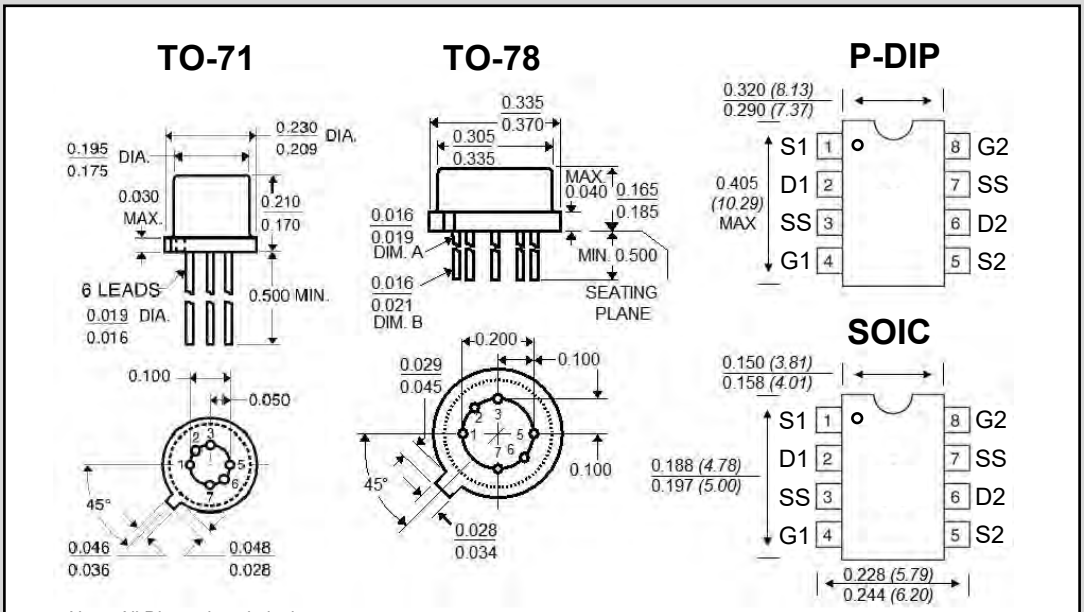


ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS5906	LS5907	LS5908	LS5909	LS5905	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature	5	10	20	40	40	μV/ºC	V_{DG} = 10V, I_D=30μA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage	5	5	10	15	15	mV	V_{DG} =10V I_D=30μA
$-I_G$ Max	Operating	1	1	1	1	3	pA	
$-I_G$ Max	High Temperature	1	1	1	1	3	nA	T_A=+125 ºC
$-I_{GSS}$ Max	Gate Reverse Current	2	2	2	2	5	pA	V_{DS}=0V V_{GS}=-20V
$-I_{GSS}$ Max	Gate Reverse Current	5	5	5	5	10	nA	T_A=+125 ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_D= -1μA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_{GG}= ±1μA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	70	300	500	μS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	50	100	200	μS	V_{DG}= 10V I_D= 30μA f = 1kHz
$\lvert G_{fs1}/G_{fs2}$[3]$\rvert$	Transconductance Ratio	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	μA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1}/I_{DSS2}$[3]$\rvert$	Drain Current Ratio	--	2	5	%	
	GATE VOLTAGE					
V_{GS}(off)	Gate-Source Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V I_D= 1nA
V_{GS}	Operating Range	--	--	-4	V	V_{DS}= 10V I_D= 30μA
	GATE CURRENT					
I_{GGO}	Gate-to-Gate Leakage	--	±1	--	pA	V_{GG}= 20V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{oss}	Full Conduction	--	--	5	µS	V_{DG}= 10V V_{GS}= 0
g_{os}	Operating	--	0.1	--	µS	V_{DG}= 10V I_D= 30µA
$\lvert g_{os1-2} \rvert$	Differential	--	0.01	0.2	µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1	dB	V_{DS}= 10V V_{GS}= 0 R_G=10MΩ f= 100Hz NBW=6Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DS}= 10V I_D= 30µA f= 10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 20V I_D= 30µA f= 1MHz



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 4mWºC above 25ºC
3. Assume smaller value in the numerator.

LINEAR SYSTEMS

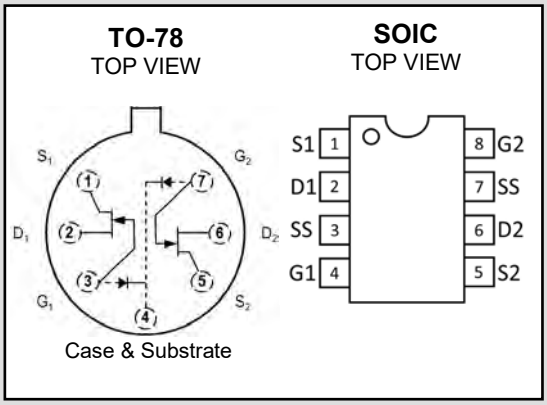
Improved Standard Products®

U421, U422, U423, U424, U425, U426

LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
HIGH INPUT IMPEDANCE	I_G=0.25pA MAX
HIGH GAIN	gfs=120µS MIN
LOW POWER OPERATION	$V_{GS(off)}$=2V MAX

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation		
Total Device Dissipation TA = 25ºC		500[2] mW

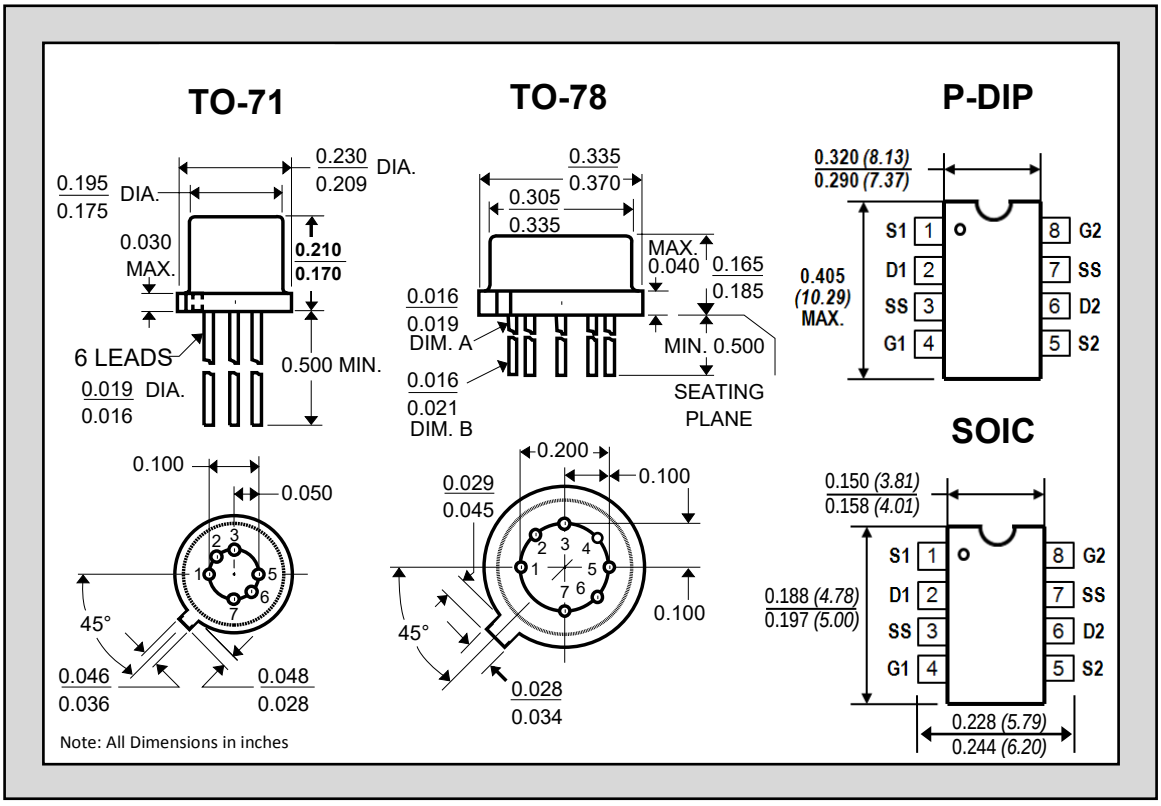


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC[3]		U421	U422	U423	U424	U425	U426	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature		10	25	40	10	25	40	µV/ºC	V_{DG} = 10V I_D = 30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage		10	15	25	10	15	25	mV	V_{DG} =10V I_D = 30µA
	GATE VOLTAGE									
$V_{GS(off)}$	Pinchoff Voltage	Max	-2.0	-2.0	-2.0	-3.0	-3.0	-3.0	V	V_{DS}=10V I_D=1nA
		Min	-0.4	-0.4	-0.4	-0.4	-0.4	-0.4		
V_{GS}	Operating Range	Max	-1.8	-1.8	-1.8	-2.9	-2.9	-2.9	V	V_{DS}=10V I_D=30µA
I_GTYP.	Operating		-.25	-.25	-.25	-.500	-.500	-.500	pA	V_{DS}=10V I_D=30µA
I_GTYP.	High Temperature		-250	-250	-250	-500	-500	-500	pA	T_A=+125ºC
I_{GSS}TYP.	Gate Reverse Current		-1.0	-1.0	-1.0	-3.0	-3.0	-3.0	pA	V_{DS}=0V V_{GS}=-20V
I_{GSS}TYP.	Gate Reverse Current		1.0	1.0	1.0	3.0	3.0	3.0	nA	T_A=+125ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0V I_G= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_{G1G2}= ±1µA I_D= 0A I_S= 0A
	TRANSCONDUCTANCE					
gfs	Full Conduction	300	--	1500	µS	V_{DS}= 10V V_{GS}= 0 f = 1kHz
gfs	Typical Operation	120	200	350	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
	DRAIN CURRENT	60	--	1000	µA	U421-3 V_{DS}= 10V V_{GS}= 0
I_{DSS}	Full Conduction	60	--	1800	µA	U424-6

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{os}	Full Conduction	--	--	10	µS	V_{DS}= 10V V_{GS}= 0
g_{os}	Operating	--	0.1	3.0	µS	V_{DG}= 10V I_D= 30µA
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V I_D=30µA
CMRR	-20 log $\lvert V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1.0	dB	V_{DG}= 10V, I_D= 30µA, R_G=10MΩ f= 10Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DG}= 10V I_D= 30µA f= 10Hz
			10			V_{DG}= 10V I_D= 30µA f= 1kHz
	CAPACITANCE					
C_{ISS}	Input	--	--	3.0	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/ºC above 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

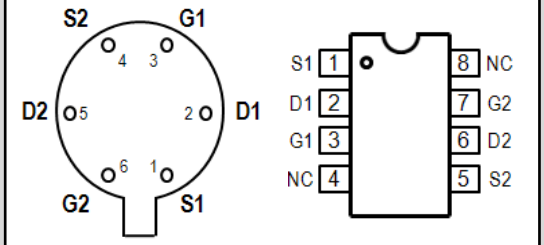
Improved Standard Products®

SST/U401 – SST/U406

LOW NOISE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert V_{GS1-2}/T \rvert$ = 10µV/ºC TYP.
LOW NOISE	e_n=6nV/Hz@10Hz TYP.
LOW PINCHOFF	V_P=2.5V MAX.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation per side NOTE 2		
Device Dissipation TA = 25°C		300mW



TO-71 Top View

SOIC Top View

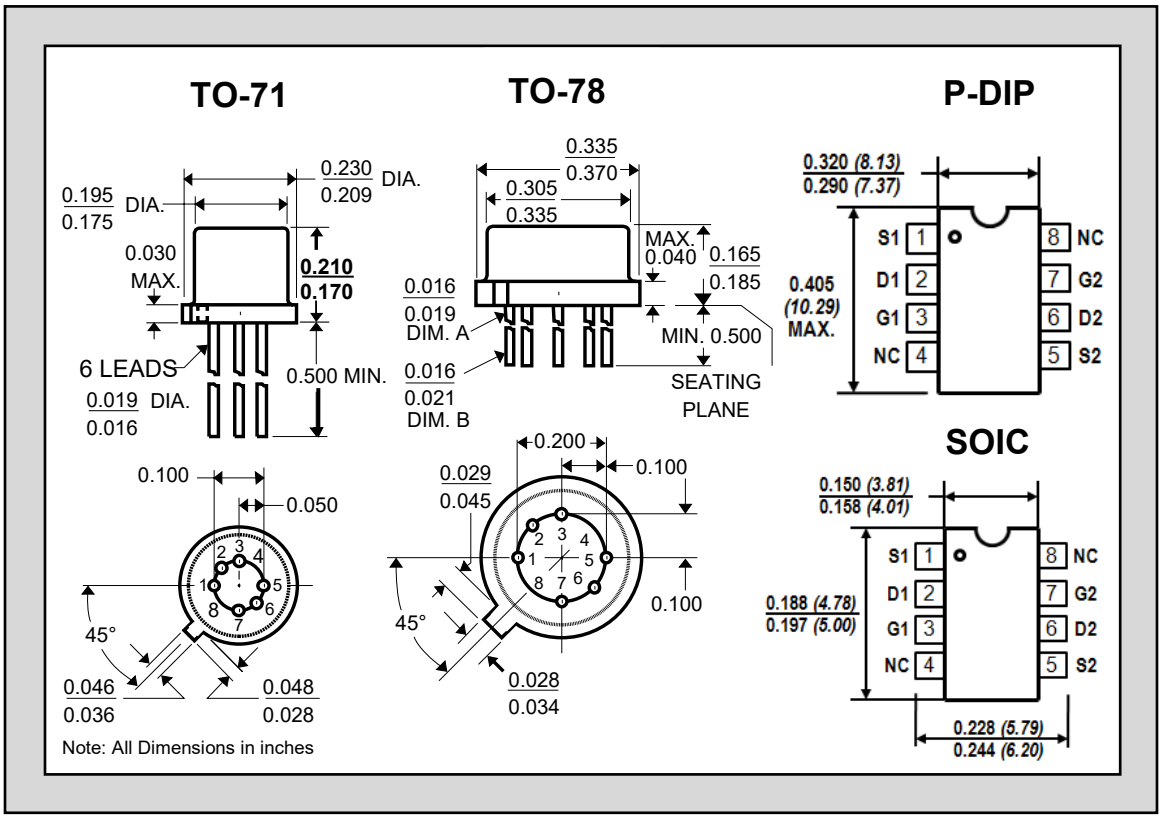
MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	U401	U402	U403	U404	U405	U406	UNITS	CONDITIONS
$\lvert V_{GS1-2}/T \rvert$ max.	Drift vs. Temperature	10	10	25	25	40	80	µV/ºC	V_{DG} = 10V, I_D = 200µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	5	10	10	15	20	40	mV	V_{DG} = 10V, I_D = 200µA

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted) NOTE 3

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-50	-60	--	V	V_{DS}= 0 I_D= 1nA
BV_{G1G2}	Gate-to-Gate Breakdown	±50	--	--	V	I_G= ±1µA I_D= 0, I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	2000	--	7000	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	1000	--	2000	µS	V_{DG}= 15V I_D= 200µA f = 1kHz
$\lvert G_{fs1}/G_{fs2} \rvert$	Mismatch	0.97	--	1.0		
I_{DSS}	Saturation Drain Current	0.5	--	10	mA	V_{DG}= 10V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Current Ratio	0.9	0.98	1.0		
	GATE VOLTAGE					
V_{GS}(off) or V_P	Pinchoff Voltage	-0.5	--	-2.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}	Operating Range	--	--	-2.3	V	V_{DS}= 15V I_D= 200µA
	GATE CURRENT					
I_G	Operating	--	-4	-15	pA	V_{DG}= 15V I_D= 200µA
I_G	High Temperature	--	--	-10	nA	T_A=+125ºC
I_{GSS}	Gate Reverse Current	--	--	-100	pA	V_{GS}=-30v, V_{DS}= 0V
I_{G1G2}	Gate to Gate Isolation Current	--	--	±1.0	µA	V_{G1}-V_{G2}= ±50V, I_D= IS= 0

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
G_{OSS}	Full Conduction	--	--	40	µS	V_{DS}= 10V, V_{GS}= 0V, f = 1kHz
G_{OS}	Operating	--	2	2.7	µS	V_{DS}= 15V, I_D= 200µA, f = 1kHz
	COMMON MODE REJECTION					V_{DG1}= 10V
CMRR	-20 log [(V_{GS1}-V_{GS2})/ΔV_{DG1-2}]	95	--	--	dB	V_{DG2}= 20V I_{D1}= I_{D2}=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 15V V_{GS}= 0 R_G=10M f= 100Hz NBW= 6Hz
e_n	Voltage	--	6	20	nV/Hz	V_{DS}= 15V I_D= 200µA f= 10Hz NBW= 1Hz
	CAPACITANCE					
C_{ISS}	Input	--	4	8	pF	V_{DS}= 15V I_D= 200µA f= 1MHz
C_{RSS}	Reverse Transfer	--	1.5	3	pF	



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 2.4mW/ºC when TA is greater than 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

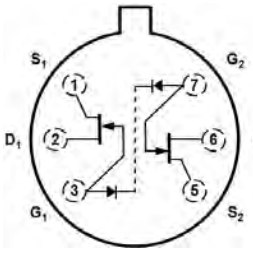
Improved Standard Products®

LS3954A LS3954 LS3955 LS3956 LS3958

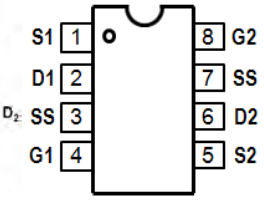
LOW NOISE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ =5µV/°C max.
LOW LEAKAGE	I_G=20pA TYP.
LOW NOISE	e_n=10Nv/√Hz TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor[1]		
$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$-I_{G(f)}$	Gate Forward Current	50mV
Maximum Power Dissipation		
Device Dissipation @ Free Air - Total		400mW @ 25ºC[2]



Top View
TO-71 & TO-78



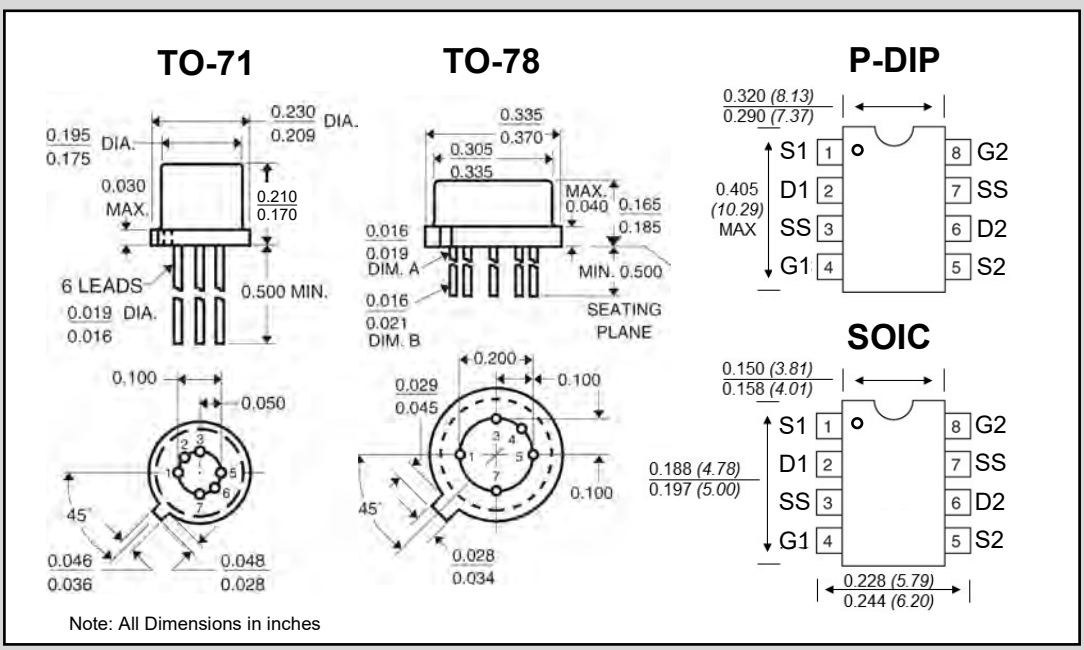
Top View
SOIC

ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS3954A	LS3954	LS3955	LS3956	LS3958	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature	5	10	25	50	100	µV/ºC	V_{DG} = 20V, I_D=200µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage	5	5	10	15	25	mV	V_{DG} =20V, I_D=200µA

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
BV_{GSS}	Breakdown Voltage	60	--	--	V	V_{DS}= 0	I_G= 1µA	
BV_{GGO}	Gate-to-Gate Breakdown	60	--	--	V	I_{GG}= ±1µA	I_D= 0	I_S= 0
	TRANSCONDUCTANCE							
g_{fss}	Full Conduction	1000	2000	4000	µS	V_{DG}= 20V	V_{GS}= 0	f = 1kHz
g_{fs}	Typical Operation	500	700	1250	µS	V_{DG}= 20V	I_D= 200µA	
$\lvert g_{fs1-2}/g_{fs}\rvert$	Differential	--	±0.6	±3	%			
	DRAIN CURRENT							
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DS}= 20V	V_{GS}= 0	
$\lvert I_{DSS1-2}/I_{DSS}\rvert$	Differential	--	±1	±5	%			
	GATE VOLTAGE							
V_{GS}(off)	Pinchoff Voltage	-1	-2	-4.5	V	V_{DS}= 20V	I_D= 1nA	
V_{GS}	Operating Range	-0.5	--	-4	V	V_{DS}= 20V	I_D= 200µA	
	GATE CURRENT							
$-I_G$	Operating	--	20	50	pA	V_{DG}= 20V	I_D= 200µA	
$-I_G$	High Temperature	--	--	50	nA	V_{DG}= 20V	I_D= 200µA	T_A=+125 ºC
$-I_G$	Reduced V_{DG}	--	5	--	pA	V_{DG}= 10V	I_D= 200µA	
$-I_{GSS}$	At Full Conduction	--	--	100	pA	V_{DG}= 20V	V_{DS}= 0	

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{oss}	Full Conduction	--	--	35	µS	V_{DG}= 20V V_{GS}= 0
g_{os}	Operating	--	0.5	1	µS	V_{DG}= 20V I_D= 200µA
$\lvert g_{os1-2} \rvert$	Differential	--	0.05		µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	100	--	dB	ΔV_{DS}= 10 to 20V I_D=200µA
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	75	--	dB	ΔV_{DS}= 5 to 10V I_D=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 20V V_{GS}= 0 R_G=10MΩ f= 100Hz NBW=6Hz
e_n	Voltage	--	--	15	nV/√Hz	V_{DS}= 20V I_D= 200µA f= 10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	6	pF	V_{DS}= 20V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	2	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	V_{DG}= 20V I_D= 200µA



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 4mWºC above 25ºC

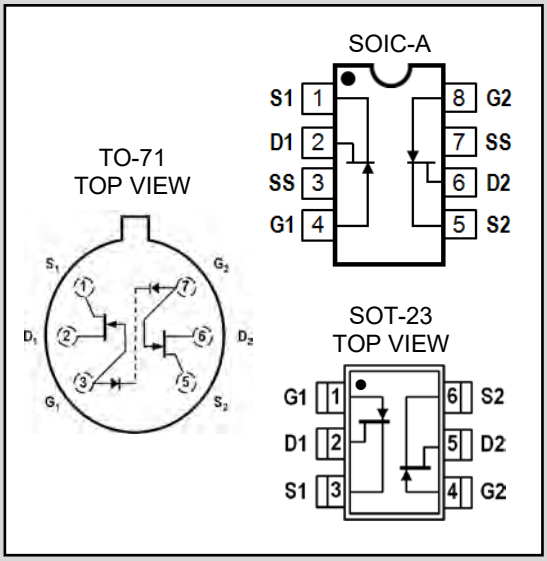
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSK589

LOW NOISE, LOW CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE	e_n = 4.0 nV/√Hz
LOW INPUT CAPACITANCE	Ciss = 5pF
HIGH TRANSCONDUCTANCE	Gfs ≥ 4000µS



ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side [4]	250mW
Power Dissipation, total [5]	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 50mA
Maximum Voltages	
Gate to Source	V_{GSO} = 25V
Gate to Drain	V_{GDO} = 25V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

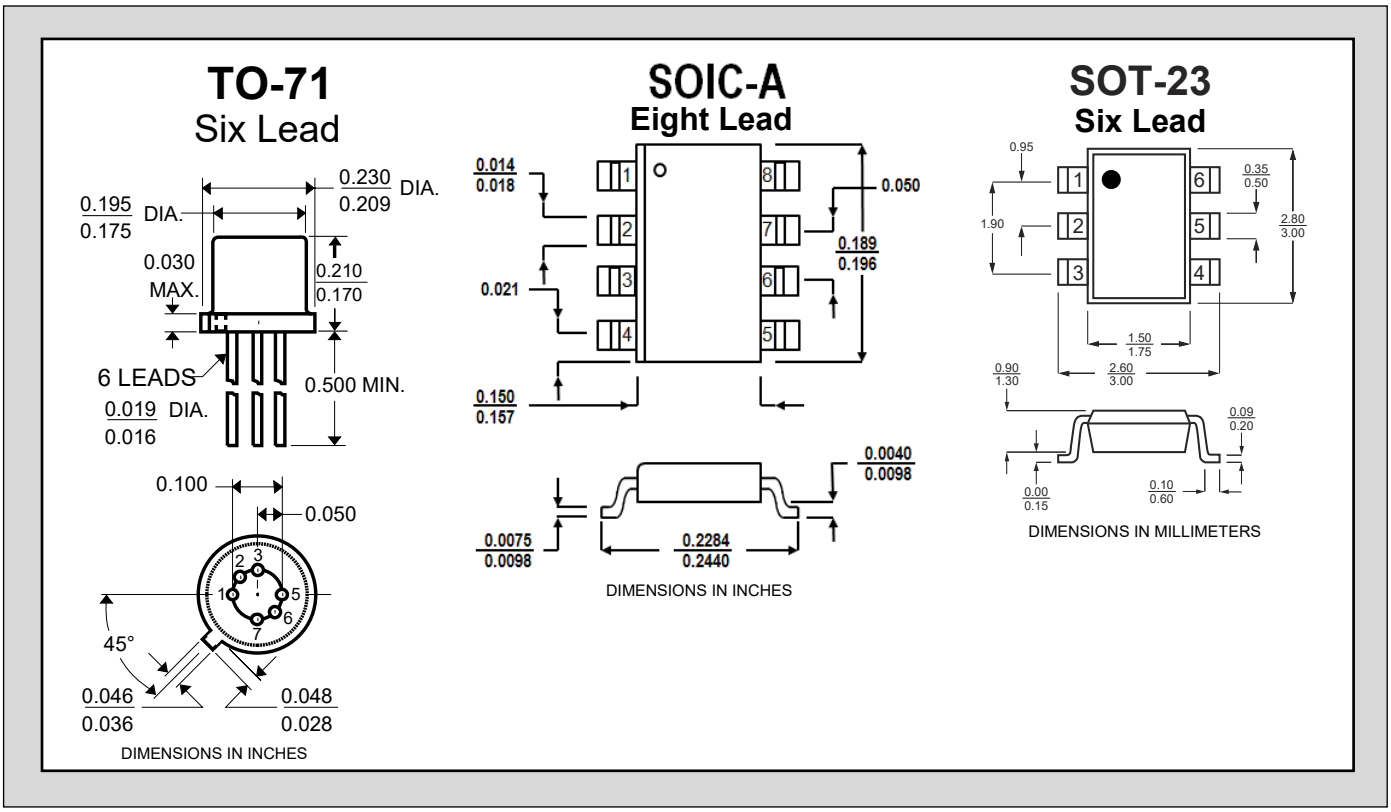
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			20	mV	V_{DS} = 10V, I_D = 5mA
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9		1.0		V_{DS} = 10V, V_{GS} = 0V (Note 2)
CMRR	**COMMON MODE REJECTION RATIO** $-20 \log \lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	85			dB	V_{DG} = 5V to 10V, I_D = 5mA

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
e_n	Noise Voltage		7		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 100Hz
e_n	Noise Voltage		4		nV/√Hz	V_{DS} = 10V, I_D = 5mA, *f* = 10kHz
C_{ISS}	Common Source Input Capacitance			5	pF	V_{DS} = 10V, I_D = 5mA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Capacitance			1.2	pF	

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-25			V	V_{DS} = 0, I_D = 1µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-1.5		-5	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.3		-4.0	V	V_{DS} = 10V, I_D = 5mA
I_{DSS}	Drain to Source Saturation Current		7.0		40	mA	V_{DS} = 10V, V_{GS} = 0V (Note 2)
I_G	Gate Operating Current			-1	-50	pA	V_{DG} = 10V, I_D = 5mA
I_{GSS}	Gate to Source Leakage Current				-50	pA	V_{gs} = -15V, V_{DS} = 0
G_{OS}	Output Conductance F = 1kHz				100	µS	V_{DS} = 10V, I_D = 5mA
NF	Noise Figure				1.0	dB	V_{DS} = 10V, I_D = 5mA, R_G = 100KΩ, *f* = 100Hz
G_{fs}	Forward Transconductance	*f* = 1kHz	4000		10000	µS	V_{Ds} = 10V, I_D = 5mA
		f = 100MHz		7000			
Gos	Output Transconductance	*f* = 1kHz			100		
		f = 100MHz		120			

PACKAGE DIMENSIONS



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300 µs, Duty Cycle ≤ 3%
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.0 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

LINEAR SYSTEMS

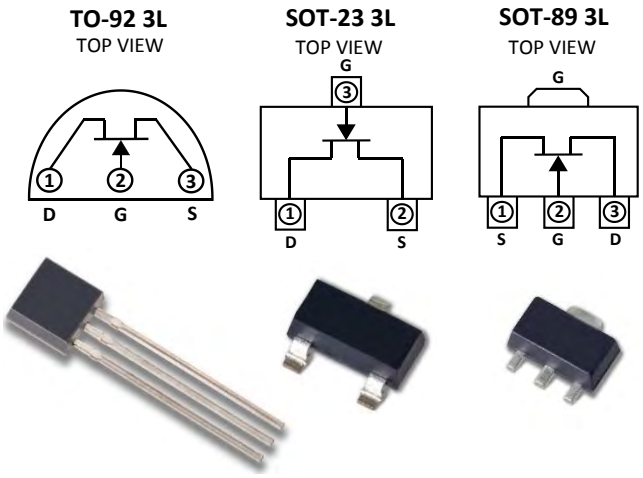
Over 30 Years of Quality Through Innovation

LSK170 A/B/C/D

High Input Impedance, Ultra-Low Noise, Single N-Channel JFET

Ultra-Low Noise at Both High & Low Frequencies With a Narrow Range of IDSS

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



Features

- ULTRA LOW NOISE (*f* =1khz): e_n = 0.9nV/√Hz
- High Breakdown Voltage: BV_{GSS} = 40V min
- High Gain: G_{fs} = 22mS (typ)
- High Input Impedance: 20GΩ typ
- Low Capacitance: 22pF max
- Improved Second Source Replacement for 2SK170
- For Equivalent Monolithic-Dual, See the LSK389 Series

Benefits

- Direct Pin-For-Pin Replacement of Toshiba's 2SK170
- Optimized to Provide Low Noise at Both High and Low Frequencies With a Narrow Range of IDSS and Low Capacitance
- Low Noise to Capacitance Ratio and Narrow Range of Low Value IDSS Provide Solutions for Low Noise Applications Which Cannot Tolerate High Values of Capacitance or Wide Ranges of IDSS

Applications

- Audio Amplifiers and Preamps
- Discrete Low-Noise Operational Amplifiers
- Guitar Pickups
- Effects Pedals
- Microphones
- Audio Mixer Consoles
- Acoustic Sensors
- Sonobouys
- Hydrophones

Applications Cont'd

- Chemical and Radiation Detectors
- Instrumentation Amplifiers
- Accelerometers
- CT Scanners Input Stages
- Oscilloscope Input Stages
- Electrometers and Vibrations Detectors

Description

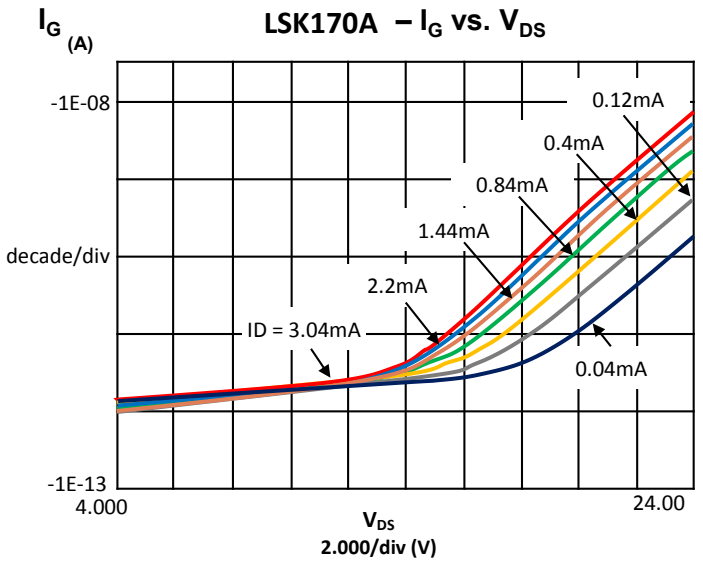
The LSK170 is specifically designed for low noise, high input impedance applications within the audio, instrumentation, medical and sensors markets. The narrow ranges of I_{DSS} grades with the LSK170 promote ease of design, particularly in low voltage applications. The LSK170 is ideal for portable battery operated applications, and features high BV_{DSS} for maximum linear headroom in high transient program content amplifiers. The series has a uniquely linear V_{GS} transfer function for a stability that is highly desirable, particularly for audio front-end preamplifiers. The device is available in a surface mount SOT-23 package, through-hole TO-92 package and SOT-89 package. The surface mount version of the LSK170 Series creates new opportunities for engineers seeking to design lower noise circuits in compact embeddable applications where shielding and space are critical. The LSK170 series is a pin for pin replacement of the Toshiba 2SK170 and improved functional replacement for the Interfet IF1320, IF1330, IF1331, and IF4500. Contact the factory for tighter noise and other specification selections.

Electrical Characteristics @ 25°C (unless otherwise stated)

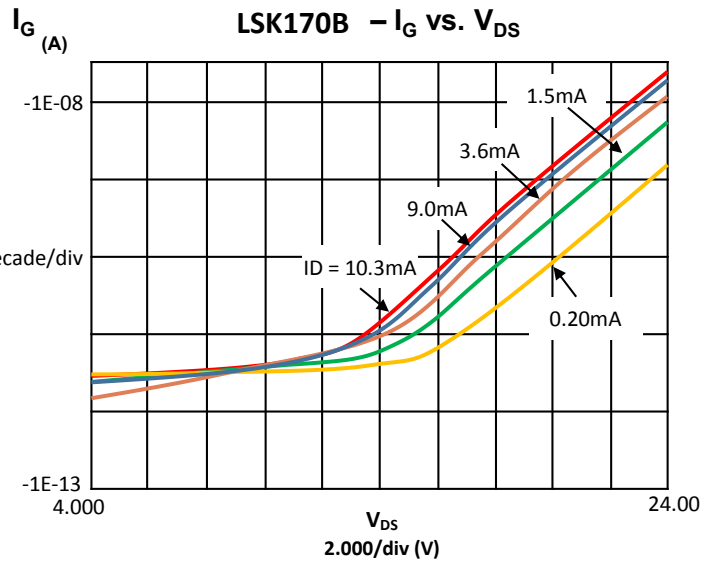
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-40.0			V	V_{DS} = 0V, I_D = -100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage		-0.2		-2.0	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage			0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS}[2]	Drain to Source Saturation Current	LSK170A	2.6		6.5	mA	V_{DS} = 10V, V_{GS} = 0
		LSK170B	6.0		12.0		
		LSK170C	10.0		20.0		
		LSK170D	18.0		30.0		
I_G	Gate Operating Current				-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current				-1.0	nA	V_{Gs} = -10V, V_{Ds} = 0V
G_{fs}	Full Conduction Transconductance		14.0	22.0		mS	V_{DS} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Typical Conduction Transconductance		6.0	10.0		mS	V_{DS} = 15V, I_D = 1mA
e_n	Noise Voltage			0.9	1.9	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage			1.4	4.0	nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance			20.0		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz,
C_{RSS}	Common Source Reverse Transfer Cap.			5.0		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz,

Typical Characteristics

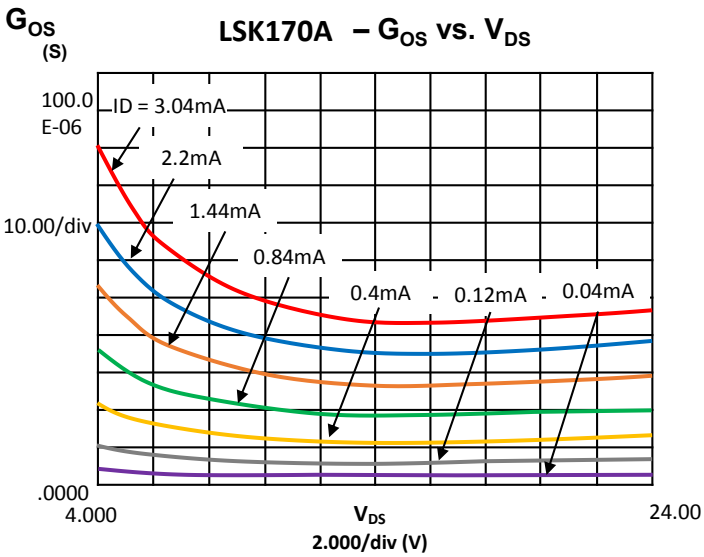
Operating Current



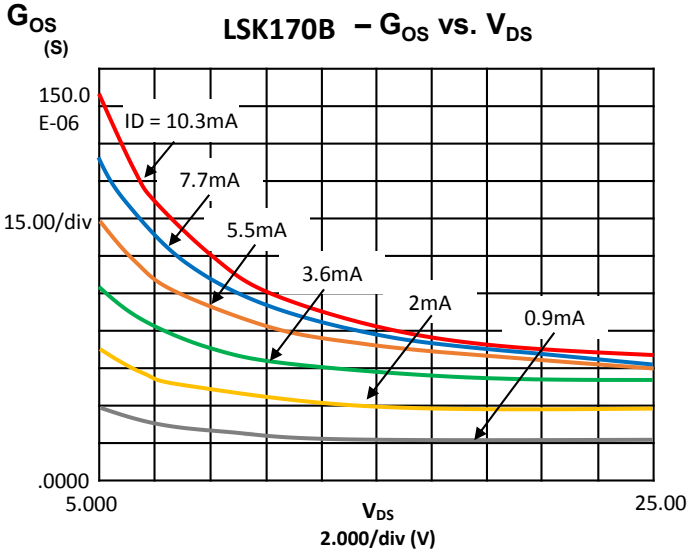
Operating Current



Output Conductance

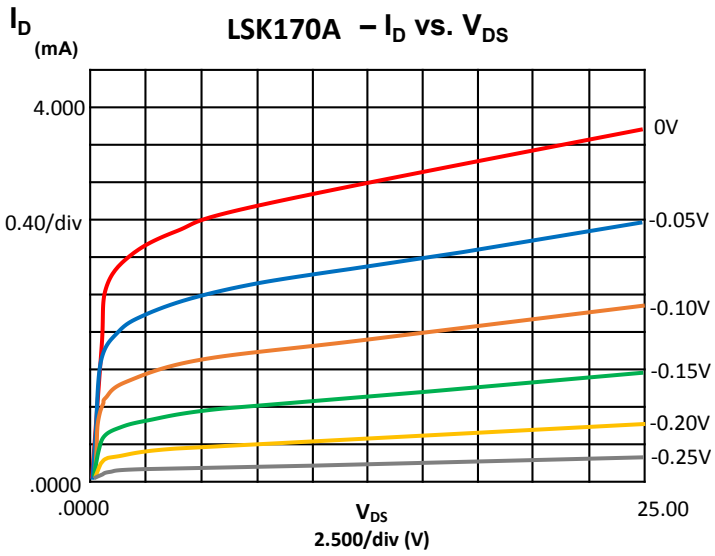


Output Conductance

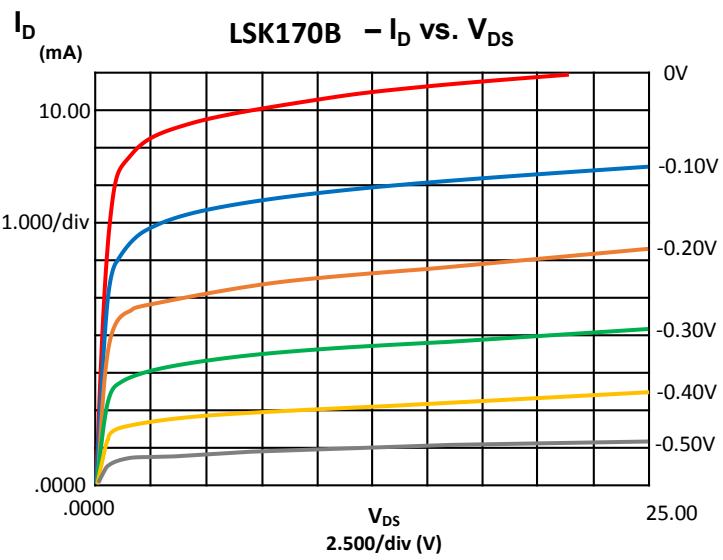


Typical Characteristics Continued

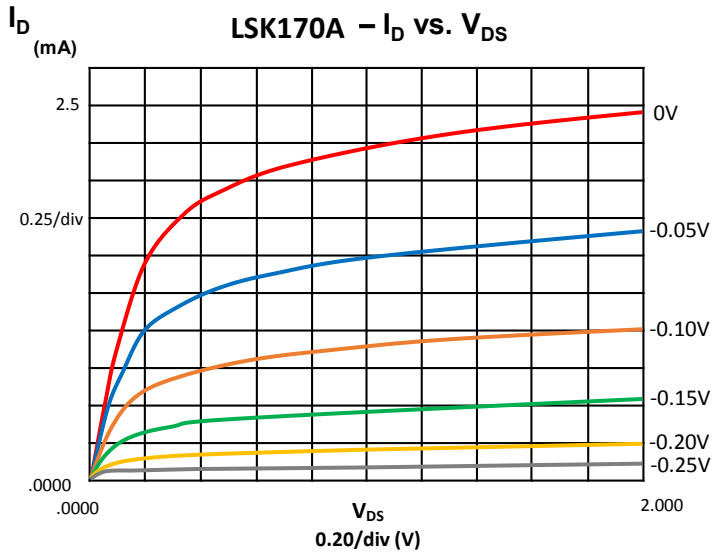
Output Characteristics



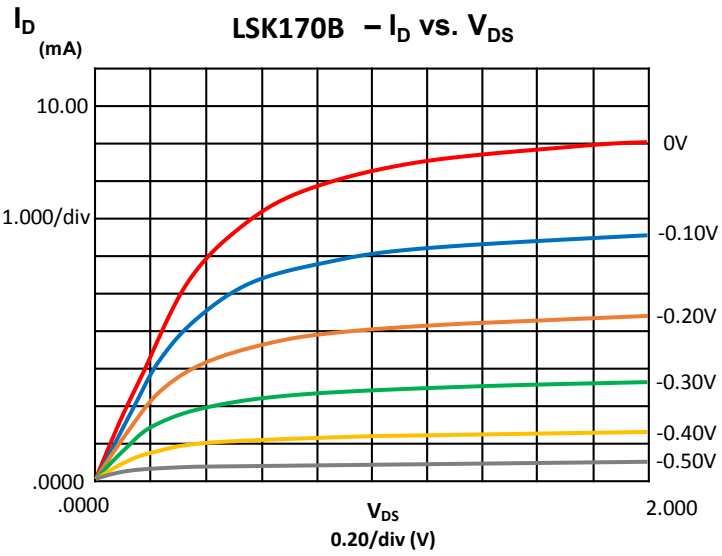
Output Characteristics



Operating Characteristics

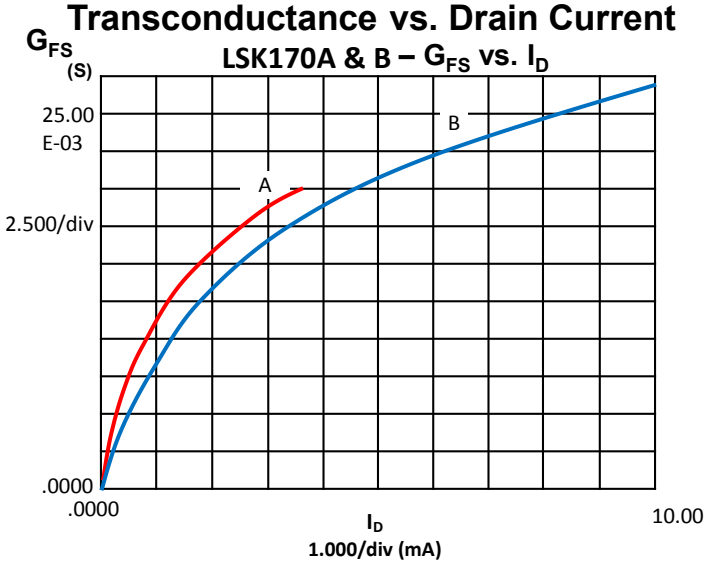


Operating Characteristics

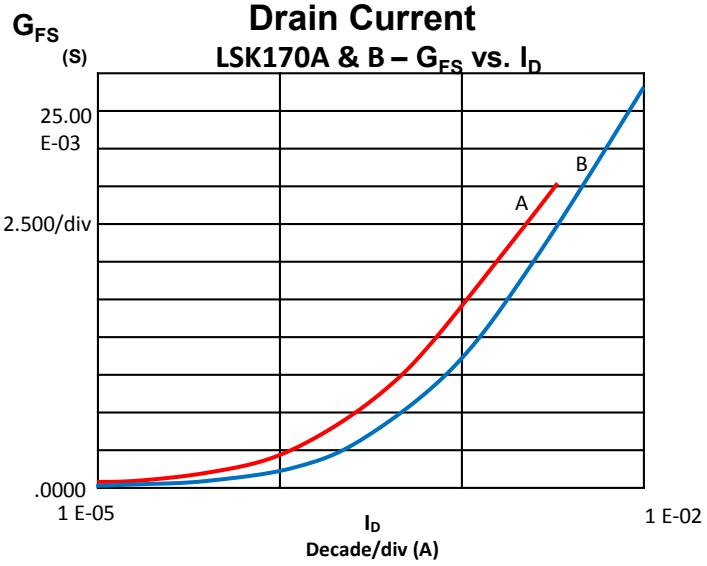


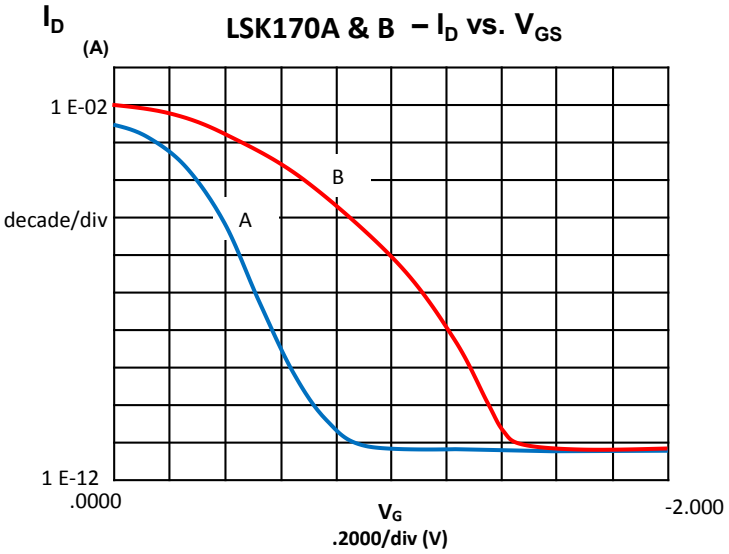
Typical Characteristics Continued

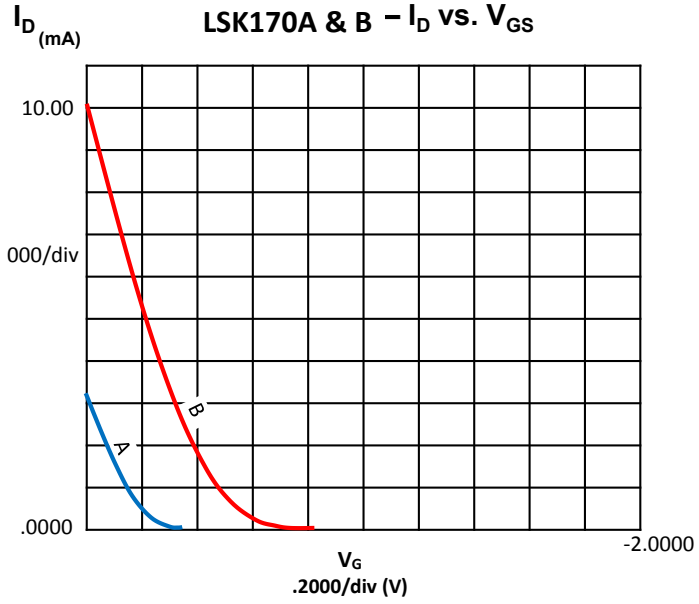
Common Source Forward Transconductance vs. Drain Current



Common Source Transconductance vs. Drain Current

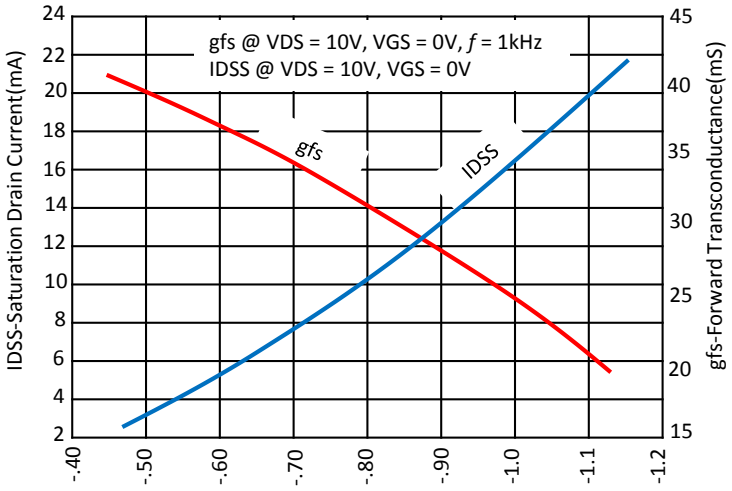




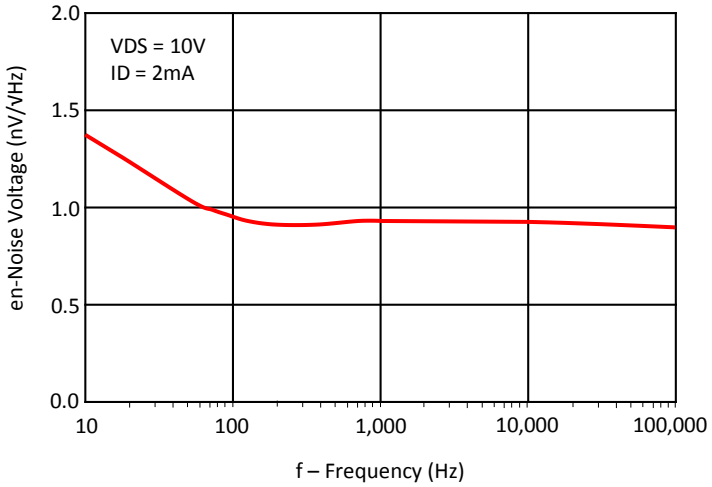


Typical Characteristics Continued

Drain Current Transconductance vs. Gate-Source Cutoff Voltage



Equivalent Input Noise Voltage vs. Frequency

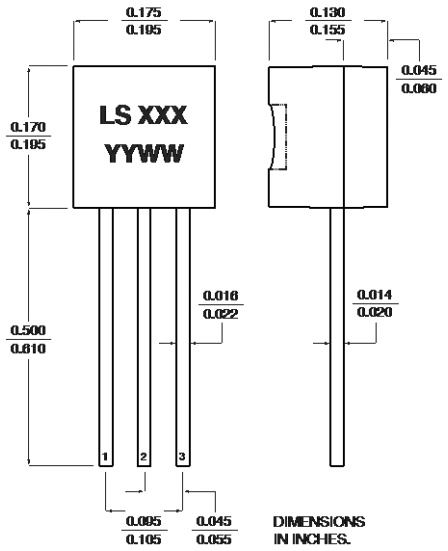


Ordering Information

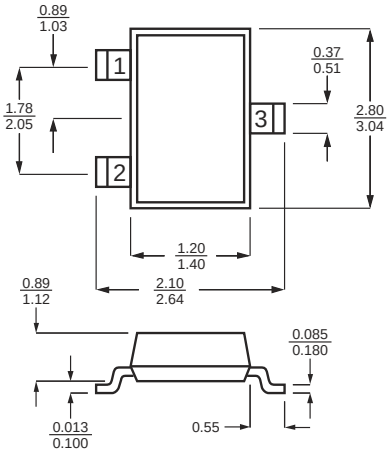
STANDARD PART CALL-OUT	CUSTOM PART CALL-OUT CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LSK170A TO-92 3L RoHS	LSK170A TO-92 3L RoHS SELXXXX
LSK170B TO-92 3L RoHS	LSK170B TO-92 3L RoHS SELXXXX
LSK170C TO-92 3L RoHS	LSK170C TO-92 3L RoHS SELXXXX
LSK170D TO-92 3L RoHS	LSK170D TO-92 3L RoHS SELXXXX
LSK170A SOT-23 3L RoHS	LSK170A SOT-23 3L RoHS SELXXXX
LSK170B SOT-23 3L RoHS	LSK170B SOT-23 3L RoHS SELXXXX
LSK170C SOT-23 3L RoHS	LSK170C SOT-23 3L RoHS SELXXXX
LSK170D SOT-23 3L RoHS	LSK170D SOT-23 3L RoHS SELXXXX
LSK170A SOT-89 3L RoHS	LSK170A SOT-89 3L RoHS SELXXXX
LSK170B SOT-89 3L RoHS	LSK170B SOT-89 3L RoHS SELXXXX
LSK170C SOT-89 3L RoHS	LSK170C SOT-89 3L RoHS SELXXXX
LSK170D SOT-89 3L RoHS	LSK170D SOT-89 3L RoHS SELXXXX

Package Dimensions

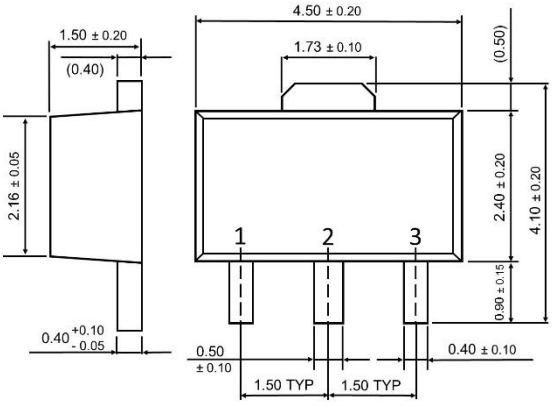
TO-92 3 Lead



SOT-23 3 Lead



SOT-89 3 Lead



Notes:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.
7. Voltage specifications are not tested 100%, but guaranteed by lot sampling. Contact the factory if 100% test is required.

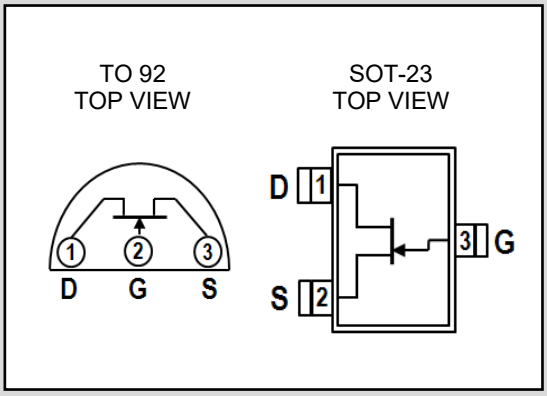
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LSK189

LOW NOISE, LOW CAPACITANCE SINGLE N-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE	e_n = 1.8nV/√Hz
LOW INPUT CAPACITANCE	C_{ISS} = 4pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation TA=25°C	300mW[4]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSO} = 60V
Gate to Drain	V_{GDO} = 60V

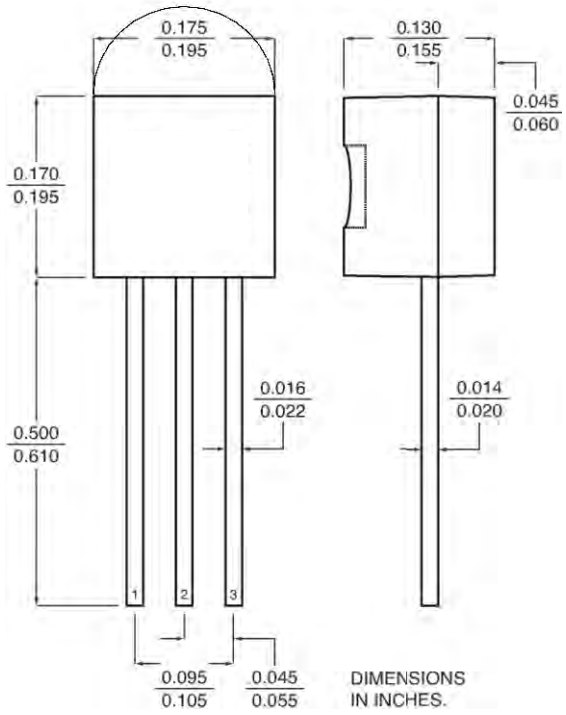


* For equivalent monolithic dual, see LSK489

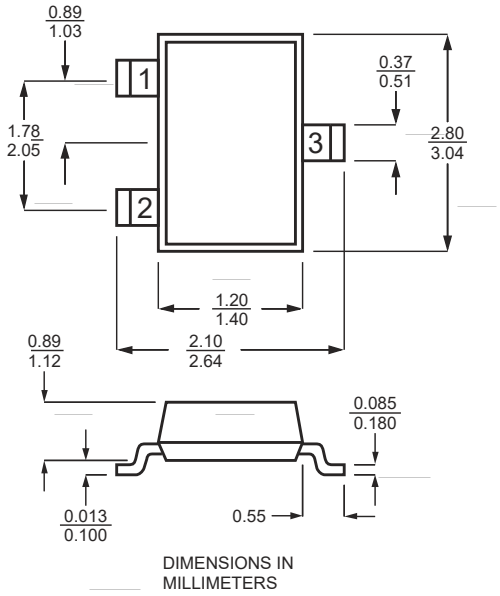
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = -1nA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.5		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}[2]	Drain to Source Saturation Current	2.5	5	15	mA	V_{DS} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-2	-25	pA	V_{DG} = 15V, I_D = 200µA
I_G			-0.8	-10	nA	TA=125°C
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{GS} = -15V
G_{fs}	Full Conductance Transconductance	1500			µS	V_{DS} = 15V, V_{GS} = 0, *f* = 1kHz
		1000	1500		µS	V_{DS} = 15V, I_D = 500µA
G_{OS}	Full Output Conductance			40	µS	V_{DS} = 15V, V_{GS} = 0
G_{OS}	Output Conductance		1.8	2.7	µS	V_{DS} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz
e_n	Noise Voltage		1.8	2.0	nV/√Hz	V_{DS} = 15V, I_D = 2mA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage		2.8	3.5	nV/√Hz	V_{DS} = 15V, I_D = 2mA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		4	8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			3	pF	

Standard Package Dimensions:

TO-92



SOT-23

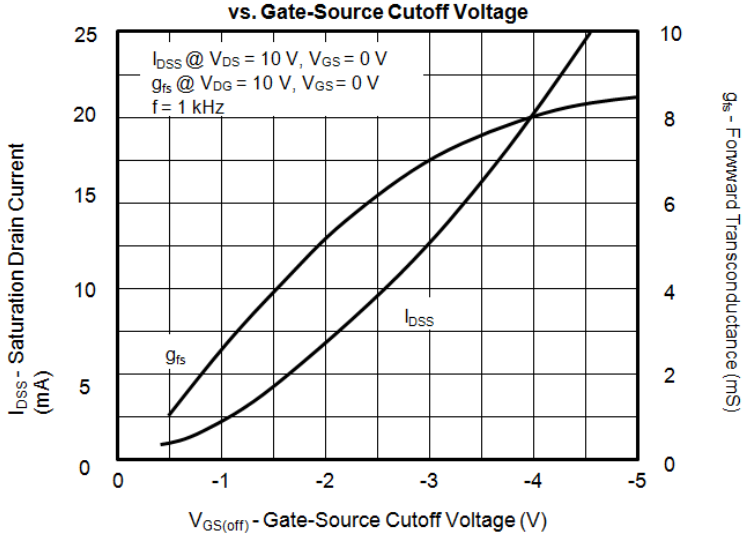


NOTES:

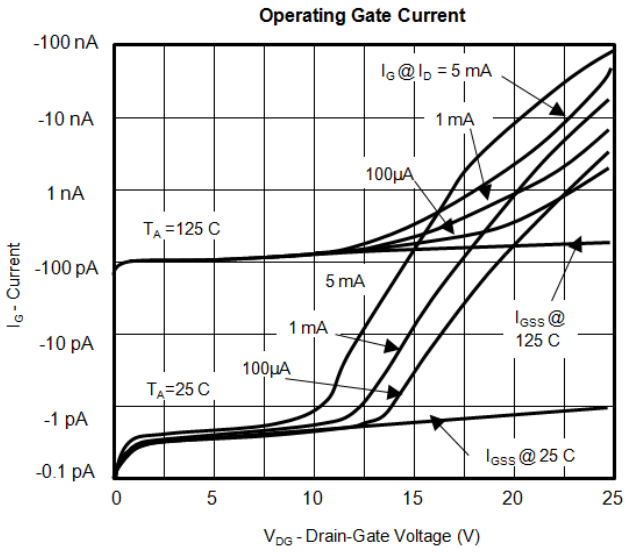
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%.
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. Derate 2.8 mW °C above 25°C.

LSK189 Typical Characteristics

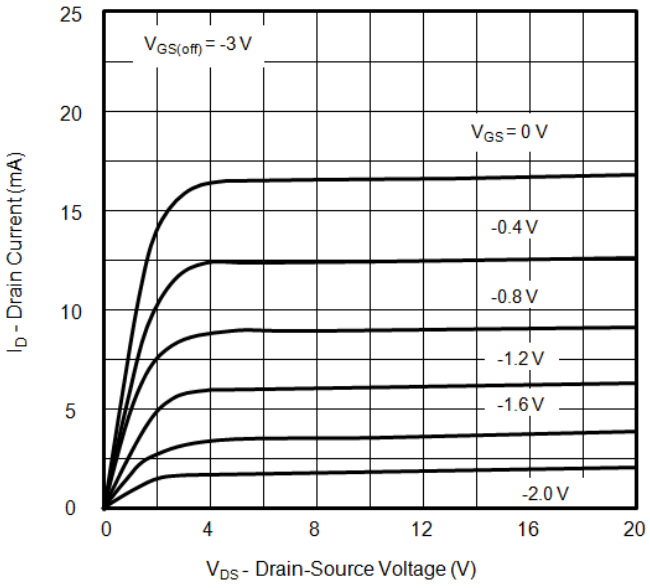
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



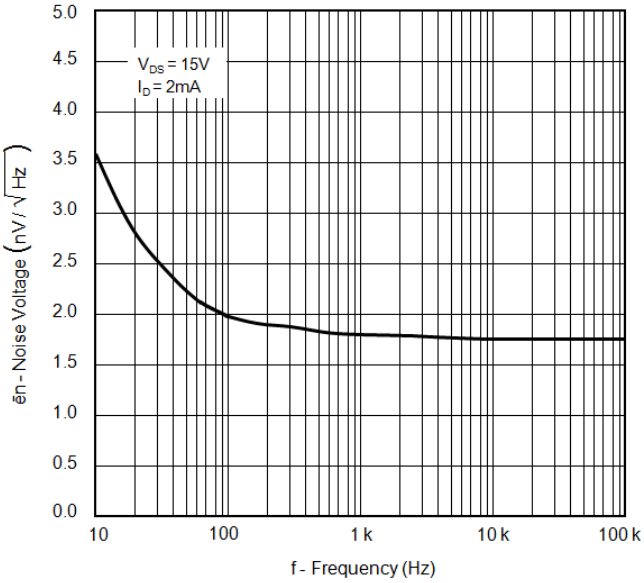
Operating Gate Current



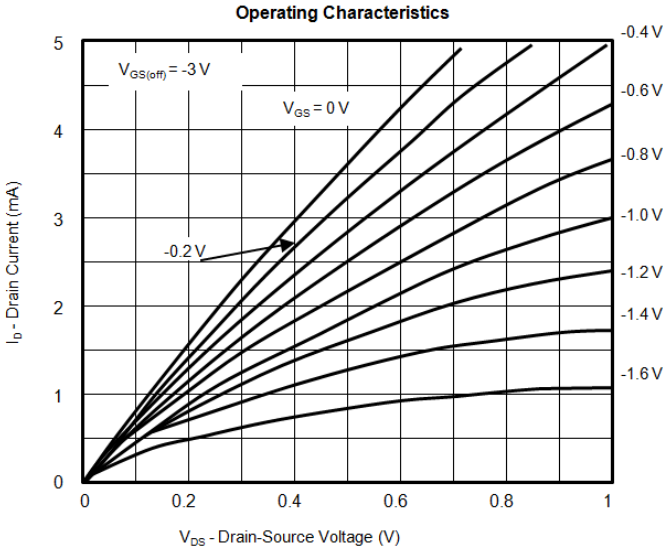
Output Characteristics



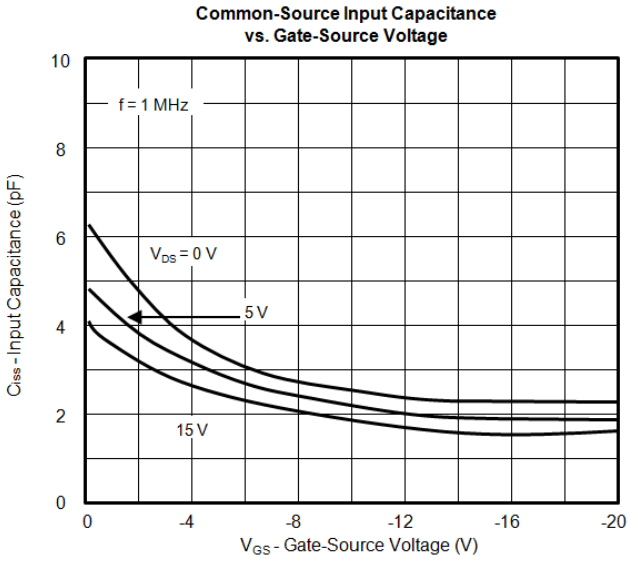
Equivalent Input Noise Voltage vs. Frequency



Operating Characteristics

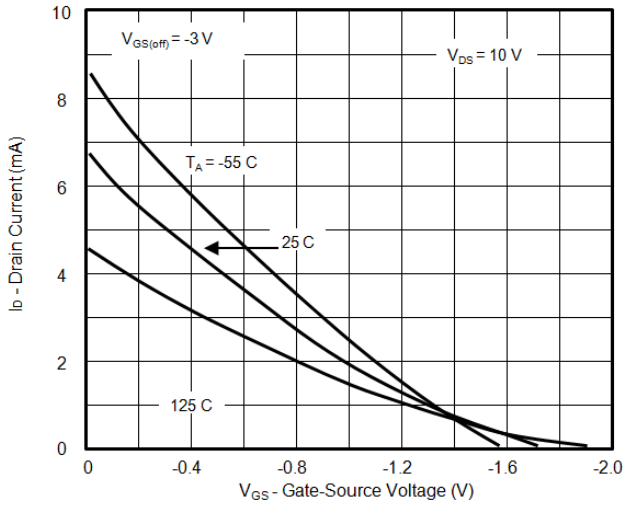


Common-Source Input Capacitance vs. Gate-Source Voltage

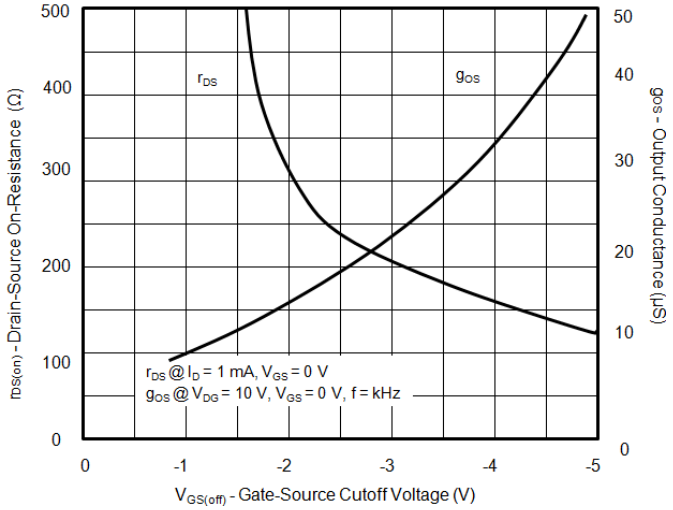


LSK189 Typical Characteristics Continued

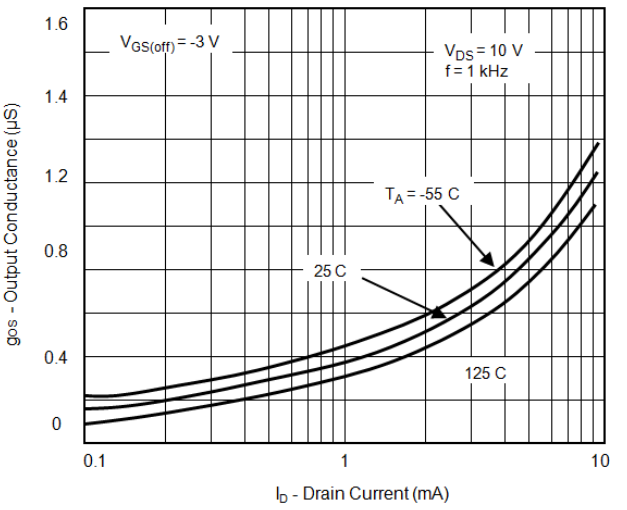
Transfer Characteristics



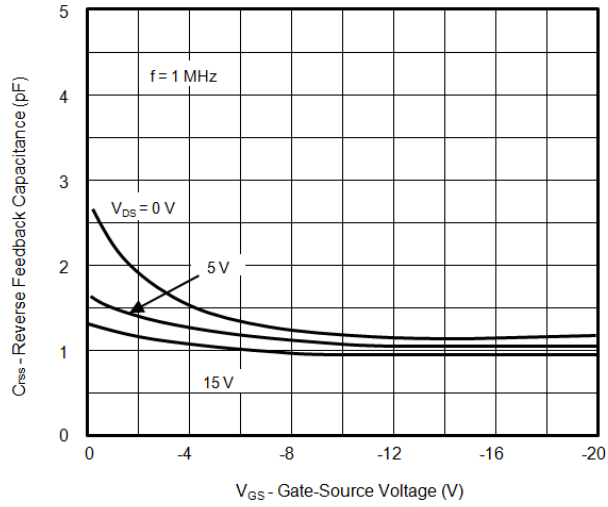
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



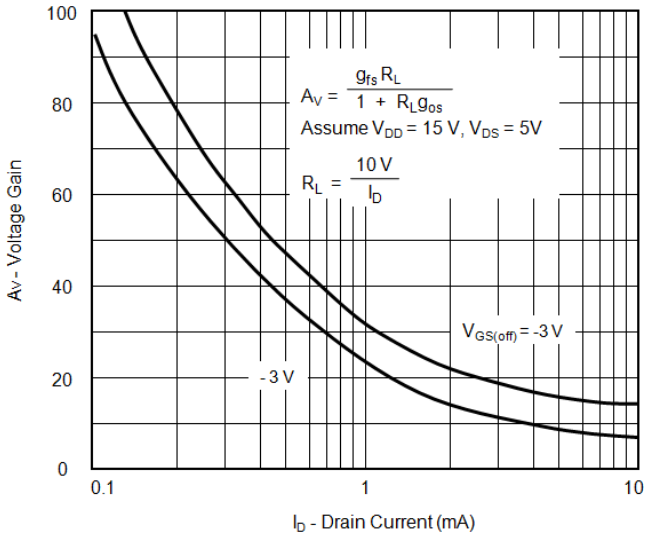
Output Conductance vs. Drain Current



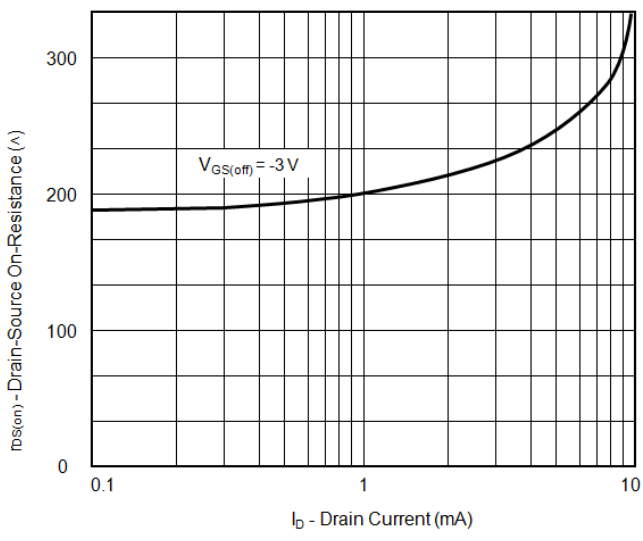
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Circuit Voltage Gain vs. Drain Current

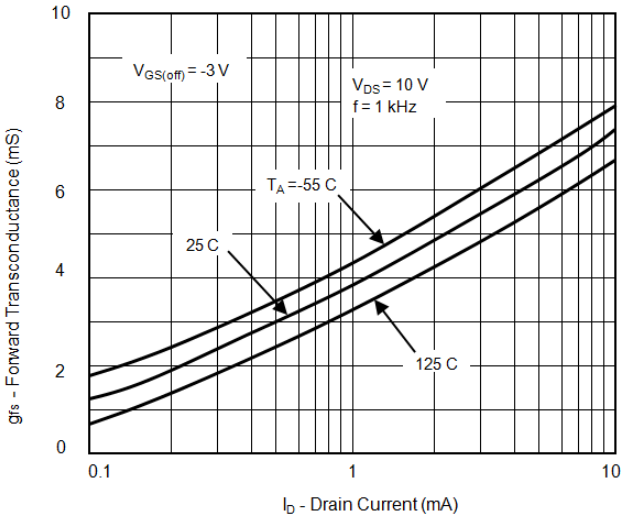


On-Resistance vs. Drain Current



LSK189 Typical Characteristics Continued

Common-Source Forward Transconductance vs. Drain Current

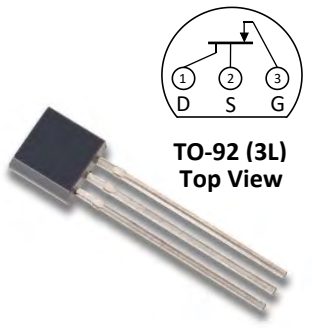


J/SST201/2/4

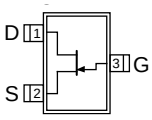
High Gain, Single N-Channel JFET Amplifier

General Purpose, Low Noise, Low Cost, Single JFET

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V



TO-92 (3L)
Top View



SOT-23 (3L)
Top View

Features

- Low Cutoff Voltage: J201 <1.5V
- High Input Impedance
- Very Low Noise
- High Gain: AV = 80 @ 20 µA
- Reverse Gate to Source and Drain Voltage ≥| -40V

Benefits

- Low Cost
- Excellent Low Power Supply Operation
- Power Supply: Down to 1.5V
- Low Signal Loss/System Error
- High System Sensitivity
- High Quality Low-Level Signal

Applications

- High-Gain, Low Noise Amplifiers
- Low-Current, Low-Voltage Battery-Powered Amplifiers
- Infrared Detector Amplifiers
- Ultra-High Input Impedance Pre-Amplifiers

Description

The J/SST201/2/4 series is a low cost direct replacement for Siliconix J/SST201/2/4 series. Features include low leakage, very low noise, low cutoff voltage ($V_{GS(off)}$ ≤ 1.5V) and high Gain (A_V = 80 V/V) for use with low-level power supplies. The J/SST201/2/4 is excellent for battery powered equipment and low current amplifiers. The J series, TO-226 (TO-92) plastic package, provides low cost, while the SST series, TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly and in die form for automated assembly.

Electrical Characteristics @ 25 °C (unless otherwise stated)

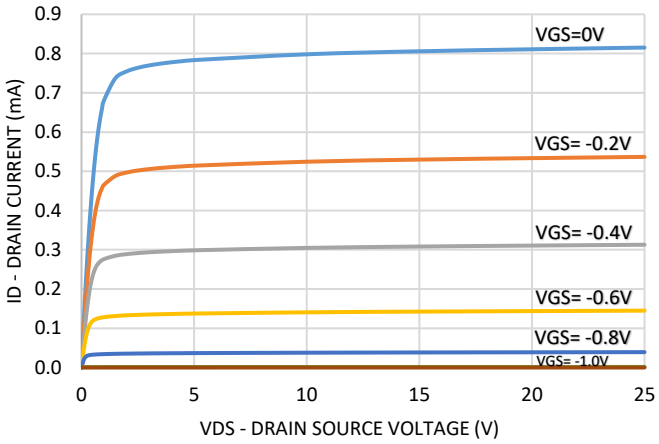
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	J/SST201, 202	-40			V	I_G = -1µA, V_{DS} = 0.0V
		J/SST204	-25				
$V_{GS(off)}$	Gate to Source Cutoff Voltage	J/SST201	-0.3		-1.5		V_{DS} = 15V, I_D = 10nA
		J/SST202	-0.8		-4.0		
		J/SST204	-0.2		2.0		
I_{DSS}	Drain to Source Saturation Current[2]	J/SST201	0.2		1.0	mA	V_{DS} = 15V, V_{GS} = 0.0V
		J/SST202	0.9		4.5		
		J/SST204	0.2		3.0		
I_{GSS}	Gate Reverse Current				-100	pA	V_{GS} = -20V, V_{DS} = 0.0V
I_G	Gate Operating Current			-2			V_{DG} = 10V, I_D = 0.1mA
$I_{D(off)}$	Drain Cutoff Current			2			V_{DS} = 15V, V_{GS} = 5.0V

Electrical Characteristics @ 25 °C (unless otherwise stated) Continued

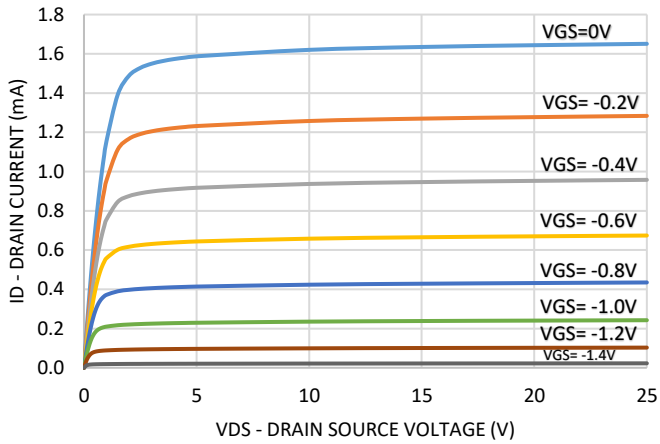
SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs}	Forward Transconductance	J/SST201, 204	0.5			mS	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1kHz
		J/SST202	1.0				
C_{iss}	Input Capacitance			4.5		pF	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance			1.3			
e_n	Noise Voltage			4.0		nV/√Hz	V_{DS} = 10V, V_{GS} = 0.0V, *f* = 1kHz

Typical Characteristics

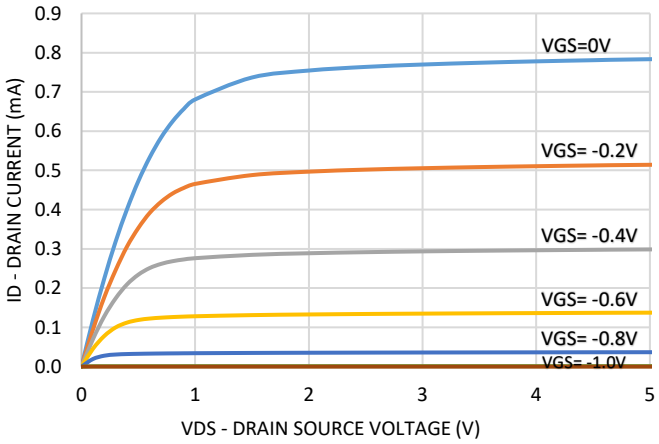
Output Characteristic
J201 - (VGS(off) = -1.1V)



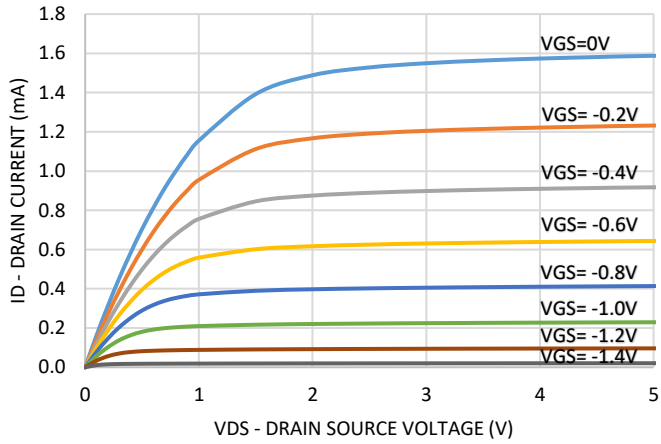
Output Characteristic
J202 - (VGS(off) = -1.75V)



Output Characteristic
J201 - (VGS(off) = -1.1V)

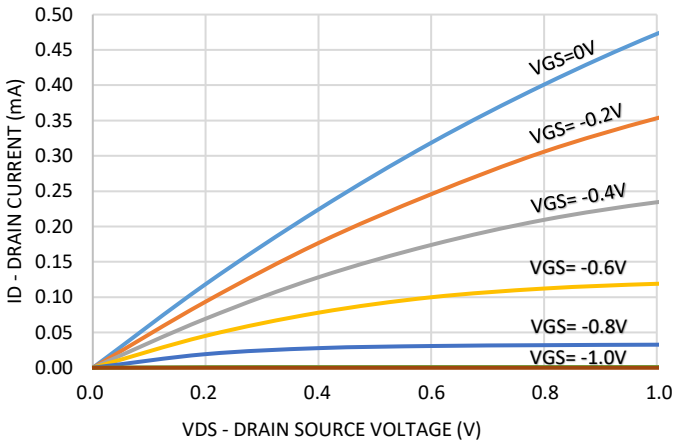


Output Characteristic
J202 - (VGS(off) = -1.75V)

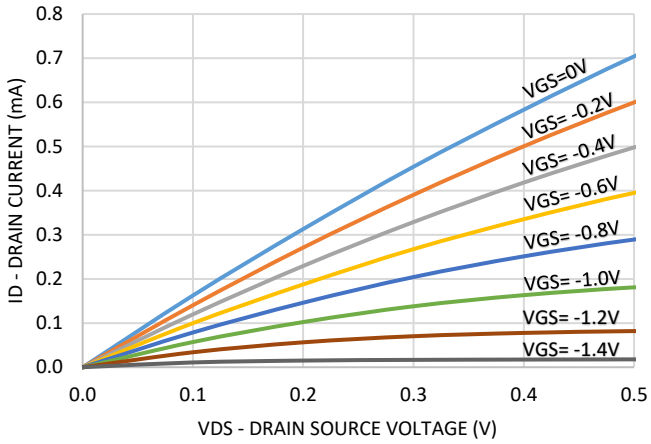


Typical Characteristics Continued

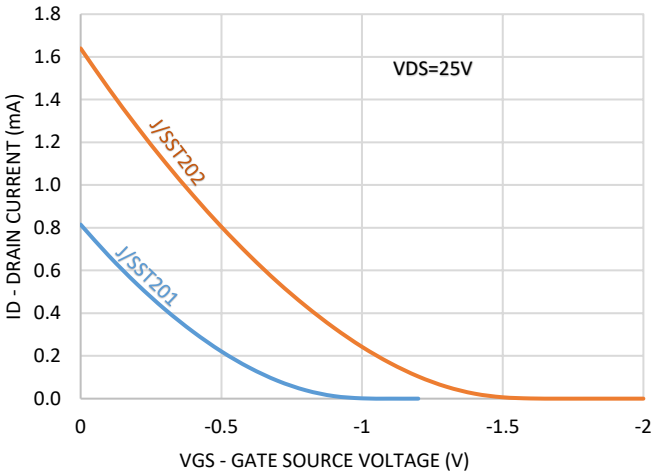
Output Characteristic
J201 - (VGS(off) = -1.1V)



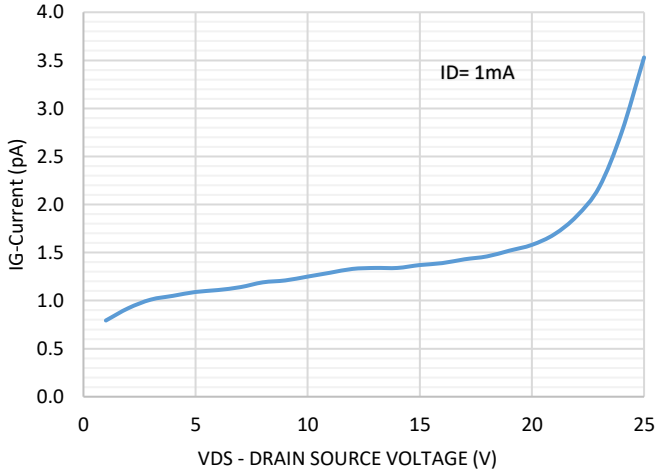
Output Characteristic
J202 - (VGS(off) = -1.75V)



Transfer Characteristics

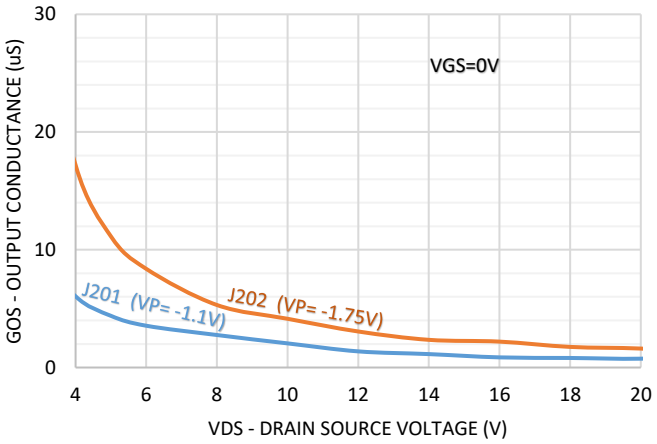


Operating Gate Current

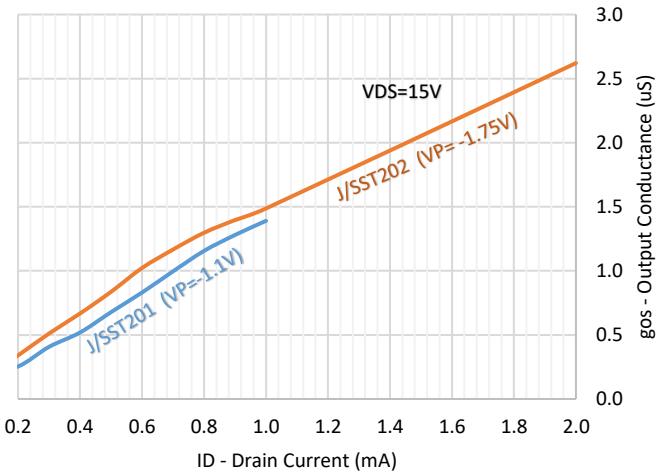


Typical Characteristics Continued

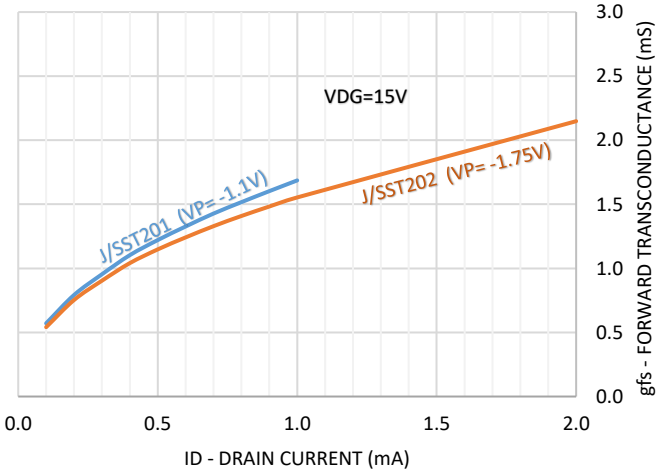
Output Conductance vs Drain Source Voltage



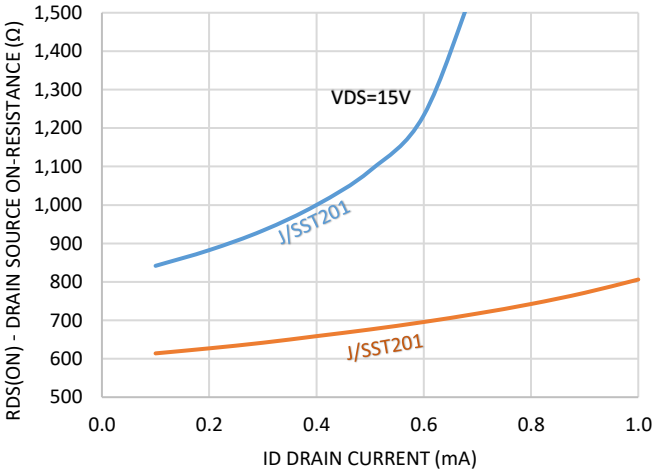
Output Conductance vs. Drain Current



Forward Transconductance vs. Drain Current

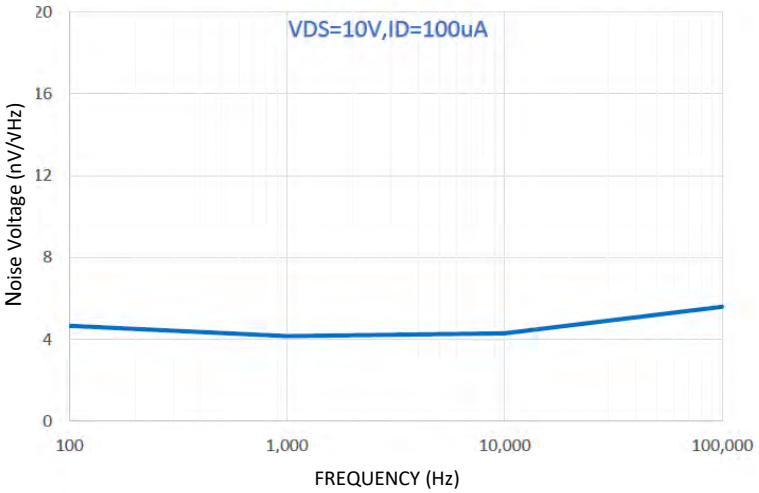


RDS - ID

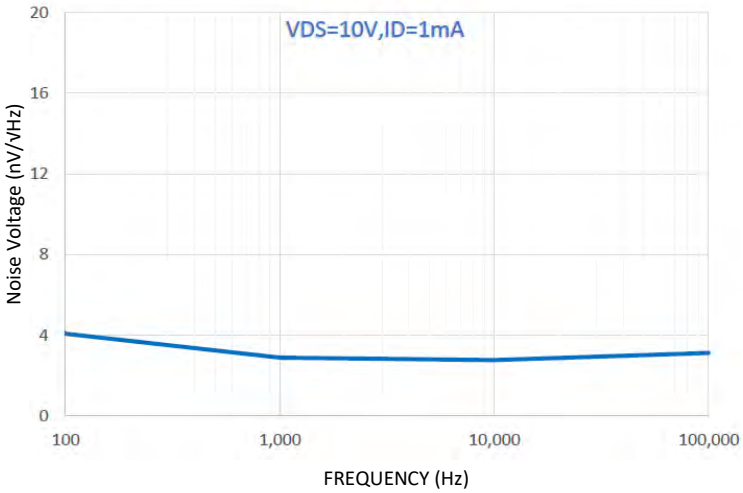


Typical Characteristics Continued

Input Noise Voltage vs Frequency

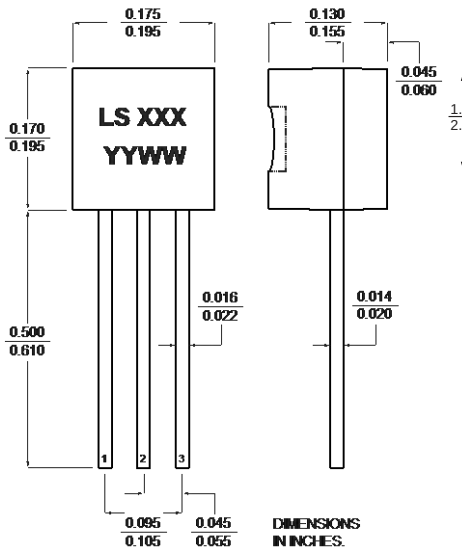


Input Noise Voltage vs Frequency

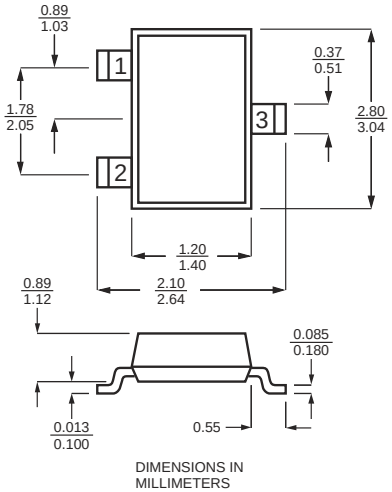


Package Dimensions

TO-92 3 Lead



SOT-23 3 Lead



Ordering Information

STANDARD PART CALL-OUT
J201 TO-92 3L RoHS
J202 TO-92 3L RoHS
J204 TO-92 3L RoHS
SST201 SOT-23 3L RoHS
SST202 SOT-23 3L RoHS
SST204 SOT-23 3L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
J201 TO-92 3L RoHS SELXXXX
J202 TO-92 3L RoHS SELXXXX
J204 TO-92 3L RoHS SELXXXX
SST201 SOT-23 3L RoHS SELXXXX
SST202 SOT-23 3L RoHS SELXXXX
SST204 SOT-23 3L RoHS SELXXXX

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

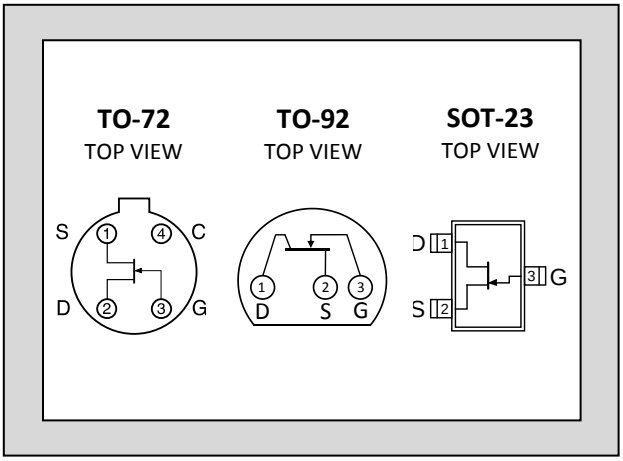
LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

LS846

LOW NOISE LOW LEAKAGE SINGLE N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW NOISE	e_n = 3nV/√Hz
LOW INPUT CAPACITANCE	C_{ISS} = 4pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation TA=25°C	300mW[3]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSO} = 60V
Gate to Drain	V_{GDO} = 60V

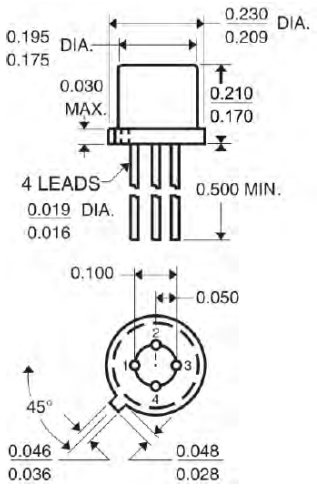


*For equivalent Monolithic Dual, see LS843 Family

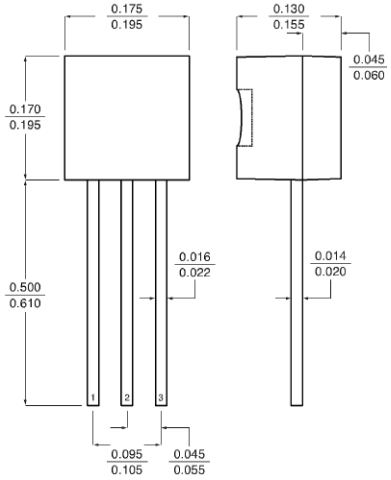
SYMBOL	CHARACTERISTIC[2]	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-60			V	V_{DS} = 0, I_D = 1nA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1		-3.5	V	V_{DS} = 15V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage	-0.5		-3.5	V	V_{DS} = 15V, I_D = 500µA
I_{DSS}	Drain to Source Saturation Current	1.5	5	15	mA	V_{DS} = 15V, V_{GS} = 0
I_G	Gate Operating Current		-15	-50	pA	V_{DG} = 15V, I_D = 500µA
I_G	Gate Operating Current Reduced V_{DG}		-5	-30	pA	V_{DG} = 3V, I_D = 500µA
I_{GSS}	Gate to Source Leakage Current			-100	pA	V_{GS} = 15V, V_{DS} = 0
G_{fss}	Full Conductance Transconductance	1500			µS	V_{DS} = 15V, V_{GS} = 0, *f* = 1kHz
G_{fs}	Typical Operation Transconductance	1000	1500		µS	V_{DS} = 15V, I_D = 200µA
G_{OSS}	Full Output Conductance			40	µS	V_{DS} = 15V, V_{GS} = 0
G_{OS}	Typical Operation Output Conductance		2.0	2.70	µS	V_{DS} = 15V, I_D = 200µA
NF	Noise Figure			0.5	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 10MΩ, *f* = 100Hz, NBW = 6Hz
e_n	Noise Voltage		3	7	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 1kHz, NBW = 1Hz
e_n	Noise Voltage			11	nV/√Hz	V_{DS} = 15V, I_D = 500µA, *f* = 10Hz, NBW = 1Hz
C_{ISS}	Common Source Input Capacitance		4	8	pF	V_{DS} = 15V, I_D = 500µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.			3	pF	

STANDARD PACKAGE DIMENSIONS:

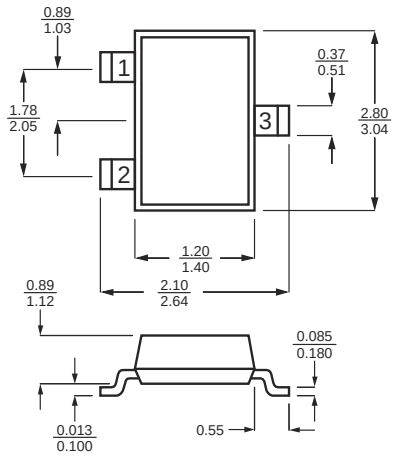
TO-72
Four Lead



TO-92
Three Lead



SOT-23
Three Lead



*Dimensions in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate negative electrical polarity only.
3. Derate 2.8mW/ºC above 25ºC.

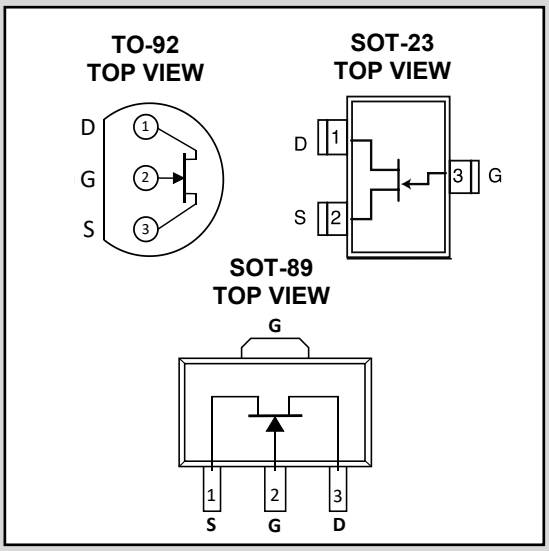
LINEAR SYSTEMS

Quality Through Innovation Since 1987

LSK170X-1

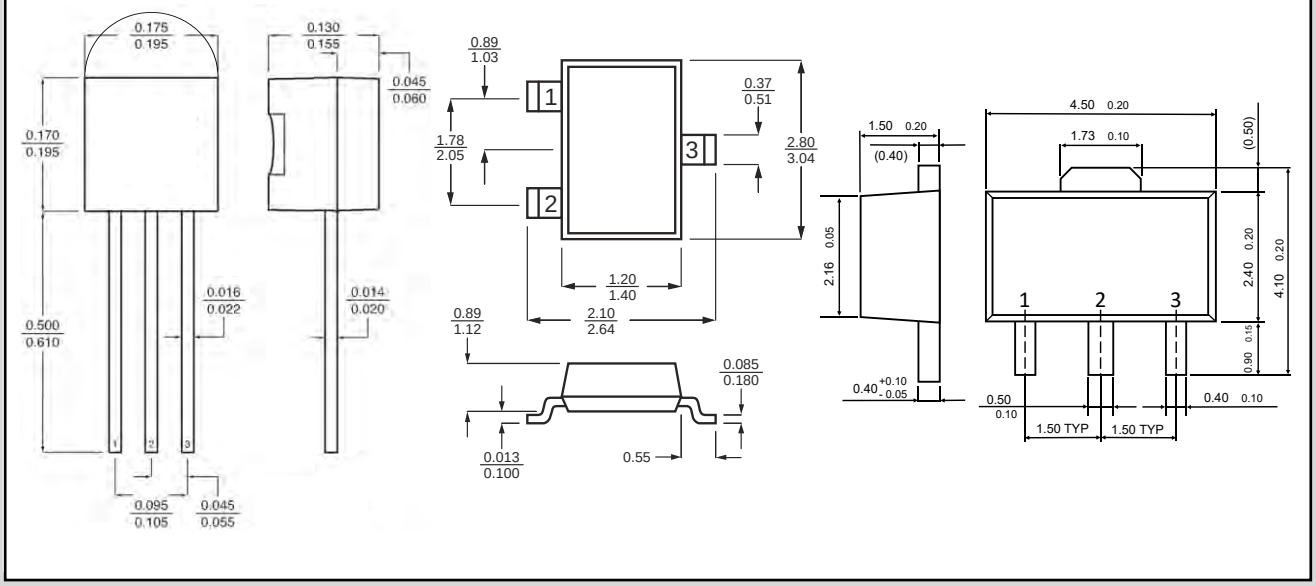
ULTRA LOW NOISE, HIGH IDSS SINGLE N-CHANNEL JFET AMPLIFIER

FEATURESss	
ULTRA LOW NOISE (f=1kHz)	e_n = 1.9NV/√HZ
HIGH BREAKDOWN VOLTAGE	BV_{GSS}=40V min
HIGH GAIN	G_{fs}=22mS (typ)
HIGH INPUT IMPEDENCE	I_G= -500pA max
LOW CAPACITANCE	20pF (typ)
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation@+25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$= 10mA
Maximum Voltages	
Gate to Source	V_{GS} = 40V
Gate to Drain	V_{GD} = 40V



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	V_{DS} = 0, I_D = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-0.2		-2	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS2}	Drain to Source Saturation Current	20		50	mA	V_{DS} = 10V, V_{GS} = 0
I_G	Gate Operating Current			-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current			-1	nA	V_{GS} = -10V, V_{DS} = 0
G_{fS}	Full Conduction Transconductance		22		mS	V_{GD} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fS}	Typical Conduction Transconductance		10		mS	V_{DG} = 15V, I_D = 1mA
e_n	Noise Voltage		1.9		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz, NBW=1Hz
e_n	Noise Voltage		4.0		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 10 Hz, NBW=1Hz
C_{ISS}	Common Source Input Capacitance		20		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		5		pF	



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

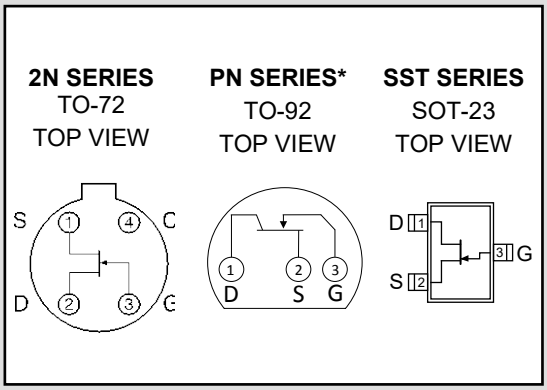
LINEAR SYSTEMS

Improved Standard Products®

2N/PN/SST4416 & 4416A

N-CHANNEL JFET HIGH FREQUENCY AMPLIFIER

FEATURES	
Replacement For SILICONIX 2N/SST4416 & 2N4416A	
VERY LOW NOISE FIGURE (400 MHz)	4 dB
EXCEPTIONAL GAIN (400 MHz)	10 dB
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
Maximum Currents	
Gate Current	10mA
Maximum Voltages	
Gate to Drain or Gate to Source 2N4416	-30V
Gate to Drain or Gate to Source 2N4416A	-35V



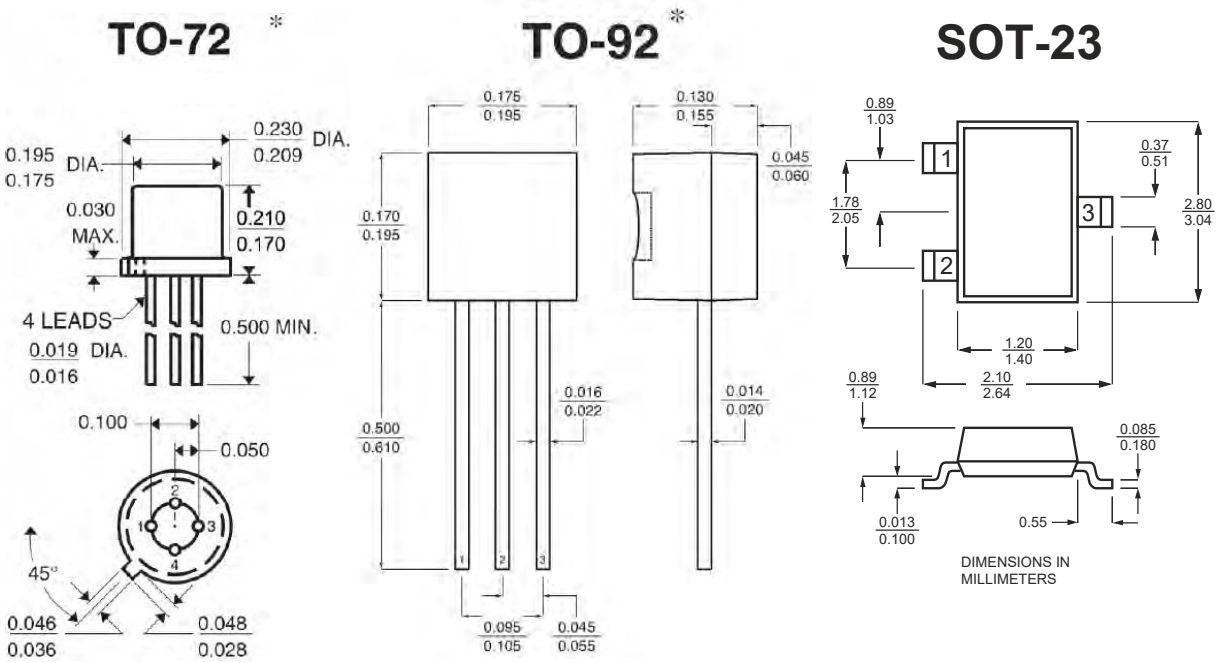
*Optional Package for 2N4416

ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	2N/PN/SST4416	-30			V	I_G = -1µA, V_{DS} = 0V
		2N4416A	-35				
$V_{GS(off)}$	Gate to Source Cutoff Voltage	2N/PN/SST4416			-6		V_{DS} = 15V, I_D = 1nA
		2N4416A	-2.5		-6		
I_{DSS}	Gate to Source Saturation Current		5		15	mA	V_{DS} = 15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	2N			-0.1	nA	V_{GS} = -20V, V_{DS} = 0V
		PN/SST			-1.0		V_{GS} = -15V, V_{DS} = 0V
g_{fs}	Forward Transconductance		4000		7500	µS	V_{DS} = 15V, V_{GS} = 0V, *f* = 1kHz
g_{os}	Output Conductance				100		
C_{iss}	Input Capacitance[2]				0.8	pF	V_{DS} = 15V, V_{GS} = 0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance[2]				4		
C_{oss}	Output Capacitance[2]				2		
e_n	Equivalent Input Noise Voltage			6		nV/√Hz	V_{DS} = 10V, V_{GS} = 0V, *f* = 1kHz

HIGH FREQUENCY ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	100 MHz		400 MHz		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
g_{iss}	Input Conductance[2]		100		1000	μS	V_{DS} = 15V, V_{GS} = 0V
b_{iss}	Input Susceptance[2]		2500		10000		
g_{oss}	Output Conductance[2]		75		100		
b_{oss}	Output Susceptance[2]		1000		4000		
G_{fs}	Forward Transconductance[2]			4000			
G_{ps}	Power Gain[2]	18		10		dB	V_{DS} = 15V, I_D = 5mA
NF	Noise Figure[2]		2		4		V_{DS} = 15V, I_D = 5mA, R_G = 1kΩ



*Dimensions in Inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Not production tested, guaranteed by design.

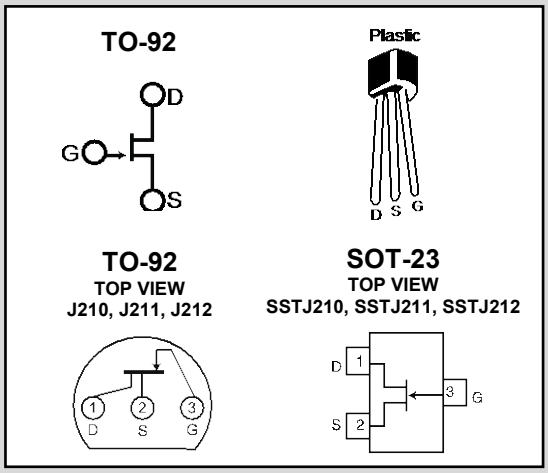
LINEAR SYSTEMS

Improved Standard Products®

SST/J210, 211 & 212

LOW NOISE N-CHANNEL JFET GENERAL PURPOSE AMPLIFIER

FEATURES	
HIGH GAIN g_{fs}=7000µmho MINIMUM (J211, J212)	
HIGH INPUT IMPEDENCE I_{GSS}= 100pA MAXIMUM	
LOW CAPACITANCE C_{ISS}= 5pF TYPICAL	
ABSOLUTE MAXIMUM RATINGS @ 25 °C (unless otherwise stated)	
Gate-Drain or Gate-Source Voltage	-25V
Gate Current	10mA
Total Device Dissipation @25°C Ambient (Derate 3.27 mW/°C)	360mW
Operating Temperature Range	-55 to +150 °C



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTICS	SSTJ210			SSTJ211			SSTJ212			UNITS	CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{GSS}	Gate Reverse Current	--	--	-100	--	--	-100	--	--	-100	pA	V_{DS} = 0, V_{GS} = -15V (NOTE 1)	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	--	-3	-2.5	--	-4.5	-4	--	-6	V	V_{DS} = 15V, I_D = 1nA	
BV_{GSS}	Gate-Source Breakdown Voltage	-25	--	--	-25	--	--	-25	--	--		V_{DS} = 0, I_G = -1µA	
I_{DSS}	Drain Saturation Current	2	--	15	7	--	20	15	--	40	mA	V_{DS} = 15V, V_{GS}=0 (NOTE 2)	
I_G	Gate Current	--	-10	--	--	-10	--	--	-10	--	pA	V_{DS} = 10V, I_D=1mA (NOTE 1)	
g_{fs}	Common-Source Forward Transconductance	4,000	--	12,000	6,000	--	12,000	7,000	--	12,000	µmho	V_{DS} = 15V, V_{GS}=0	f=1kHz
g_{os}	Common-Source Output Conductance	--	--	150	--	--	200	--	--	200			
C_{ISS}	Common-Source Input Capacitance	--	4	--	--	4	--	--	4	--	pF		f=1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance	-	1	--	--	1	--	--	1	--			
e_n	Equivalent Short-Circuit Input Noise Voltage	-	10	--	--	10	--	--	10	--	nV√Hz		f=1kHz

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2ms.

LINEAR SYSTEMS

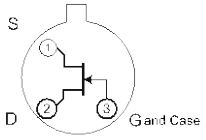
Improved Standard Products®

U/J/SST308 SERIES

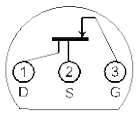
SINGLE N-CHANNEL, HIGH FREQUENCY JFET AMPLIFIER

FEATURES	
Direct Replacement For SILICONIX U/J/SST308 SERIES	
OUTSTANDING HIGH FREQUENCY GAIN	G_{pg} = 11.5dB
LOW HIGH FREQUENCY NOISE	NF = 2.7dB
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (J/SST)[4]	350mW
Continuous Power Dissipation (U)[5]	500mW
Maximum Currents	
Gate Current (J/SST)	10mA
Gate Current (U)	20mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V

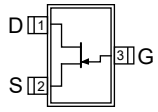
U SERIES
TO-18
TOP VIEW



J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNIT	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage		-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		1.15		I_G = 10mA, V_{DS} = 0V
I_G	Gate Operating Current			-15		pA	V_{DG} = 9V, I_D = 10mA
$r_{DS(on)}$	Drain to Source On Resistance			35		Ω	V_{GS} = 0V, I_D = 1mA
e_n	Equivalent Noise Voltage			6		nV/√Hz	V_{DS} = 10V, I_D = 10mA, *f* = 100Hz
NF	Noise Figure	*f* = 105MHz		1.5		dB	V_{DS} = 10V, I_D = 10mA
		f = 450MHz		2.7			
G_{pg}	Power Gain[2]	*f* = 105MHz		16			
		f = 450MHz		11.5			
g_{fg}	Forward Transconductance	*f* = 105MHz		14		mS	
		f = 450MHz		13			
g_{og}	Output Conductance	*f* = 105MHz		0.16			
		f = 450MHz		0.55			
IGSS	Gate Reverse Current				-1	nA	V_{GS} = -15V, V_{DS} = 0V

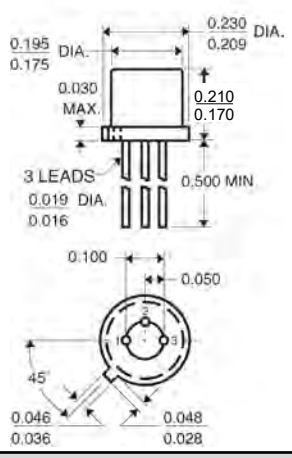
SPECIFIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST308		J/SST309		J/SST310		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-6.5	-1	-4	-2	-6.5	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Source to Drain Saturation Current[3]		12	75	12	30	24	75	mA	V_{DS} = 10V, V_{GS} = 0V
C_{iss}	Input Capacitance	4							pF	V_{DS} = 10V, V_{GS} = -10V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	1.9								
g_{fs}	Forward Transconductance	14	8		10		8		mS	V_{DS} = 10V, I_D = 10mA *f* = 1kHz
g_{os}	Output Conductance	110		250		250		250	µS	

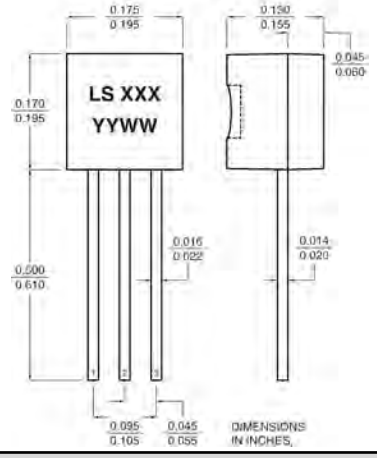
SPECIFIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	U308		U309		U310		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-6.5	-1	-4	-2.5	-6.5	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Source to Drain Saturation Current[3]		12	75	12	30	24	75	mA	V_{DS} = 10V, V_{GS} = 0V
C_{iss}	Input Capacitance	4		5		5		5	pF	V_{DS} = 10V, V_{GS} = -10V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	1.9		2.5		2.5		2.5		
g_{fs}	Forward Transconductance	14	10		10		10		mS	V_{DS} = 10V, I_D = 10mA *f* = 1kHz
g_{os}	Output Conductance	110		250		250		250	µS	

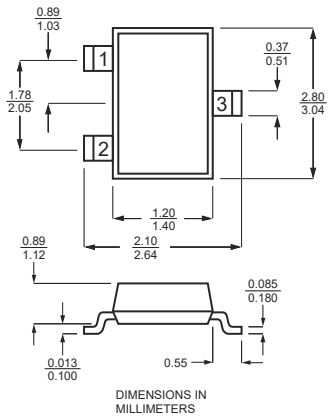
TO-18



TO-92



SOT-23



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Measured at optimum input noise match
3. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
4. Derate 2.8mW/ºC above 25ºC
5. Derate 4mW/ºC above 25ºC

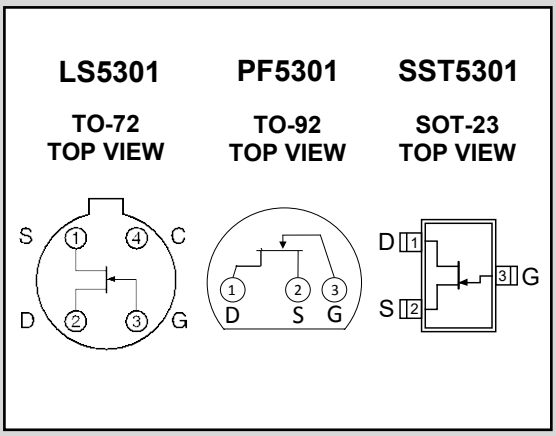
LINEAR SYSTEMS

Improved Standard Products®

LS5301/PF5301/ SST5301

VERY HIGH INPUT IMPEDANCE N-CHANNEL JFET AMPLIFIER

Features	
Replacement for LF5301, PF5301	
High Input Impedance	I_G >1 GΩ
High Gain	g_{fs} > 70 µS
Absolute Maximum Ratings[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures (°C)	
Storage Temperature	-55 to 150°C
Operating Junction Temperature	-55 to 135°C
Maximum Power Dissipation @TA = 25°C	**300mW**
Derate LS5301	2.0mW/°C
Derate PF & SST5301	2.8mW/°C
Maximum Forward Current	**50mA**
Maximum Gate to Drain Voltage	**-30V**
Maximum Gate to Source Voltage	**-30V**



Static Electrical Characteristics @ TA = 25°C (unless otherwise stated)

Symbol	Characteristic			TYP	Max	Unit	Conditions
BV_{GSS}	Gate to Source Breakdown Voltage		-30			V	V_{DS} = 0V, I_D = -1µA
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-0.6		-3.0		V_{DS} = 10V, I_D = 1nA
I_{GSS}	Gate Leakage Current	LS5301			-1	pA	V_{DS} = 15V, V_{GS} = 0V
		PF5301			-5		
		SST5301			-10		
I_G	Gate Operating Current			-0.04			V_{DG} = 6V, I_D = 5µA
I_{DSS}	Drain to Source Saturation Current		30		500	µA	V_{DS} = 10V, V_{GS} = 0V
g_{fs}	Forward Transconductance		70		500	µS	V_{DS} = 10V, V_{GS} = 0V, *f* = 1kHz
C_{iss}	Input Capacitance				3	pF	V_{DS} = 10V, V_{GS} = 0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance				1.5		
e_n	Equivalent Noise Voltage			45	150	nV/√Hz	V_{DG} = 10V, I_D = 50µA, *f* = 100Hz

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Derate PF series 2.8mW/° C when TA>25° C. Derate LS series 2.0mW°C when TA>25° C
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicated electrical polarity only.

LINEAR SYSTEMS

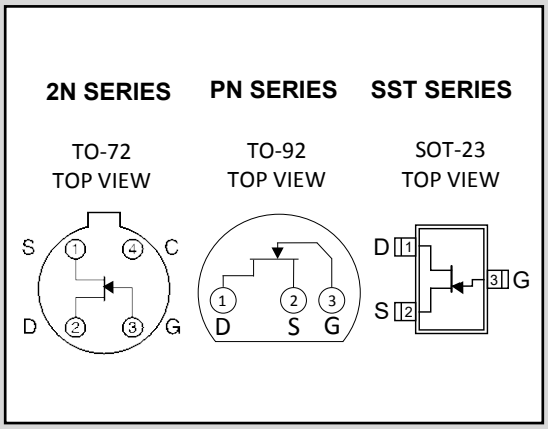
Improved Standard Products®

2N/PN/SST 4117, 4118, 4119

ULTRA-HIGH INPUT IMPEDANCE N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW POWER	I_{DSS}<600 µA (2N4117A)
MINIMUM CIRCUIT LOADING	I_{GSS}<1 pA (2N4117A Series)

ABSOLUTE MAXIMUM RATINGS (NOTE 3) @ 25°C (unless otherwise noted)	
Gate-Source or Gate-Drain Voltage	-40V
Gate-Current	50mA
Total Device Dissipation (Derate 2mW/ºC above 25ºC)	300mW
Storage Temperature Range	-55ºC to+150ºC
Lead Temperature (1/16" from case for 10 seconds)	300ºC



ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

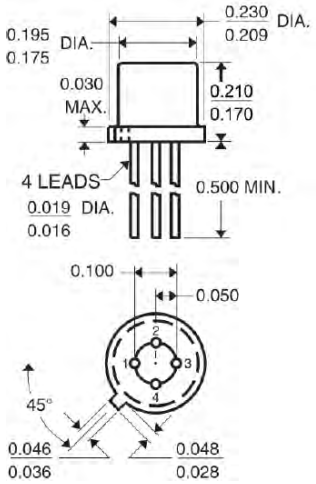
SYMBOL	CHARACTERISTIC	4117 MIN	4117 MAX	4118 MIN	4118 MAX	4119 MIN	4119 MAX	UNITS	CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	-40	--	-40	--	-40	--	V	I_G =-1µA V_{DS}=0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} =10V I_D=1nA	
I_{DSS}	Saturation Drain Current (NOTE 2)	0.03	0.60	0.08	0.60	0.20	0.80	mA	V_{DS} =10V V_{GS}=0	
I_{GSS}	Gate Reverse Current 2N4117A, 2N4118A, 2N4119A	--	-1	--	-1	--	-1	pA	V_{GS} =-20V V_{DS}=0	
		--	-2.5	--	-2.5	--	-2.5	nA		150ºC
	PN4117, PN4118, PN4119 SST4117, SST4118, SST4119	--	-10	--	-10	--	-10	pA	V_{GS} =-10V V_{DS}=0	
		--	-25	--	-25	--	-25	nA		150ºC
g_{fs}	Common-Source Forward Transconductance	70	450	80	650	100	700	µS	V_{DS} =10V V_{GS}=0	f=1kHz
g_{os}	Common-Source Output Conductance	--	3	--	5	--	10			
C_{iss}	Common-Source Input Capacitance (NOTE 4)	--	3	--	3	--	3	pF		f=1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance (NOTE 4)	--	1.5	--	1.5	--	1.5			

STANDARD PACKAGE DIMENSIONS:

2N4117A, 2N4118A, 2N4119A

TO-72

Three Lead

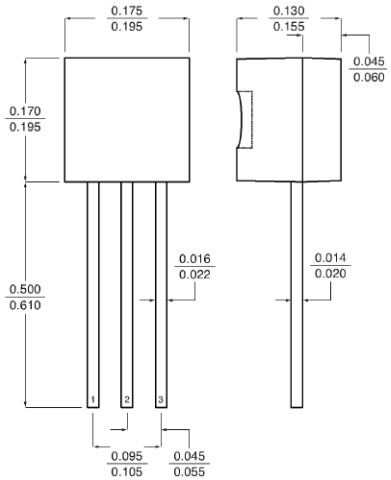


*Dimensions in inches

PN4117, PN4118, PN4119

TO-92

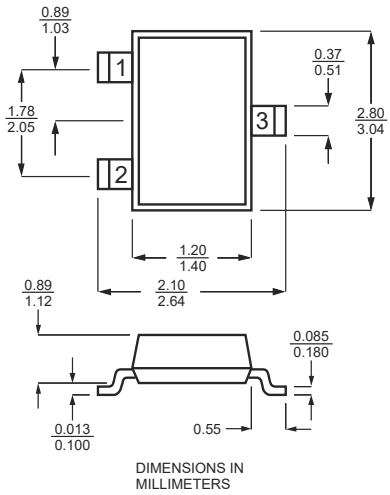
Three Lead



SST4117, SST4118, SST4119

SOT-23

Three Lead



NOTES:

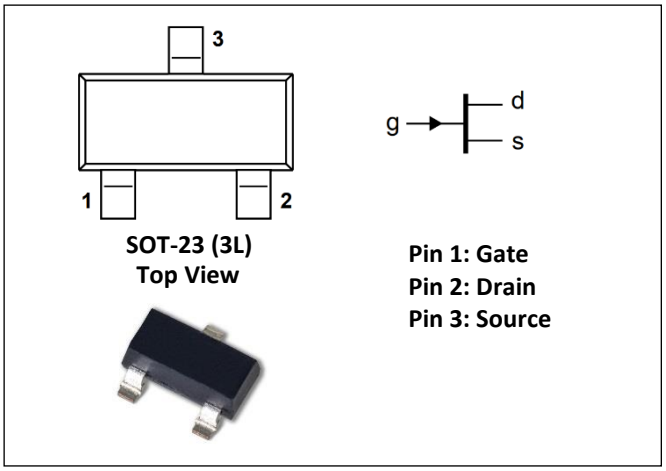
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)
3. Absolute maximum ratings are limiting values above which serviceability may be impaired.
4. Not production tested, guaranteed by design.

LSBF510

High Gain, Single N-Channel JFET Amplifier

General Purpose, Low-Noise, Low-Cost, Single N-Channel JFET, Replacement for the BF510

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 30V
Gate to Drain	V_{GDS} = 30V



Features

- Low Cutoff Voltage: <2.5V
- High Input Impedance
- Very Low Noise
- High Gain: AV = 80 @ 20 µA
- Reverse Gate to Source and Drain Voltage ≥| -30V

Benefits

- Low Cost
- Excellent Low Power Supply Operation
- Power Supply: Down to 2.5V
- Low Signal Loss/System Error
- High System Sensitivity
- High Quality Low-Level Signal

Applications

- High-Gain, Low Noise Amplifiers
- Low-Current, Low-Voltage
- Battery-Powered Amplifiers
- Infrared Detector Amplifiers
- Ultra-High Input Impedance Pre-Amplifiers

Description

The LSBF510 is a low-cost N-Channel JFET. Features include low leakage, very low noise, low cutoff voltage ($V_{GS(off)} \leq 2.5V$) and high Gain (A_V = 80 V/V) for use with low-level power supplies. The LSBF510 is excellent for battery powered equipment and low current amplifiers. The TO-236 (SOT-23) package provides surface-mount capability. The LSBF510 is available in tape-and-reel for automated assembly and in die form for automated assembly.

Electrical Characteristics @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-30			V	I_G = -1µA, V_{DS} = 0.0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3		-2.5		V_{DS} = 15V, I_D = 10nA
I_{DSS}	Drain to Source Saturation Current[2]	0.2		3.0	mA	V_{DS} = 15V, V_{GS} = 0.0V
I_{GSS}	Gate Reverse Current			-200	pA	V_{GS} = -20V, V_{DS} = 0.0V
I_G	Gate Operating Current		-2			V_{DG} = 10V, I_D = 0.1mA
$I_{D(off)}$	Drain Cutoff Current		2			V_{DS} = 15V, V_{GS} = 5.0V
g_{fs}	Forward Transconductance	0.5			mS	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1kHz
C_{iss}	Input Capacitance			4.5	pF	V_{DS} = 15V, V_{GS} = 0.0V, *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance		1.3			
e_n	Noise Voltage		3.0		nV/√Hz	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz

Typical Characteristics

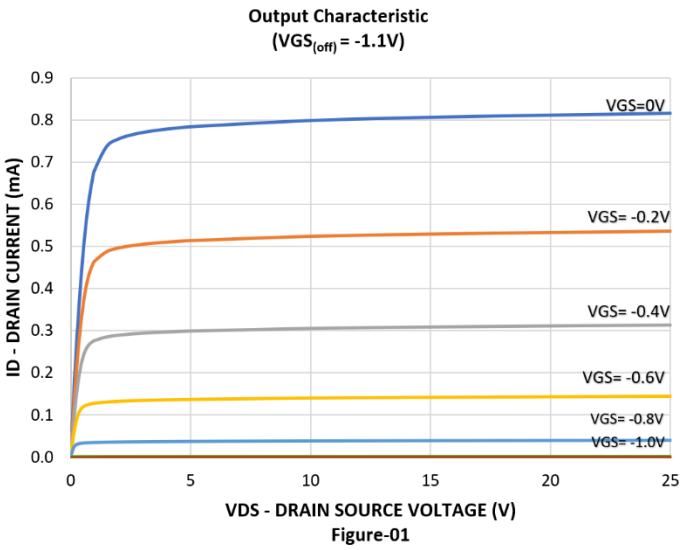


Figure-01

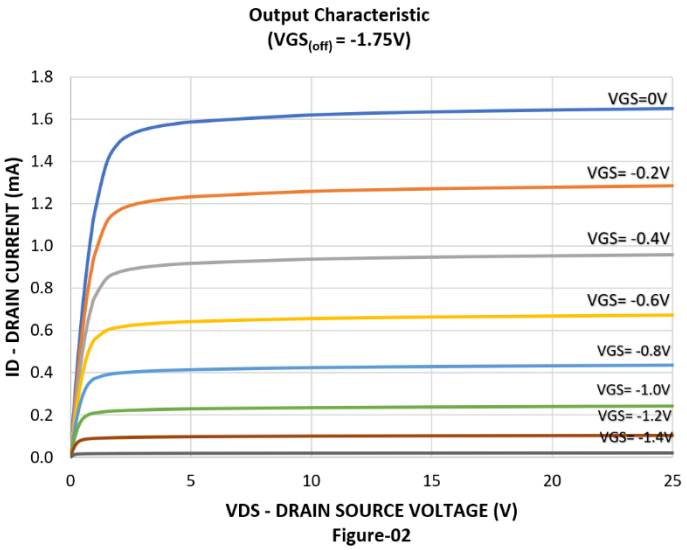


Figure-02

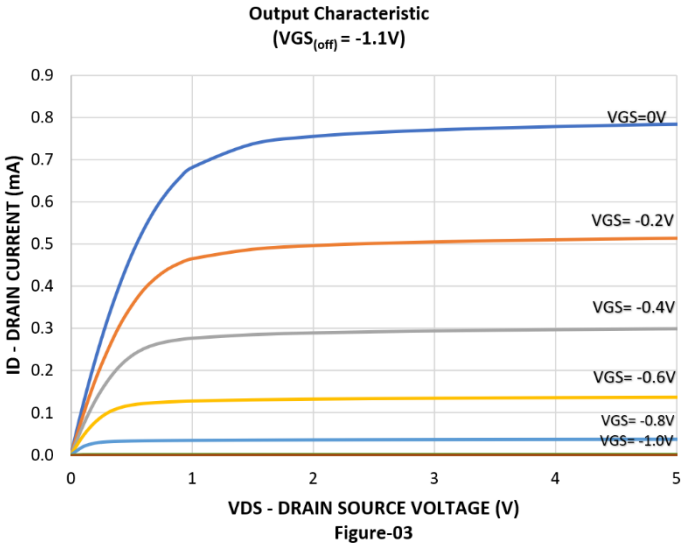


Figure-03

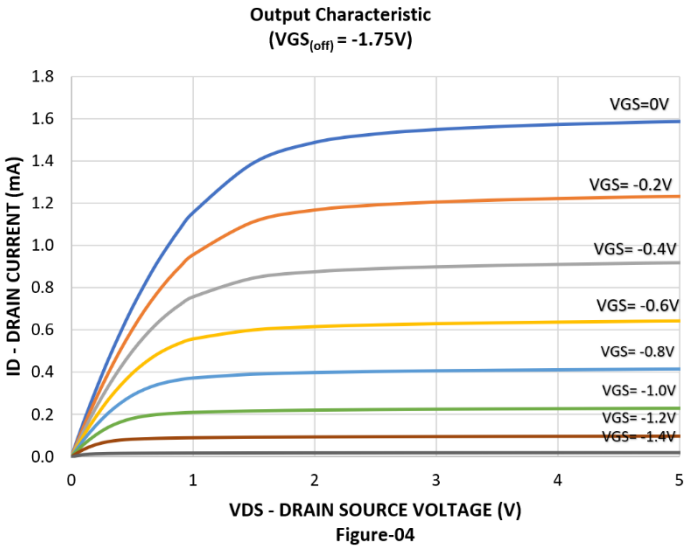


Figure-04

Typical Characteristics Continued

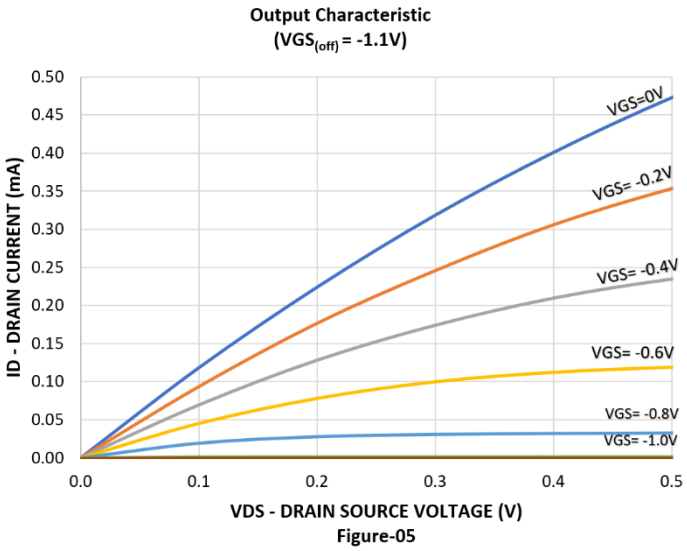


Figure-05

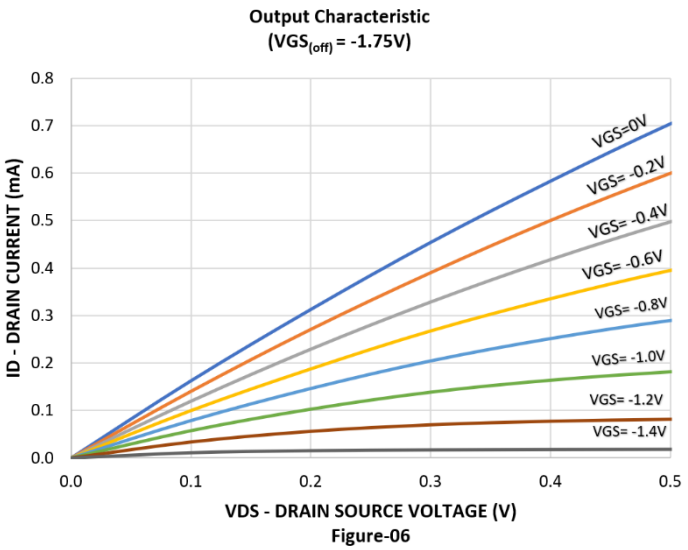


Figure-06

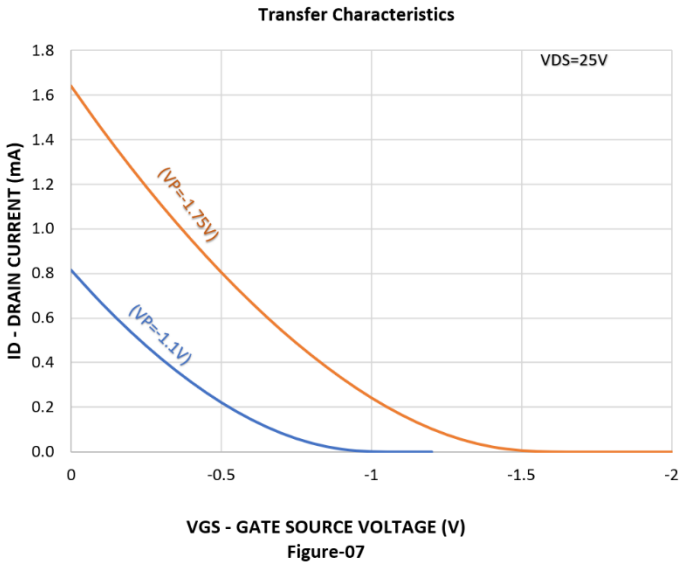


Figure-07

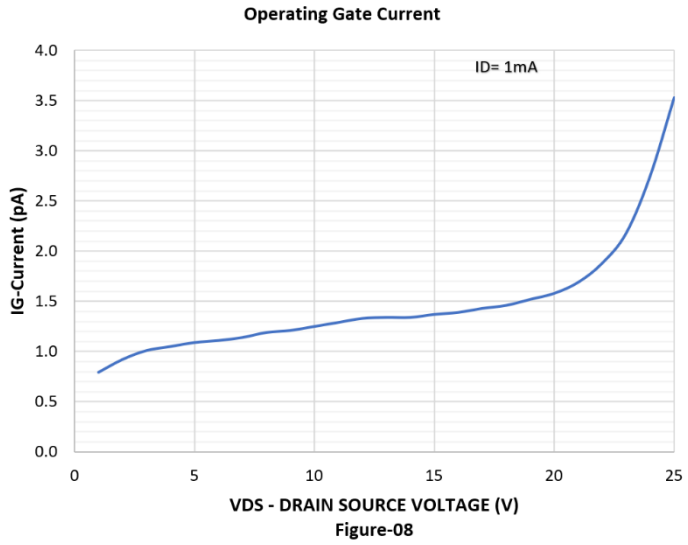


Figure-08

Typical Characteristics Continued

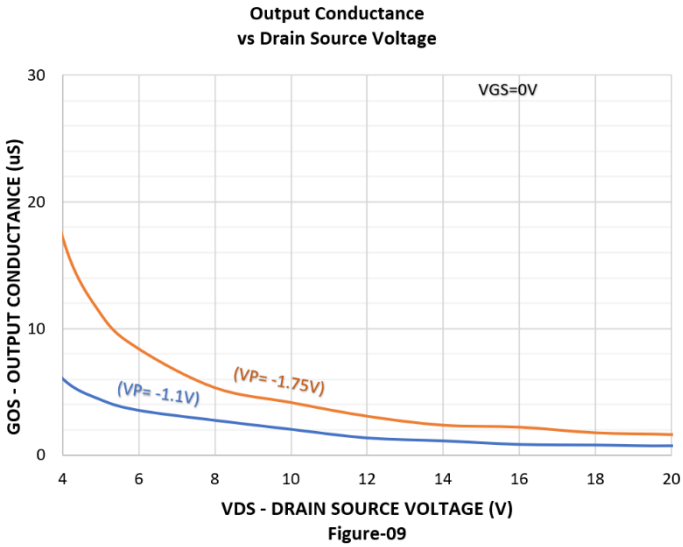


Figure-09

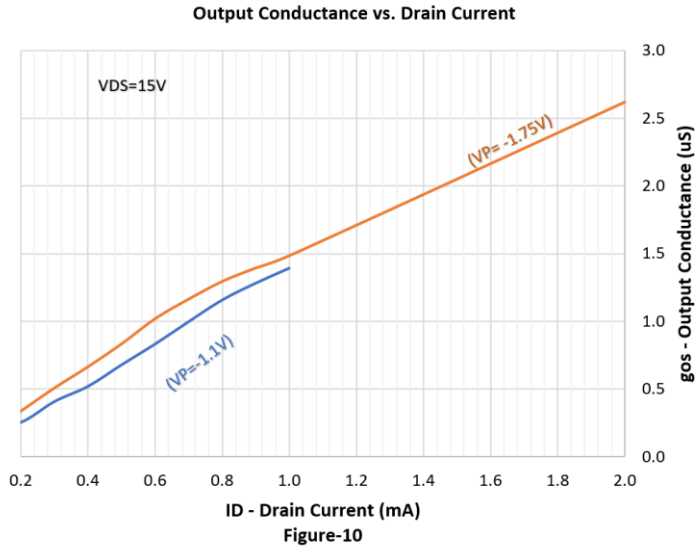


Figure-10

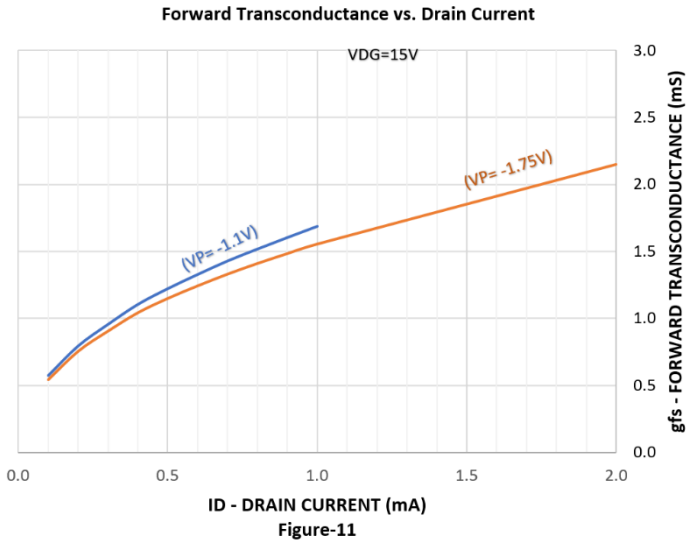


Figure-11

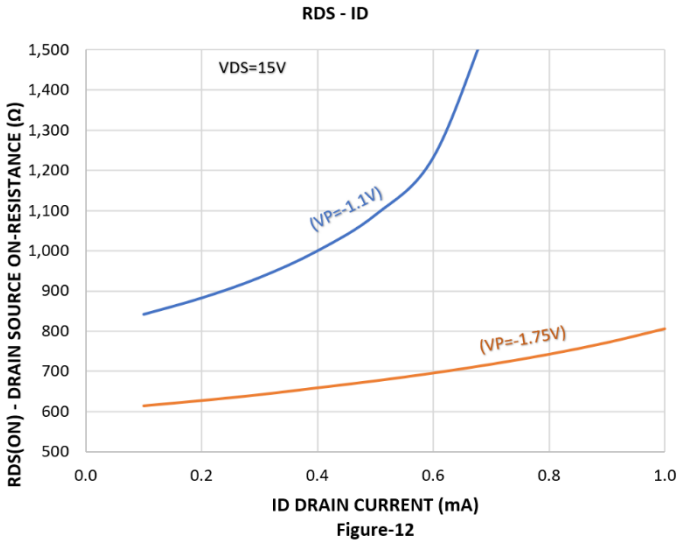
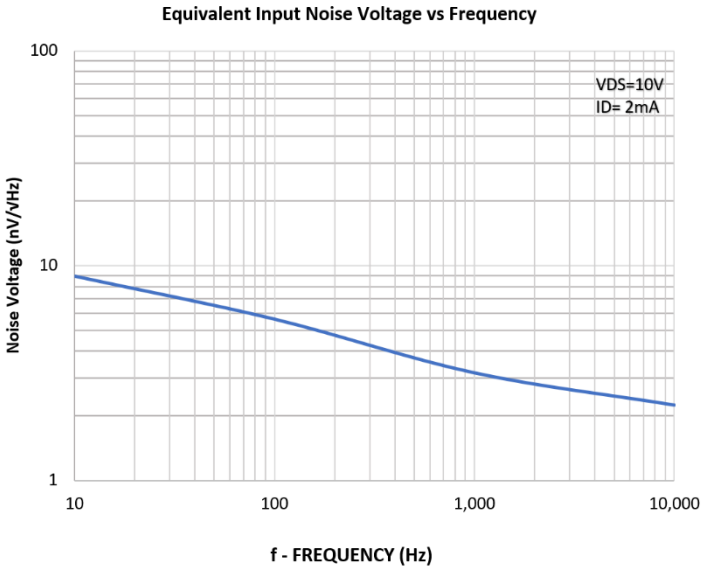


Figure-12

Typical Characteristics Continued



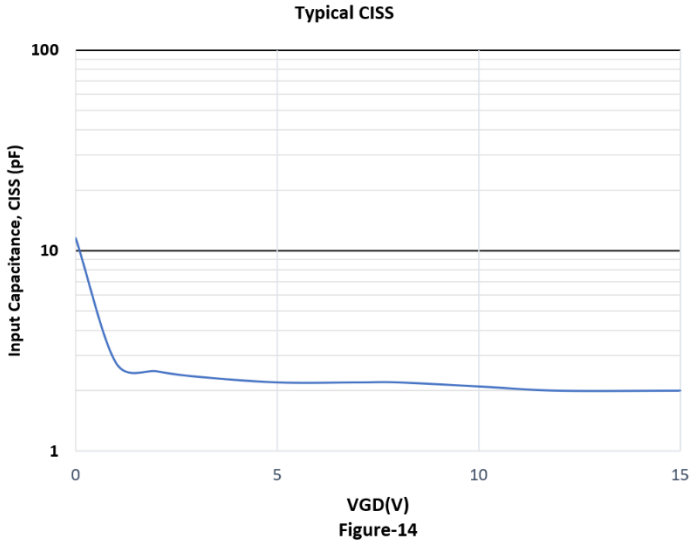
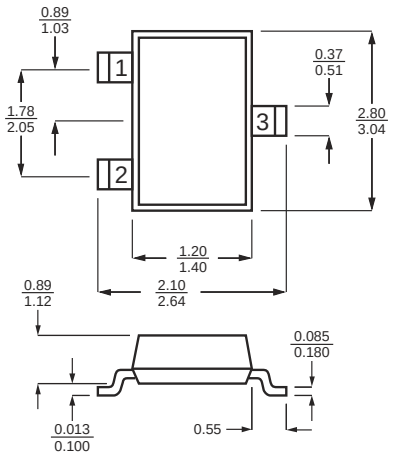


Figure-14

Package Dimensions

SOT-23 3 Lead



DIMENSIONS IN MILLIMETERS

Ordering Information

STANDARD PART CALL-OUT
LSBF510 SOT-23 3L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LSBF510 SOT-23 3L RoHS SELXXXX

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

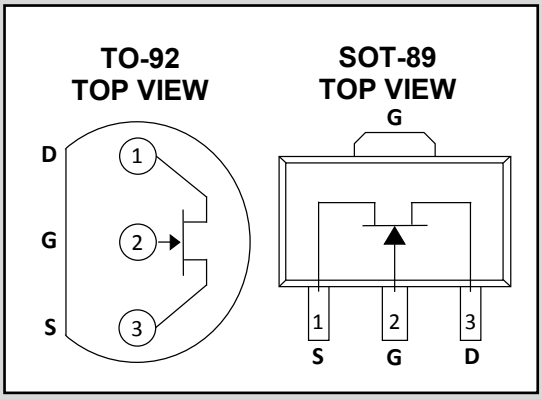
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS190

GENERAL PURPOSE SINGLE N-CHANNEL JFET AMPLIFIER

FEATURES	
HIGH BREAKDOWN VOLTAGE	BV_{GSS}=40V max
HIGH GAIN	G_{fs}=22mS (typ)
HIGH INPUT IMPEDENCE	I_G= -500pA max
LOW CAPACITANCE	20pF (typ)
ABSOLUTE MAXIMUM RATINGS[1] TA = 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation (TO-92)	400mW[4]
Continuous Power Dissipation (SOT-89)	1.4W[5, 6]
Maximum Currents	
Gate Forward Current	$I_{G(F)}$= 10mA
Maximum Voltages	
Gate to Source	V_{GS} = 40V
Gate to Drain	V_{GD} = 40V



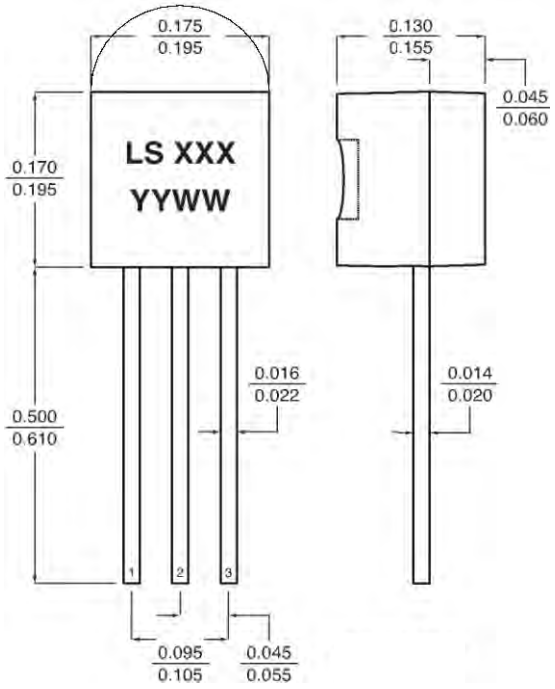
*For equivalent monolithic dual, see LSK589

ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	V_{DS} = 0, I_D = 100µA
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-0.2		-2	V	V_{DS} = 10V, I_D = 1nA
V_{GS}	Gate to Source Operating Voltage		-0.5		V	V_{DS} = 10V, I_D = 1mA
I_{DSS}	Drain to Source Saturation Current	2.6		30	mA	V_{DS} = 10V, V_{GS} = 0
I_G	Gate Operating Current			-0.5	nA	V_{DG} = 10V, I_D = 1mA
I_{GSS}	Gate to Source Leakage Current			-1	nA	V_{GS} = -10V, V_{DS} = 0
G_{fS}	Full Conduction Transconductance		22		mS	V_{GD} = 10V, V_{GS} = 0, *f* = 1kHz
G_{fS}	Typical Conduction Transconductance		10		mS	V_{DG} = 15V, I_D = 1mA
$R_{DS(on)}$	Drain to Source on Resistance		75	150	Ω	V_{GS} = 0V, I_D = -1mA
C_{ISS}	Common Source Input Capacitance		20		pF	V_{DS} = 15V, I_D = 100µA, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		5		pF	

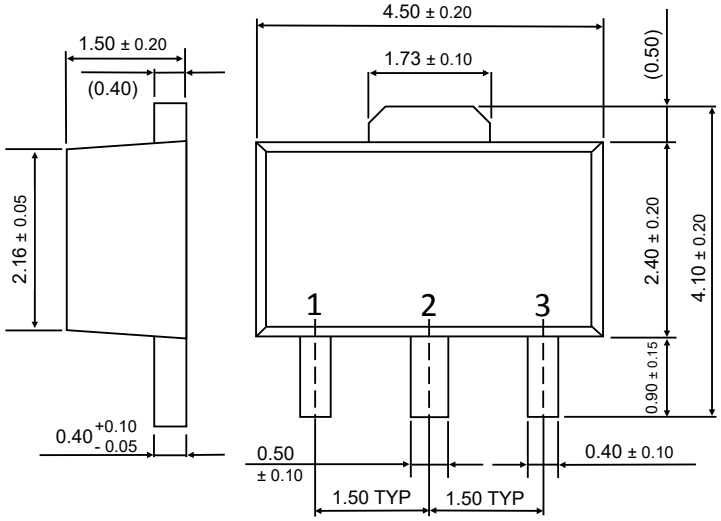
Standard Package Dimensions:

TO-92



Dimensions in inches

SOT-89



Dimensions in millimeters

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 2.8mW/ºC above TA = 25ºC
4. Mounted on FR5 board, 25mm x 25mm x 1.57mm
5. Derate by 25mW/ºC above 25ºC
6. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

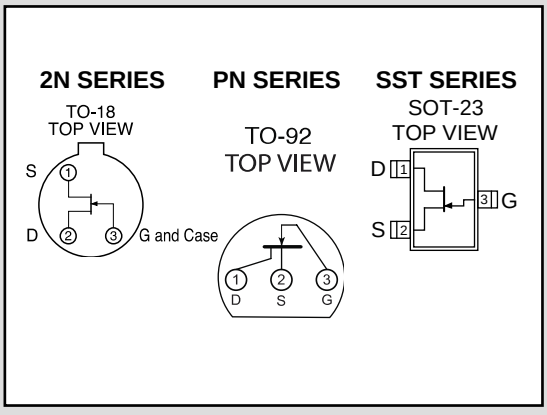
LINEAR SYSTEMS

Quality Through Innovation Since 1987

2N/PN/SST4391 SERIES

SINGLE N-CHANNEL JFET SWITCH

FEATURES	
Replacement for Siliconix 2N/PN/SST4391, 4292, & 4393	
LOW ON RESISTANCE	$r_{DS(on)} \leq 30\Omega$
FAST SWITCHING	$t_{ON} \leq 15ns$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature (2N)	-65 to 200°C
Storage Temperature (PN/SST)	-55 to 150°C
Junction Operating Temperature (2N)	-55 to 200°C
Junction Operating Temperature (PN/SST)	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (2N)@Tc=25°C	1800mW[3]
Continuous Power Dissipation (PN/SST)	350mW[4]
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain or Source (2N/PN)	-40V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	2N/PN/SST		-40		-40		-40		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	2N/PN		-4	-10	-2	-5	-0.5	-3		V_{DS} = 20V, I_D = 1nA
		SST		-4	-10	-2	-5	-0.5	-3		V_{DS} = 15V, I_D = 10nA
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		1		1		1		I_G = 1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage		0.25						0.4		V_{GS} = 0V, I_D = 3mA
			0.3				0.4				V_{GS} = 0V, I_D = 6mA
			0.35		0.4						V_{GS} = 0V, I_D = 12mA
I_{DSS}	Drain to Source Saturation Current[2]	2N		50	165	25	150	5	125	mA	V_{DS} = 20V, V_{GS} = 0V
		PN		50	165	25	150	5	125		
		SST		50		25		5			
I_{GSS}	Gate Leakage Current	2N/SST	-5		-100		-100		-100	pA	V_{GS} = -20V, V_{DS} = 0V
		PN	-5		-1000		-1000		-1000		
I_G	Gate Operating Current		-5								V_{DG} = 15V, I_D = 10mA

STATIC ELECTRICAL CHARACTERISTICS CONT. @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
$I_{D(off)}$	Drain Cutoff Current	2N	5						100	pA	V_{DS} = 20V, V_{GS} = -5V
			5				100				V_{DS} = 20V, V_{GS} = -7V
			5		100						V_{DS} = 20V, V_{GS} = -12V
		PN	5						1000		V_{DS} = 20V, V_{GS} = -5V
			5				1000				V_{DS} = 20V, V_{GS} = -7V
			5		1000						V_{DS} = 20V, V_{GS} = -12V
		SST	5		100		100		100		V_{DS} = 10V, V_{GS} = -12V
$r_{DS(on)}$	Drain to Source On Resistance				30		60		100	Ω	V_{GS} = 0V, I_D = 1mA

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance		6							mS	V_{DS} = 20V, I_D = 1mA *f* = 1kHz
g_{os}	Output Conductance		25							µS	
$r_{ds(on)}$	Drain to Source On Resistance				30		60		100	Ω	V_{GS} = 0V, I_D = 1mA
C_{iss}	Input Capacitance	2N	12		14		14		14	pF	V_{DS} = 20V, V_{GS} = 0V *f* = 1MHz
		PN	12		16		16		16		
		SST	13								
C_{rss}	Reverse Transfer Capacitance	2N	3.3						3.5		V_{DS} = 0V, V_{GS} = -5V *f* = 1MHz
		PN	3.5						5		
		SST	3.6								
		2N	3.2				3.5				V_{DS} = 0V, V_{GS} = -7V *f* = 1MHz
		PN	3.4				5				
		SST	3.5								
		2N	2.8		3.5						V_{DS} = 0V, V_{GS} = -12V *f* = 1MHz
		PN	3.0		5						
		SST	3.1								
e_n	Equivalent Input Noise Voltage		3							nV/√Hz	V_{DS} = 10V, I_D = 10mA *f* = 1kHz

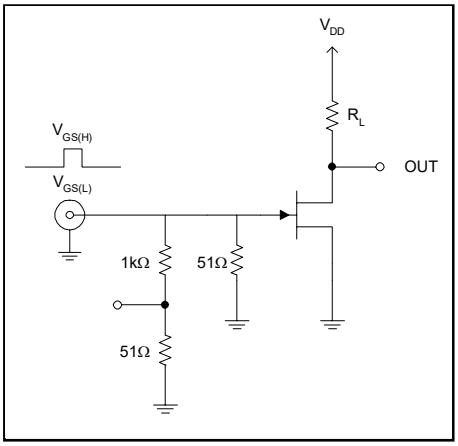
SWITCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC		TYP	4391		4392		4393		UNIT	CONDITIONS
				MIN	MAX	MIN	MAX	MIN	MAX		
$t_{d(on)}$	Turn On Time	2N/PN	2		15		15		15	ns	V_{DD} = 10V, $V_{GS(H)}$ = 0V
		SST	2								
t_r		2N/PN	2		5		5		5		
		SST	2								
$t_{d(off)}$	Turn Off Time	2N/PN	6		20		35		50		
		SST	6								
t_f		2N/PN	13		15		20		30		
		SST	13								

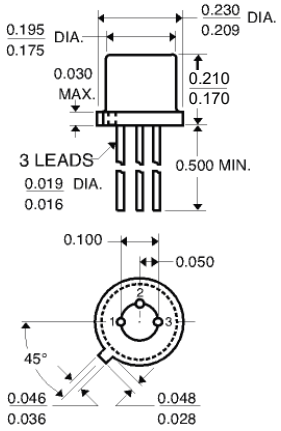
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	4391	4392	4393
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

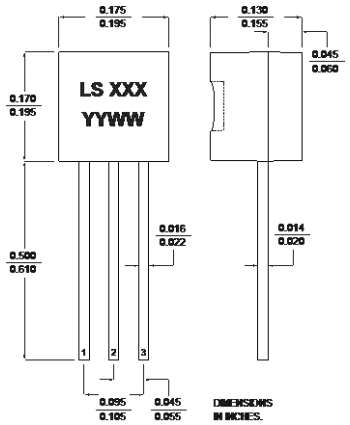
SWITCHING TEST CIRCUIT



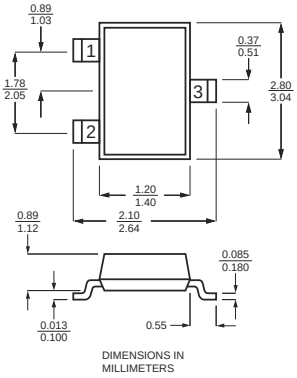
TO-18 * Three Lead



TO-92 *



SOT-23



*Dimensions in inches

NOTES :

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 10mW/°C above 25°C
4. Derate 2.8mW/°C above 25°C

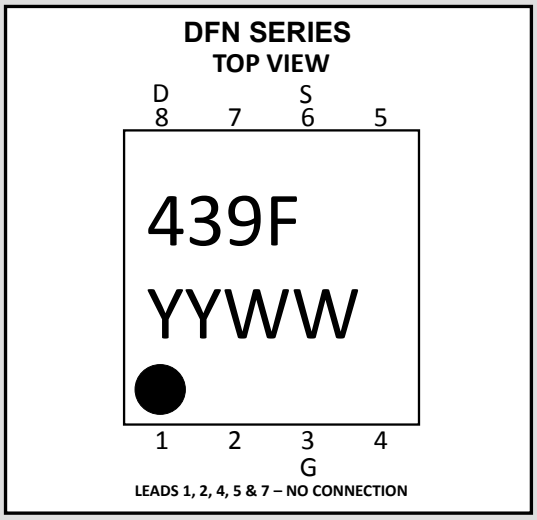
LINEAR SYSTEMS

Improved Standard Products®

4391DFN SERIES

MINIATURE/NON-MAGNETIC 8-PIN DFN PACKAGE N-CHANNEL JFET SWITCH

FEATURES	
LOW ON RESISTANCE	$r_{DS(on)} \leq 30\Omega$
FAST SWITCHING	$t_{ON} \leq 15ns$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	300mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain or Source	-40V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		-40		-40		-40		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-4	-10	-2	-5	-0.5	-3		V_{DS} = 15V, I_D = 10nA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7		1		1		1		I_G = 1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage	0.25						0.4		V_{GS} = 0V, I_D = 3mA
		0.3				0.4				V_{GS} = 0V, I_D = 6mA
		0.35		0.4						V_{GS} = 0V, I_D = 12mA
I_{DSS}	Drain to Source Saturation Current[2]		50		25		5		mA	V_{DS} = 20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-.005		-1.0		-1.0		-1.0	nA	V_{GS} = -20V, V_{DS} = 0V
I_G	Gate Operating Current	-.005								V_{DG} = 15V, I_D = 10mA
$I_{D(off)}$	Drain Cutoff Current	.005		1.0		1.0		1.0	nA	V_{DS} = 10V, V_{GS} = -12V
$r_{DS(on)}$	Drain to Source On Resistance			30		60		100	Ω	V_{GS} = 0V, I_D = 1mA

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	6							mS	V_{DS} = 20V, I_D = 1mA
g_{os}	Output Conductance	25							µS	*f* = 1kHz
C_{iss}	Input Capacitance	13							pF	V_{DS} = 20V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	3.6								V_{DS} = 0V, V_{GS} = -5V *f* = 1MHz
		3.5								V_{DS} = 0V, V_{GS} = -7V *f* = 1MHz
		3.1								V_{DS} = 0V, V_{GS} = -12V *f* = 1MHz
e_n	Equivalent Input Noise Voltage	3							nV/√Hz	V_{DS} = 10V, I_D = 10mA *f* = 1kHz

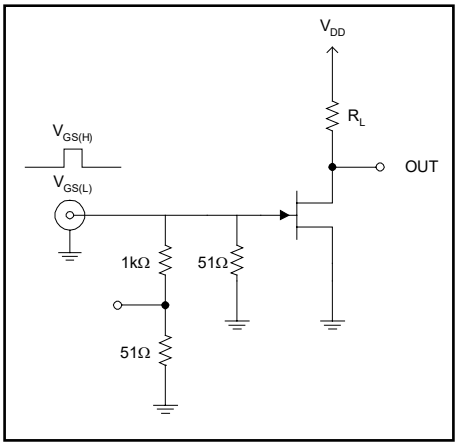
SWITCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	4391DFN		4392DFN		4393DFN		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$t_{d(on)}$	Turn On Time	2							ns	V_{DD} = 10V, $V_{GS(H)}$ = 0V
t_r		2								
$t_{d(off)}$	Turn Off Time	6								
t_f		13								

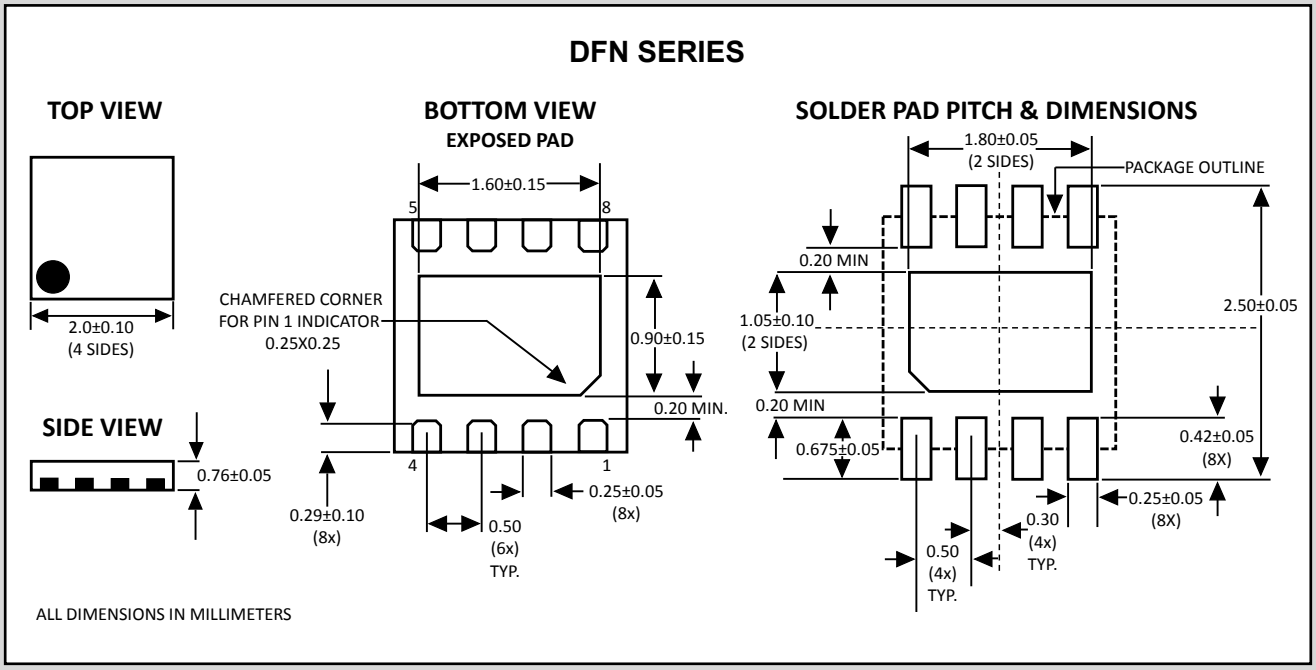
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	4391DFN	4392DFN	4393DFN
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

SWITCHING TEST CIRCUIT



Standard Package Dimensions:



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 2.8mW/°C above 25°C

LINEAR SYSTEMS

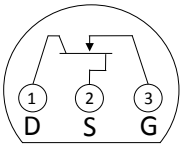
Improved Standard Products®

J/SST111 SERIES

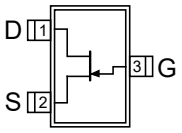
SINGLE N-CHANNEL JFET SWITCH

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX J/SST111 SERIES	
LOW GATE LEAKAGE CURRENT	5pA
FAST SWITCHING	4ns
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation (J)[3]	360mW
Continuous Power Dissipation (SST)[3]	350mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-35V
Gate to Source	-35V

J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST111		J/SST112		J/SST113		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		-35		-35		-35		V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-3	-10	-1	-5		-3		V_{DS} = 5V, I_D = 1µA
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7								I_G = 1mA, V_{DS} = 0V
I_{DSS}	Drain to Source Saturation Current[2]		20		5		2		mA	V_{DS} = 15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	-0.005		-1		-1		-1	nA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current	-5							pA	V_{DG} = 15V, I_D = 1.0mA
$I_{D(off)}$	Drain Cutoff Current	0.005		1		1		1	nA	V_{DS} = 5V, V_{GS} = -10V
$r_{DS(on)}$	Drain to Source On Resistance			30		50		100	Ω	V_{GS} = 0V, V_{DS} = 0.1V

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	J/SST111		J/SST112		J/SST113		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	6							mS	V_{DS} = 20V, I_D = 1mA
g_{os}	Output Conductance	25							µS	*f* = 1kHz
$r_{ds(on)}$	Drain to Source On Resistance			30		50		100	Ω	V_{GS} = 0V, I_D = 1mA *f* = 1kHz
C_{iss}	Input Capacitance	7		12		12		12	pF	V_{DS} = 0V, V_{GS} = -10V
C_{rss}	Reverse Transfer Capacitance	3		5		5		5		*f* = 1MHz
e_n	Equivalent Noise Voltage	3							nV/√Hz	V_{DG} = 10V, I_D = 1mA *f* = 1 kHz

SWITCHING CHARACTERISTICS

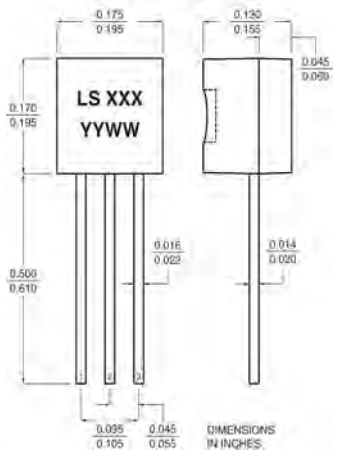
SYM.	CHARACTERISTIC	TYP	UNIT	CONDITIONS
$t_{d(on)}$	Turn On Time	2	ns	V_{DD} = 10V $V_{GS(H)}$ = 0V
t_r		2		
$t_{d(off)}$	Turn Off Time	6		
t_f		15		

SWITCHING CIRCUIT CHARACTERISTICS

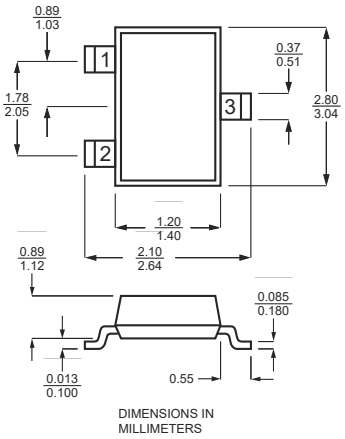
SYM.	J/SST111	J/SST112	J/SST113
$V_{GS(L)}$	-12V	-7V	-5V
R_L	800Ω	1600Ω	3200Ω
$I_{D(on)}$	12mA	6mA	3mA

STANDARD PACKAGE DIMENSIONS:

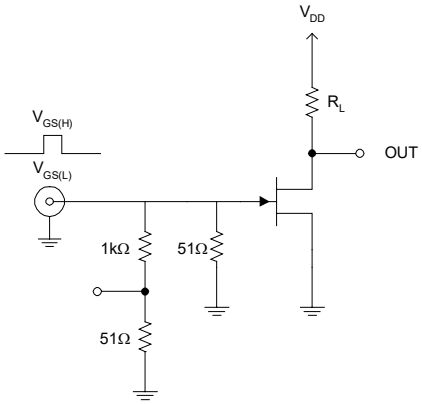
TO-92



SOT-23



SWITCHING TEST CIRCUIT



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. Derate 2.8mW/°C above 25°C

LINEAR SYSTEMS

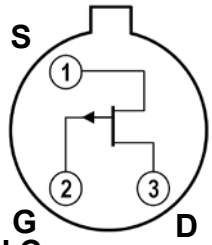
Improved Standard Products®

2N5018 SERIES

SINGLE P-CHANNEL JFET SWITCH

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX 2N5018	
ZERO OFFSET VOLTAGE	
LOW ON RESISTANCE	75Ω
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	500mW
Maximum Currents	
Gate Current	-10mA
Maximum Voltages	
Gate to Drain	30V
Gate to Source	30V

TO-18
TOP VIEW



STATIC ELECTRICAL CHARACERISTICS @25ºC (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5018		2N5019		UNITS	CONDITIONS
			MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		30		30		V	I_G = 1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage			10		5		V_{DS} = -15V, I_D = -1µA
$V_{DS(on)}$	Drain to Source On Voltage			-0.5				V_{GS} = 0V, I_D = -6mA
						-0.5		V_{GS} = 0V, I_D = -3mA
I_{DSS}	Drain to Source Saturation Current[2]		-10		-5		mA	V_{DS} = -20V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current			2		2	nA	V_{GS} = 15V, V_{DS} = 0V
$I_{D(off)}$	Drain Cutoff Current			-10		-10		V_{DS} = -15V, V_{GS} = 12V
						-10	µA	V_{DS} = -15V, V_{GS} = 7V
I_{DGO}	Drain Reverse Current			-2		-2	nA	V_{DG} = -15V, I_S = 0A
$r_{DS(on)}$	Drain to Source On Resistance			75		150	Ω	I_D = -1mA, V_{GS} = 0V

DYNAMIC ELECTRICAL CHARACTERISTICS @25ºC (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5018		2N5019		UNITS	CONDITIONS
			MIN	MAX	MIN	MAX		
$r_{ds(on)}$	Drain to Source On Resistance			75		150	Ω	I_D = -100μA, V_{GS} = 0V *f* = 1kHz
C_{iss}	Input Capacitance			45		45	pF	V_{DS} = -15V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance			10				V_{DS} = 0V, V_{GS} = 12V *f* = 1MHz
						10		V_{DS} = 0V, V_{GS} = 7V *f* = 1MHz

SWITCHING CHARACTERISTICS (max)

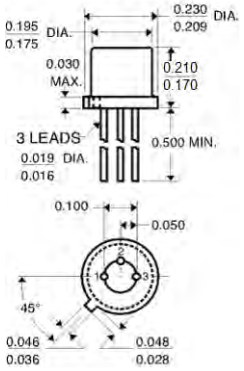
SYM.	CHARACTERISTIC	2N5018	2N5019	UNITS
$t_{d(on)}$	Turn On Time	15	15	ns
t_r		20	75	
$t_{d(off)}$	Turn Off Time	15	25	
t_f		50	100	

SWITCHING CIRCUIT CHARACTERISTICS

SYM.	2N5018	2N5019
V_{DD}	-6V	-6V
V_{GG}	12V	8V
R_L	910Ω	1.8KΩ
R_G	220Ω	390Ω
$I_{D(on)}$	-6mA	-3mA
$V_{GS(H)}$	0V	0V
$V_{GS(L)}$	12V	7V

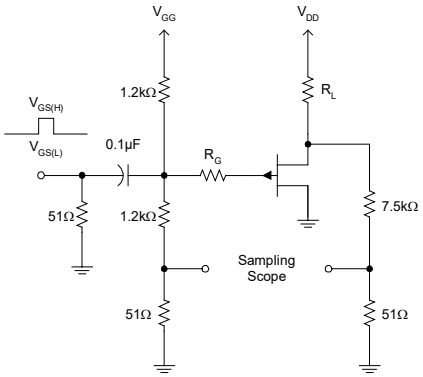
STANDARD PACKAGE DIMENSIONS:

TO-18
Three Lead



Note: All Dimensions in inches

SWITCHING TEST CIRCUIT



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. Derate 3mW/°C above 25°C.

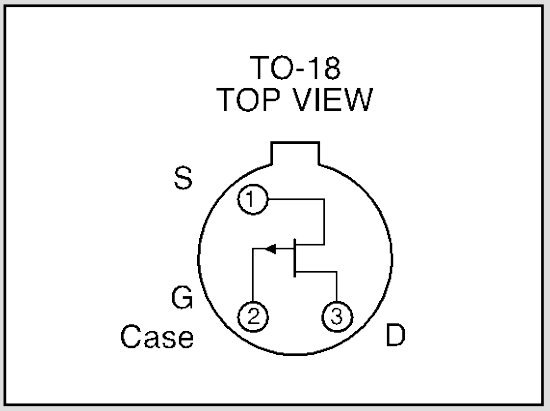
LINEAR SYSTEMS

Improved Standard Products®

2N5114 SERIES

SINGLE P-CHANNEL JFET SWITCH

FEATURES	
REPLACEMENT FOR SILICONIX 2N5114, 2N5115, 2N5116	
LOW ON RESISTANCE	75Ω
LOW CAPACITANCE	6pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	500mW
Maximum Currents	
Gate Current	-50mA
Maximum Voltages	
Gate to Drain	30V
Gate to Source	30V



STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5114		2N5115		2N5116		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage		30		30		30		V	I_G = 1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage		5	10	3	6	1	4		V_{DS} = -15V, I_D = -1nA
$V_{GS(F)}$	Gate to Source Forward Voltage	-0.7		-1		-1		-1		I_G = -1mA, V_{DS} = 0V
$V_{DS(on)}$	Drain to Source On Voltage	-1.0		-1.3						V_{GS} = 0V, I_D = -15mA
		-0.7				-0.8				V_{GS} = 0V, I_D = -7mA
		-0.5						-0.6		V_{GS} = 0V, I_D = -3mA
I_{DSS}	Drain to Source Saturation Current[2]		-30	-195					mA	V_{DS} = -18V, V_{GS} = 0V
					-15	-110	-5	-55		V_{DS} = -15V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	5		500		500		500	pA	V_{GS} = 20V, V_{DS} = 0V
I_G	Gate Operating Current	-5								V_{DG} = -15V, I_D = -1mA
$I_{D(off)}$	Drain Cutoff Current	-10		-500						V_{DS} = -15V, V_{GS} = 12V
		-10				-500				V_{DS} = -15V, V_{GS} = 7V
		-10						-500		V_{DS} = -15V, V_{GS} = 5V
$r_{DS(on)}$	Drain to Source On Resistance			75		100		150	Ω	V_{GS} = 0V, I_D = -1mA

Note: All Min & Max limits are absolute values. Negative signs indicate electrical polarity only.

DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	2N5114		2N5115		2N5116		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g_{fs}	Forward Transconductance	4.5							mS	V_{DS} = -15V, I_D = -1mA *f* = 1kHz
g_{os}	Output Conductance	20							µS	
$r_{ds(on)}$	Drain to Source On Resistance			75		100		150	Ω	V_{GS} = 0V, I_D = -1mA *f* = 1kHz
C_{iss}	Input Capacitance	20		25		25		25	pF	V_{DS} = -15V, V_{GS} = 0V *f* = 1MHz
C_{rss}	Reverse Transfer Capacitance	5		7						V_{DS} = 0V, V_{GS} = 12V *f* = 1MHz
		6				7				V_{DS} = 0V, V_{GS} = 7V *f* = 1MHz
		6						7		V_{DS} = 0V, V_{GS} = 5V *f* = 1MHz
e_n	Equivalent Noise Voltage	20							nV/√Hz	V_{DG} = -10V, I_D = -10mA *f* = 1 kHz

SWITCHING CHARACTERISTICS (max)

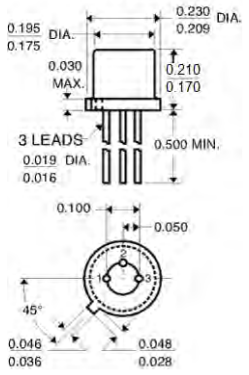
SYM.	CHARACTERISTIC	2N5114	2N5115	2N5116	UNITS
$t_{d(on)}$	Turn On Time	6	10	12	ns
t_r		10	20	30	
$t_{d(off)}$	Turn Off Time	6	8	10	
t_f		15	30	50	

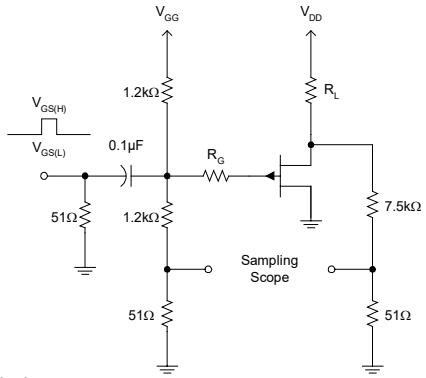
SWITCHING CIRCUIT CHARACTERISTICS

SYM.	2N5114	2N5115	2N5116
V_{DD}	-10V	-6V	-6V
V_{GG}	20V	12V	8V
R_L	430Ω	910Ω	2kΩ
R_G	100Ω	220Ω	390Ω
$I_{D(on)}$	-15mA	-7mA	-3mA
$V_{GS(H)}$	0V	0V	0V
$V_{GS(L)}$	-11V	-7V	-5V

STADARD PACKAGE DIMENSIONS:

TO-18
Three Lead





Note: All Dimensions are in inches

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. Derate 3mW/°C above 25°C.

LINEAR SYSTEMS

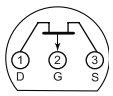
Over 30 Years of Quality Through Innovation

J/SST174 SERIES

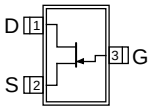
SINGLE P-CHANNEL JFET SWITCH

FEATURES	
Replacement For SILICONIX J/SST174 SERIES	
LOW ON RESISTANCE	$r_{DS(on)} \leq 85\Omega$
LOW GATE OPERATING CURRENT	$I_{D(off)}$ = 10pA
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 135°C
Maximum Power Dissipation	
Continuous Power Dissipation[3]	350mW
Maximum Currents	
Gate Current	I_G = -50mA
Maximum Voltages	
Gate to Drain Voltage	V_{GDS} = 30V
Gate to Source Voltage	V_{GSS} = 30V

J SERIES
TO-92
TOP VIEW



SST SERIES
SOT-23
TOP VIEW



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	30			V	I_G = 1µA, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		-0.7			I_G = -1mA, V_{DS} = 0V
I_{GSS}	Gate Reverse Current		0.01	1	nA	V_{GS} = 20V, V_{DS} = 0V
I_G	Gate Operating Current		0.01			V_{DG} = -15V, I_D = -1mA
$I_{D(off)}$	Drain Cutoff Current		-0.01	-1		V_{DS} = -15V, V_{GS} = 10V

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	J/SST174		J/SST175		J/SST176		J/SST177		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$V_{GS(off)}$	Gate to Source Cutoff Voltage	5	10	3	6	1	4	0.8	2.25	V	V_{DS} = -15V, I_D = -10nA
I_{DSS}	Drain to Source Saturation Current	-20	-195	-7	-90	-2	-55	-1.5	-30	mA	V_{DS} = -15V, V_{GS} = 0V
$r_{DS(on)}$	Drain to Source On Resistance		85		125		250		300	Ω	V_{GS} = 0V, V_{DS} = -0.1V

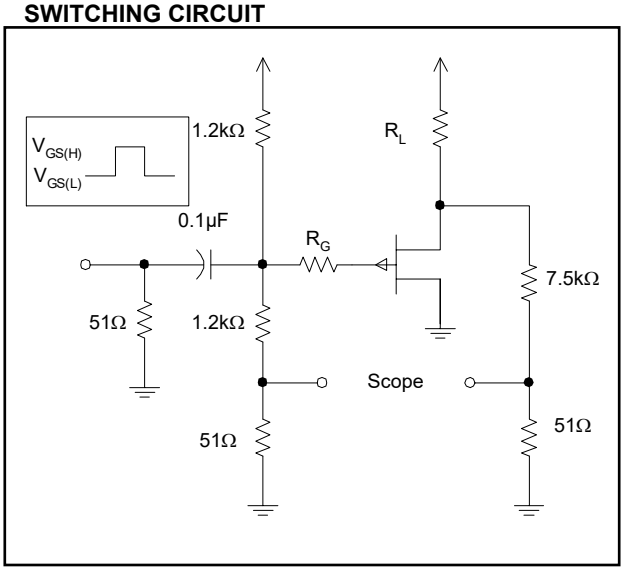
SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	TYP	UNITS	CONDITIONS
$t_{d(on)}$	Turn On Time	10	ns	$V_{GS(L)}$ = 0V $V_{GS(H)}$ = 10V See Switching Circuit
t_r	Turn On Rise Time	15		
$t_{d(off)}$	Turn Off Time	10		
t_f	Turn Off Fall Time	20		

SWITCHING CIRCUIT PARAMETERS

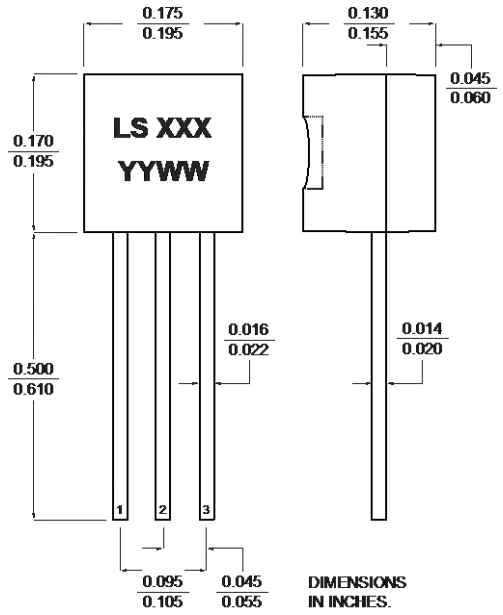
	J/SST174	J/SST175	J/SST176	J/SST177
V_{DD}	-10V	-6V	-6V	-6V
V_{GG}	20V	12V	8V	5V
R_L	560Ω	750Ω	1800Ω	5600Ω
R_G	100Ω	220Ω	390Ω	390Ω
$I_{D(on)}$	-15mA	-7mA	-3mA	-1mA

SWITCHING CIRCUIT

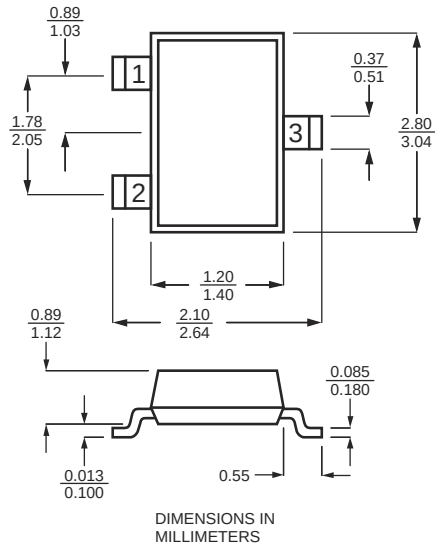


STANDARD PACKAGE DIMENSIONS:

TO-92



SOT-23



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulsed test: $P_W \leq 300\mu S$ Duty Cycle: 3%
3. Derate 2.8mW/°C above 25 °C.

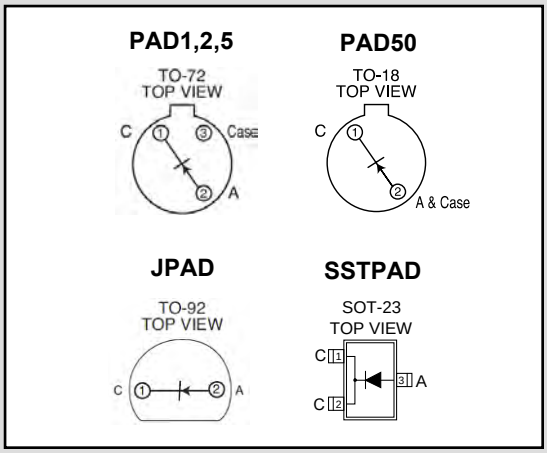
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

PAD SERIES

PICO AMPERE DIODES

FEATURES	
DIRECT REPLACEMENT FOR SILICONIX PAD SERIES	
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq -30V$
REVERSE CAPACITANCE	$C_{rss} \leq 2.0pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation (PAD)	300mW
Continuous Power Dissipation (J/SSTPAD)	350mW
Maximum Currents	
Forward Current (PAD)	50mA
Forward Current (J/SSTPAD)	10mA



COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	ALL PAD	-45			V	I_R = -1µA
		ALL SSTPAD	-30				
		ALL JPAD	-35				
V_F	Forward Voltage			0.8	1.5		I_F = 5mA
C_{rss}	Total Reverse Capacitance	PAD1,5		0.5	0.8	pF	V_R = -5V, *f* = 1MHz
		All Others		1.5	2		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		PAD	JPAD	SSTPAD	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current	PAD1	-1			pA	V_R = -20V
		PAD2	-2				
		(SST/J)PAD5	-5	-5	-5		
		(SST/J)PAD10	-10	-10	-10		
		(SST/J)PAD20	-20	-20	-20		
		(SST/J)PAD50	-50	-50	-50		
		(SST/J)PAD100	-100	-100			
		(SST/J)PAD200		-200			
		(SST/J)PAD500		-500			

1. Derate 2mW/°C above 25°C
2. Derate 2.8mW/°C above 25°C

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by JPADs D_1 and D_2. Common Mode Input voltage limited by JPADs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

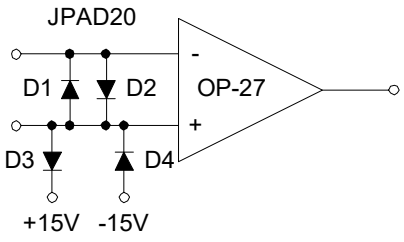
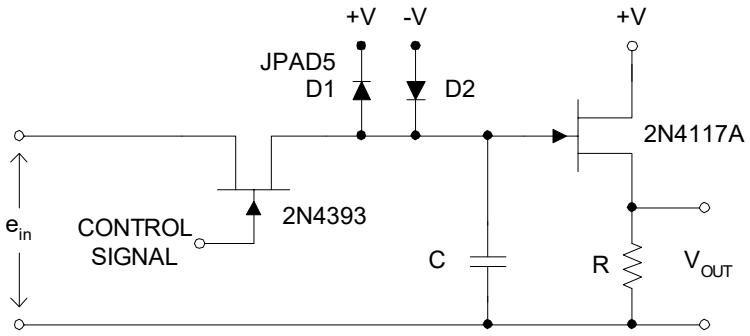
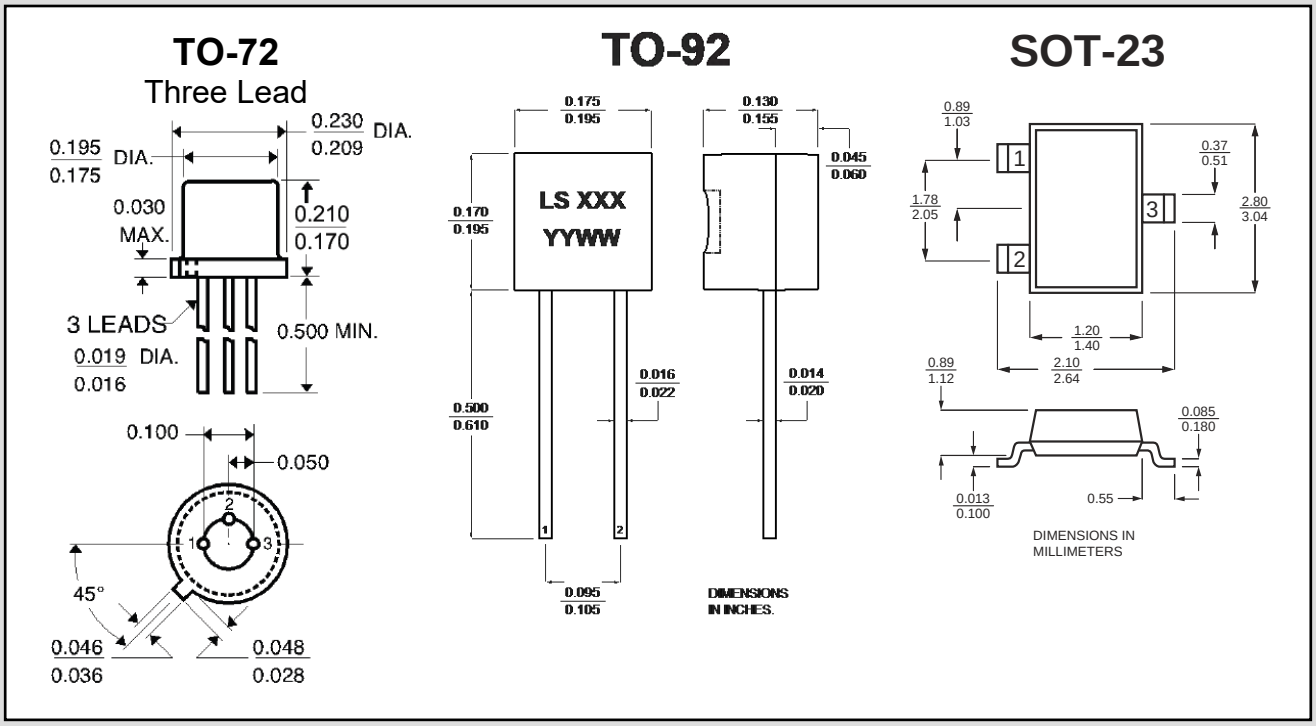


FIGURE 2





NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

LINEAR SYSTEMS

Improved Standard Products®

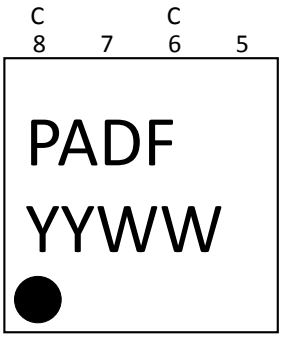
PAD-DFN SERIES

MINIATURE/NON MAGNETIC
8-PIN DFN PACKAGE
LOW LEAKAGE DIODE

FEATURES	
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq -30V$
REVERSE CAPACITANCE	$C_{rss} \leq 2.0pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation[2]	
Continuous Power Dissipation	300mW
Maximum Currents	
Forward Current	10mA

DFN SERIES

TOP VIEW



LEADS 1, 2, 4, 5 & 7 – NO CONNECTION

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	-30			V	I_R = -1µA
V_F	Forward Voltage		0.8	1.5		I_F = 5mA
C_{rss}	Total Reverse Capacitance		1.5		pF	V_R = -5V, *f* = 1MHz

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		TYP	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current	PAD5DFN	-5	pA	V_R = -20V
		PAD50DFN	-50		

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by DFNs D_1 and D_2. Common Mode Input voltage limited by DFNs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. DFN diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

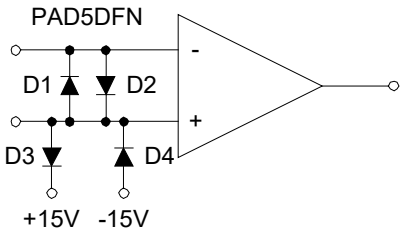
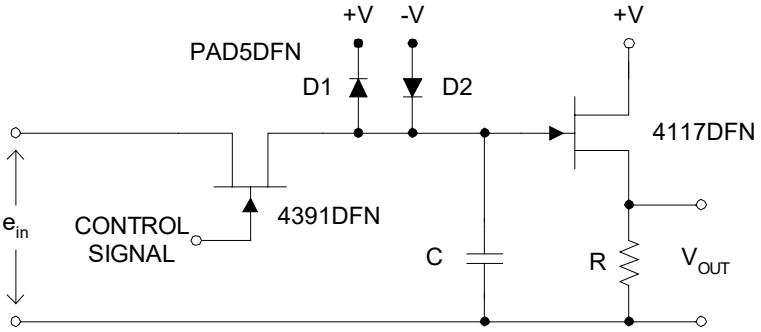
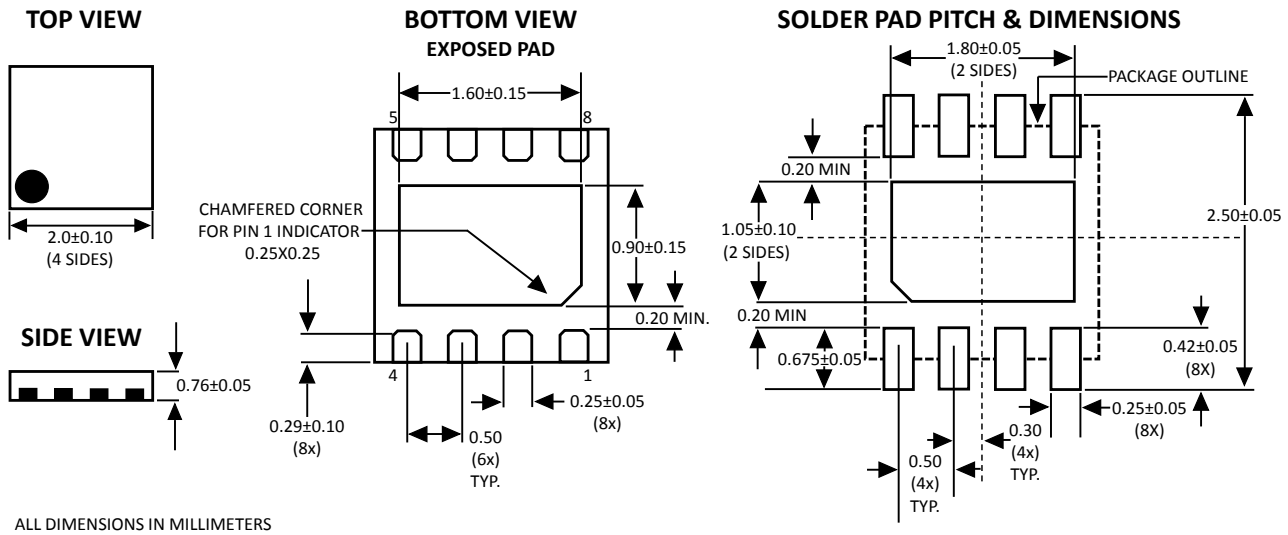


FIGURE 2



DFN PACKAGE



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Derate 2.8 mW/ºC above 25ºC
3. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

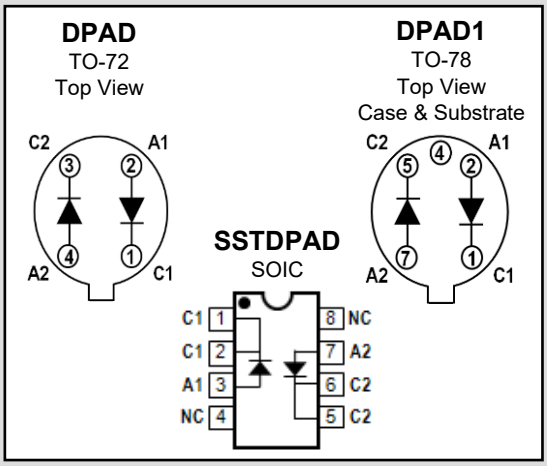
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

DPAD SERIES

MONOLITHIC DUAL PICO AMPERE DIODES

FEATURES	
Direct Replacement For SILICONIX DPAD SERIES	
HIGH ON ISOLATION	20fA
EXCELLENT CAPACITANCE MATCHING	$\Delta C_R \leq 0.2pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55ºC to +150°C
Operating Junction Temperature	-55ºC to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation (DPAD)[3]	500mW
Maximum Currents	
Forward Current (DPAD)	50mA



* Case and Pin 4 must be floating on all TO-78 case devices

COMMON ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	DPAD1	-45			V	I_R= -1µA
		DPAD2,5,10,20,50,100	-45				
		SSTDPAD5,50,100	-30				
V_F	Forward Voltage			0.8	1.5		I_F= 1mA
$\lvert C_{R1} - C_{R2} \rvert$	Differential Capacitance (ΔC_R)	DPAD1			0.2	pF	$V_{R1} = V_{R2}$ = -5V, *f*=1MHz
		ALL OTHERS			0.5		
C_{rss}	Total Reverse Capacitance	DPAD1			0.8		V_R = -5V, *f*=1MHz
		DPAD2,5,10,20,50,100			2.0		
		SSTDPAD5,50,100			4.0		

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise stated)

SYMBOL	CHARACTERISTIC		DPAD[2]	SSTDPAD[2]	UNITS	CONDITIONS
I_R	Maximum Reverse Leakage Current[2]	(SST)DPAD1	-1		pA	V_R = -20V
		(SST)DPAD2	-2			
		(SST)DPAD5	-5	-5		
		(SST)DPAD10	-10			
		(SST)DPAD20	-20			
		(SST)DPAD50	-50	-50		
		(SST)DPAD100	-100	-100		

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by DPADs D_1 and D_2. Common Mode Input voltage limited by DPADs D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

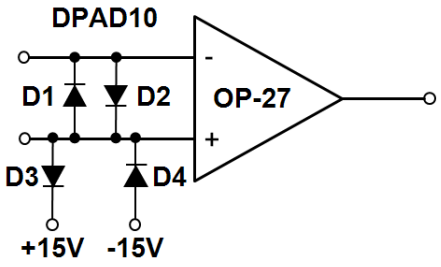
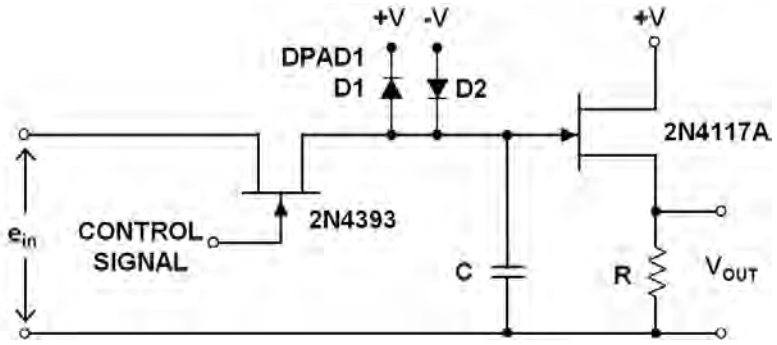
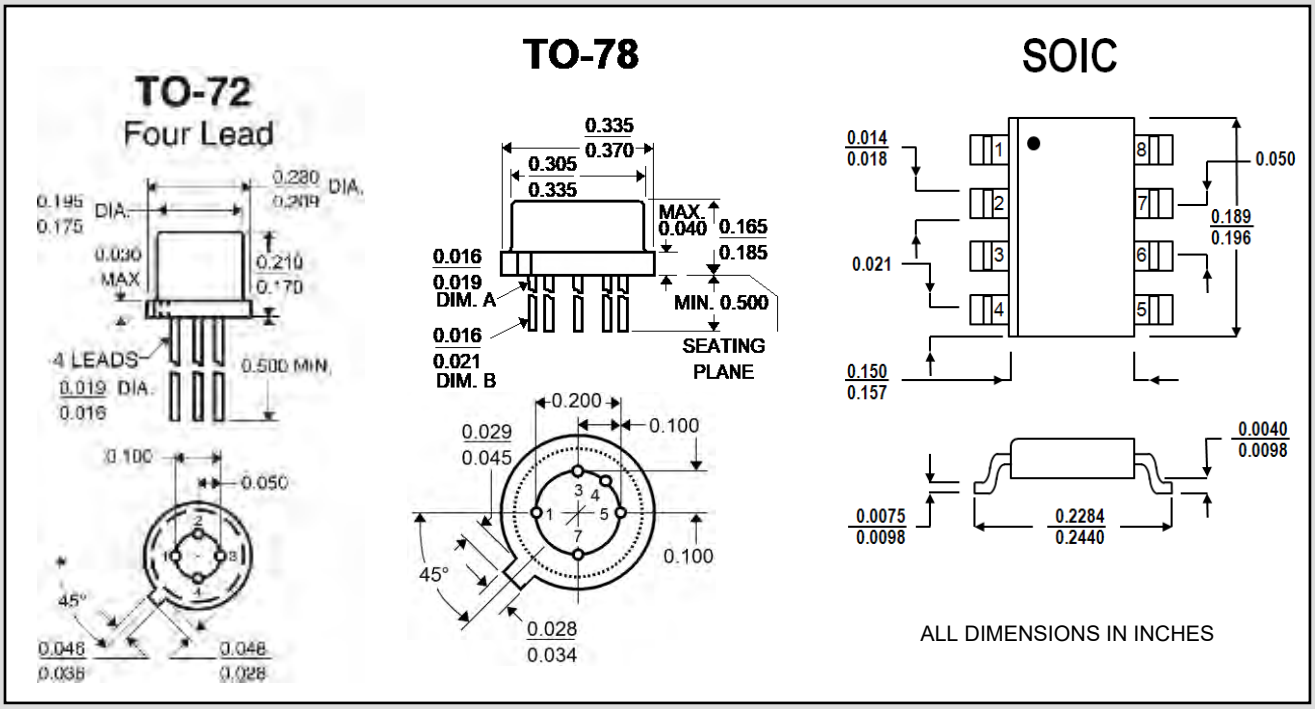


FIGURE 2





NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The DPAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.
3. Derate 4 mW/ºC above 25ºC

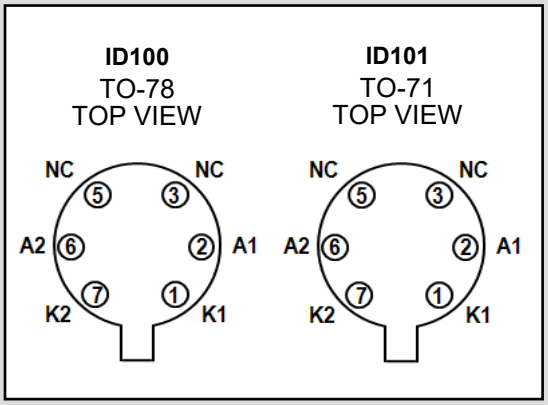
LINEAR SYSTEMS

Improved Standard Products®

ID100 ID101

MONOLITHIC DUAL PICO AMPERE DIODES

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL ID100 & ID101	
REVERSE LEAKAGE CURRENT	I_R = 0.1pA
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq$ 30V
REVERSE CAPACITANCE	C_{rss} = 0.75pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation @ TA = + 25°	
Continuous Power Dissipation	300mW
Maximum Currents	
Forward Current	20mA
Reverse Current	100µA
Maximum Voltages	
Reverse Voltage	30V
Diode to Diode Voltage	±50V



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1µA
V_F	Forward Voltage	0.8		1.1		I_F = 10mA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1V
			2.0	10		V_R = 10V
$\|I_{R1}-I_{R2}\|$	Differential Leakage Current			3		
C_{rss}	Total Reverse Capacitance[2]		0.75	1	pF	V_R = 10V, *f* = 1MHz

Figure 1. Operational Amplifier Protection
Input Differential Voltage limited to 0.8V (typ) by Diodes ID100 D_1 and D_2.
Common Mode Input voltage limited by Diodes ID100 D_3 and D_4 to ±15V.

Figure 2. Sample and Hold Circuit
Typical Sample and Hold circuit with clipping. ID100 diodes reduce offset voltages fed capacitively from the ID100 switch gate.

FIGURE 1

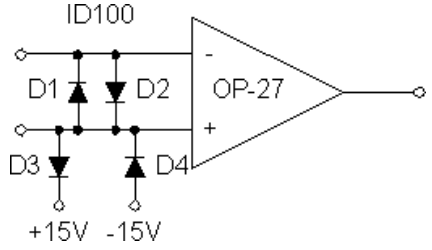
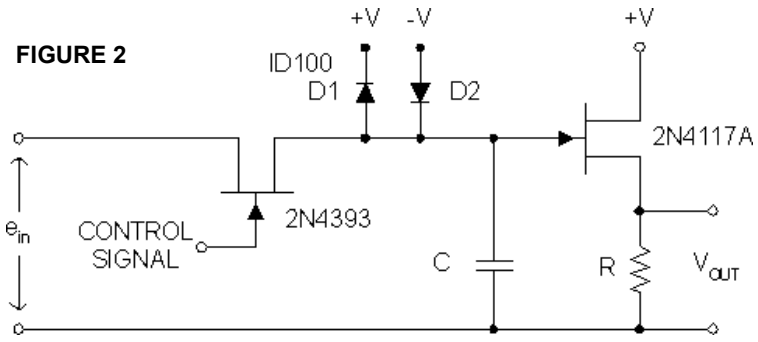
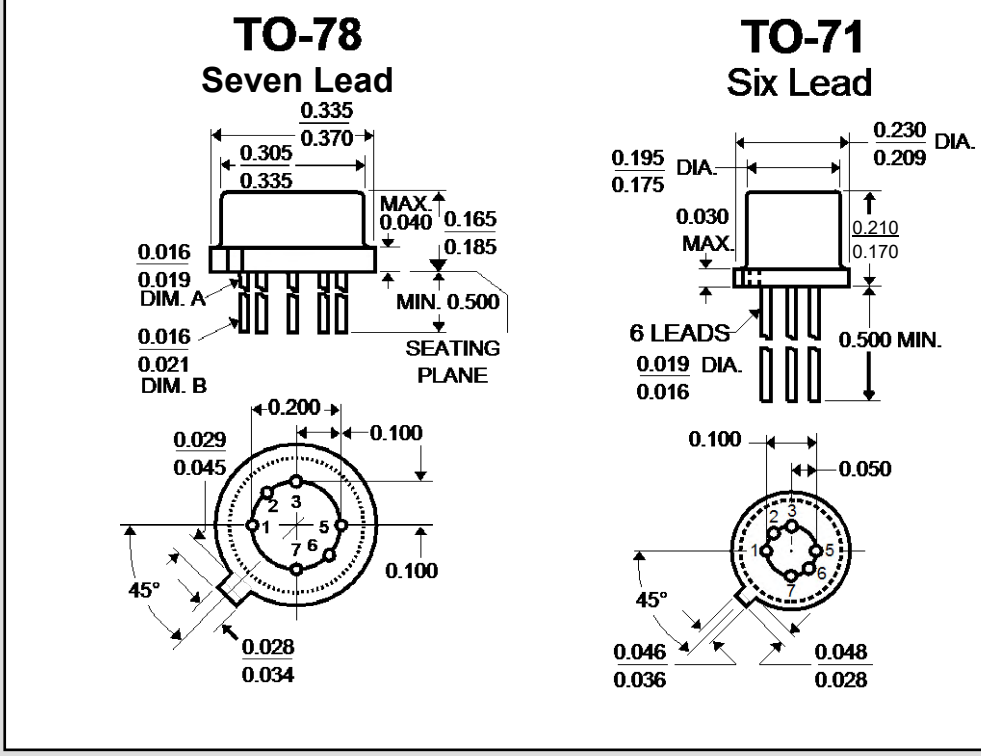


FIGURE 2



STANDARD PACKAGE DIMENSIONS:



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Design reference only, not 100% tested.
3. Pins 3 & 5 on ID100 and ID101 must not be connected, in any fashion or manner, to any circuit or node.

LINEAR SYSTEMS

Improved Standard Products®

SD-SST210/214

N-CHANNEL LATERAL DMOS SWITCH

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD210DE	30	1.5	45 @ V_{GS}=10V	0.5	2
SD214DE	20	1.5	45 @ V_{GS}=10V	0.5	2
SST210	30	1.5	50 @ V_{GS}=10V	0.5	2
SST214	20	1.5	50 @ V_{GS}=10V	0.5	2

PRODUCT SUMMARY

Features

- Ultra-High Speed Switching—t_{ON}: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

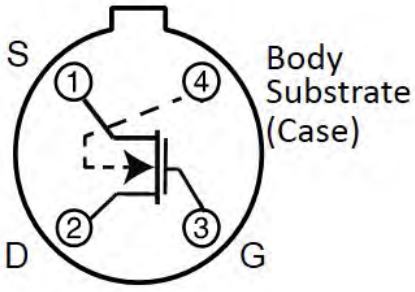
Description

The SD210DE/214 and SST210/214 are enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD214DE and SST214 are normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These MOSFETs do not have a gate protection Zener diode which results in lower gate leakage and ± voltage capability from gate to substrate. A poly-silicon gate is featured for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, Zener protected—SD211DE/SST211 Series.

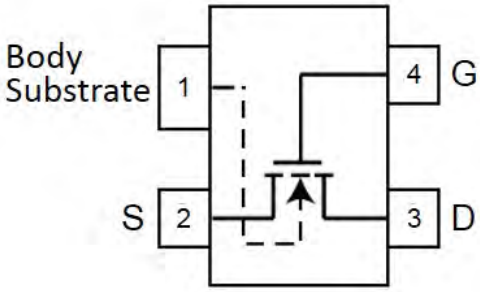
Top Views

SD210DE, SD214DE



TO-206AF
(TO-72)

SST210, SST214



TO-253
(SOT-143)

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate-Drain, Gate-Source Voltage . . . . . ± 40V
Gate-Substrate Voltage . . . . . ± 30V
Drain-Source Voltage (SD210DE/SST210) 30V
(SD214DE/SST214) 20V
Source-Drain Voltage (SD210DE/SST210) 10V
(SD214DE/SST214) 20V
Drain-Substrate Voltage (SD210DESST210) 30V
(SD214DE/SST214) 25V

Source-Substrate Voltage (SD210DE/SST210) 15V
(SD210DE/SST210) 25V
Drain Current 50mA
Lead Temperature (1/16" from ease for 10 seconds) . . . . . 300°C
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature . . . . . -55 to 125°C
Power Dissipation* 300mW

Note:
* Derate 3mW/°C above 25°C

Specifications[a]

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS 210 Series Min	LIMITS 210 Series Max	LIMITS 214 Series Min	LIMITS 214 Series Max	UNIT
Static									
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = 0V, I_D = 10 µA		35	30				V
		V_{GS} = V_{BS} = -5V, I_D = 10 nA		30	10		20		
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GD} = V_{BD} = -5V, I_S = 10 nA		22	10		20		
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB} = 0V, I_D= 10 nA Source Open		35	15		25		
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB} = 0V, I_s = 10 µA Drain Open		35	15		25		
Drain – Source Leakage	$I_{DS(off)}$	V_{GS} = V_{BS} = -5V	V_{DS} = 10V	0.4		10			nA
			V_{DS} = 20V	0.9				10	
Source - Drain Leakage	$I_{SD(off)}$	V_{GD} = V_{BD} = -5V	V_{SD} = 10V	0.5		10			
			V_{SD} = 20V					10	
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0V, V_{GB} = ±40V		±0.001		±100		±100	pA
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 µA , V_{SB} = 0V		0.8	0.5	1.5	0.1	1.5	V
Drain – Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0V I_D = 1mA	V_{GS} = 5V (SD Series)	58		70		70	Ω
			V_{GS} = 5V (SST Series)	60		75		75	
			V_{GS} = 10V (SD Series)	38		45		45	
			V_{GS} = 10V (SST Series)	40		50		50	
			V_{GS} = 15V	30					
			V_{GS} = 20V	26					
			V_{GS} = 25V	24					

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[c]	LIMITS				UNIT
					210 Series		214 Series		
					Min	Max	Min	Max	
Dynamic									
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz	SD Series	11	10		10		mS
			SST Series	10.5	9		9		
	g_{os}		All	0.9					
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V	SD Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2					
			SD Series	0.2		0.5		0.5	
Switching									
Turn-On Time	$t_{D(on)}$	SD Series Only V_{SB} = 0V, V_{IN} 0 to 5V, R_G = 25Ω V_{DD} = 5V, R_L = 680Ω		0.5		1		1	ns
	t_r			0.6		1		1	
Turn-Off Time	$t_{D(off)}$			2					
	t_f			6					

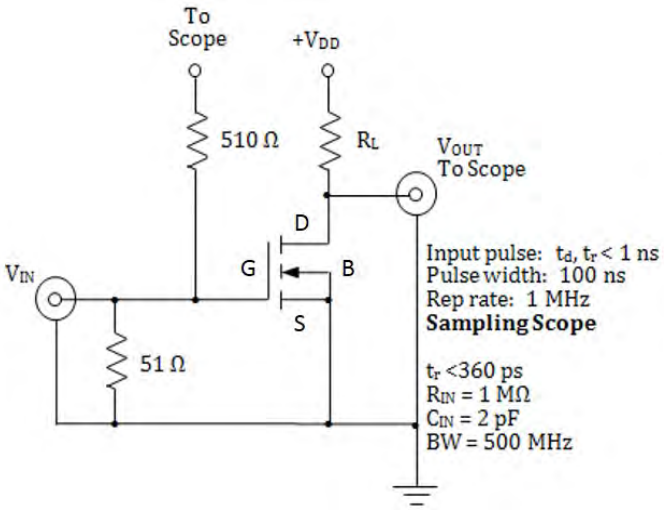
NOTES:

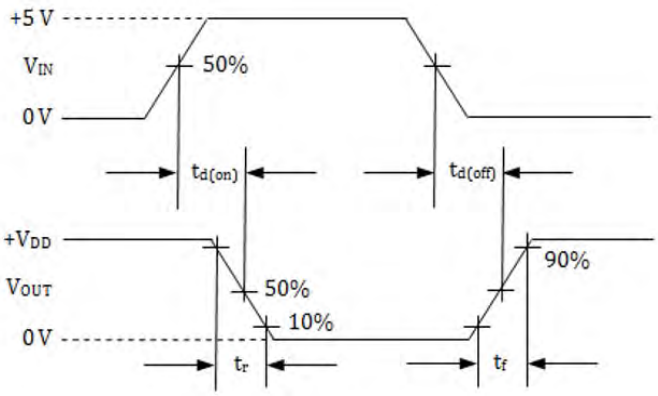
a. T_A = 25°C unless otherwise notes.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Switching Time Test Circuit





LINEAR SYSTEMS

Improved Standard Products®

SD-SST211/213/215

N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ V_{GS}=10V	0.5	2
SD213DE	10	1.5	45 @ V_{GS}=10V	0.5	2
SD215DE	20	1.5	45 @ V_{GS}=10V	0.5	2
SST211	30	1.5	50 @ V_{GS}=10V	0.5	2
SST213	10	1.5	50 @ V_{GS}=10V	0.5	2
SST215	20	1.5	50 @ V_{GS}=10V	0.5	2

Features

- Ultra-High Speed Switching—I_{ON}: 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

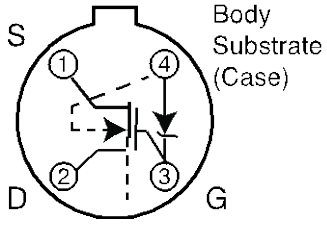
Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD211 may be used for a ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated ZENER diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, non-Zener protection—SD210DE/214DE.

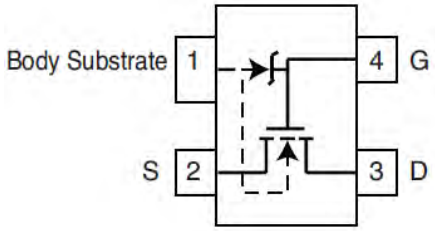
TOP VIEW

SD211DE, SD213DE, SD215DE



TO-206AF
(TO-72)

TO-253
(SOT-143)



TOP VIEW

SST211, SST213, SST215

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Gate Drain, Gate Source Voltage (SD211DE/SST211) . . . . . -30/25V
(SD213DE/SST213). . . . . -15/25V
(SD215DE/SST215). . . . . -25/30V
Gate-Substrate Voltage[a] (SD211DE/SST211) . . . . . -0.3/25V
(SD213DE/SST213) . . . . . -0.3/25V
(SD215DE/SST215) . . . . . -0.3/30V
Drain-Source Voltage (SD211DE/SST211) 30V
(SD213DE/SST213) 10V
(SD215DE/SST215) 20V
Voltage (SD211DE/SST211) 10V
(SD213DE/SST213) 10V
(SD215DE/SST215) 20V

Drain-Substrate Voltage (SD211DE/SST211) 30V
(SD213DE/SST213) 15V
(SD215DE/SST215) 25V
Source-Substrate Voltage (SD211DE/SST211) 15V
(SD213DE/SST213) 15V
(SD215DE/SST215) 25V
Drain Current 50mA
Lead Temperature (1/16" from ease for 10 seconds) . . . . . 300°C
Storage Temperature . . . . . -65 to 150°C
Operating Junction Temperature . . . . . -55 to 125°C
Power Dissipation 300mW

Notes:
a. Derate 3mW/°C above 25°C

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[b]	LIMITS						UNIT
					211 Series		213 Series		215 Series		
					Min	Max	Min	Max	Min	Max	
Static											
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS} = V_{BS} = 0V, I_D = 10 µA		35	30						V
		V_{GS} = V_{BS} = -5V, I_D = 10 nA		30	10		10		20		
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GS} = V_{BD} = -5V, I_S = 10 nA		22	10		10		20		
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB} = 0V, I_D= 10 nA Source Open		35	15		15		25		
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB} = 0V, I_s = 10 µA Drain Open		35	15		15		25		
Drain – Source Leakage	$I_{DS(off)}$	V_{GS} = V_{BS} = -5V	V_{DS} = 10V	0.4		10		10			nA
			V_{DS} = 20V	0.9						10	
Source - Drain Leakage	$I_{SD(off)}$	V_{GD} = V_{BD} = -5V	V_{SD} = 10V	0.5		10		10			
			V_{SD} = 20V							10	
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0V, V_{GB} = 30V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 µA , V_{SB} = 0V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain – Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0V I_D = 1mA	V_{GS} = 5V (SD Series)	58		70		70		70	Ω
			V_{GS} = 5V (SST Series)	60		75		75		75	
			V_{GS} = 10V (SD Series)	38		45		45		45	
			V_{GS} = 10V (SST Series)	40		50		50		50	
			V_{GS} = 15V	30							
			V_{GS} = 20V	26							
			V_{GS} = 25V	24							

Specifications[a]

PARAMETER	SYMBOL[b]	TEST CONDITIONS[b]		TYP[c]	LIMITS						UNIT
					211 Series		213 Series		215 Series		
					Min	Max	Min	Max			
Dynamic											
Forward Transconductance	g_{fs}	V_{DS} = 10V, V_{SB} = 0V, , I_D = 20mA, f = 1kHz	SD Series	11	10		10		10		mS
	g_{os}		SST Series	10.5	9		9		9		
			All	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2							
			SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{D(on)}$	SD Series Only V_{SB} = 0V, V_{IN} 0 to 5V, R_G = 25Ω V_{DD} = 5V, R_L = 680Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{D(off)}$			2							
	t_f			6							

Notes:

a. T_A = 25°C unless otherwise notes.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

LINEAR SYSTEMS

Improved Standard Products®

SD5000/5001/5400/5401

QUAD N-CHANNEL LATERAL DMOS SWITCH ZENER PROTECTED

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD5000I	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5000N	20	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5001N	10	1.5	70 @ V_{GS} = 5 V	0.5	2
SD5400CY	20	1.5	75 @ V_{GS} = 5 V	0.5	2
SD5401CY	10	1.5	75 @ V_{GS} = 5 V	0.5	2

Features

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

Description

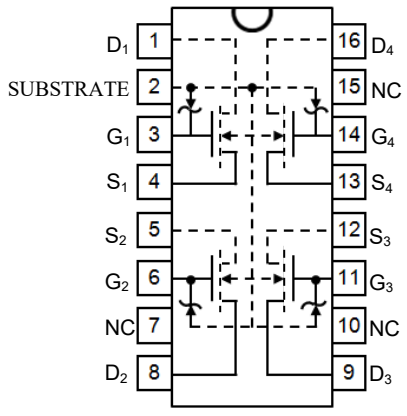
The SD5000/5400 series of monolithic switches features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. These bidirectional devices provide low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

Built on Siliconix' proprietary DMOS process, the SD5000/5400 series utilizes lateral construction to achieve low capacitance and ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes

The SD 5000/5400 are rated to handle ±10-V analog signals, while the SD5001/5401 are rated for ±5-V signals.

For similar products packaged in TO-206AF (TO-72) and TO-253 (SOT-143) see the SD211DE/SST211 series.

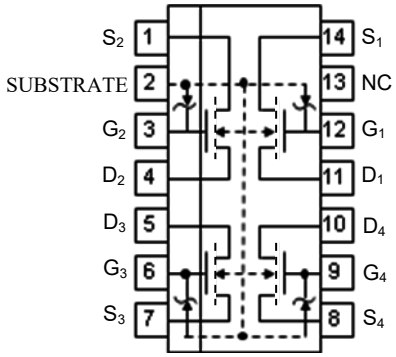
Dual-In-Line



Top View

Plastic: SD5000N
SD5001N
Sidebraze: SD5000I

Narrow Body SOIC



Top View

SD5400CY
SD5401CY

Absolute Maximum Ratings (T_A = 25ºC Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage
(SD5000, SD5400)……+30V/-25V
(SD5001, SD5401)……+25V/-15V
Gate-Substrate Voltage (SD5000, SD5400)……+30V/-0.3V
(SD5001I, SD5401)……+25V/-0.3V
Drain-Source Voltage (SD5000, SD5400)……20V
(SD5001I, SD5401)……10V
Drain-Source-Substrate Voltage (SD5000, SD5400)……25V
(SD5001I, SD5401)……15V

Drain Current……50 mA
Lead Temperature (1/16" from case for 10 seconds)……300ºC
Storage Temperature……-65 to 150ºC
Operating Junction Temperature……-55 to 150ºC
Power Dissipation": (Package)……500 mW
(each Device)……300 mW

Notes:
a. SD5000/SD5001I derate 5 mW/C above 25ºC
b. SD5400/SD5401 derate 4 mW/C above 25ºC

Specifications[a]

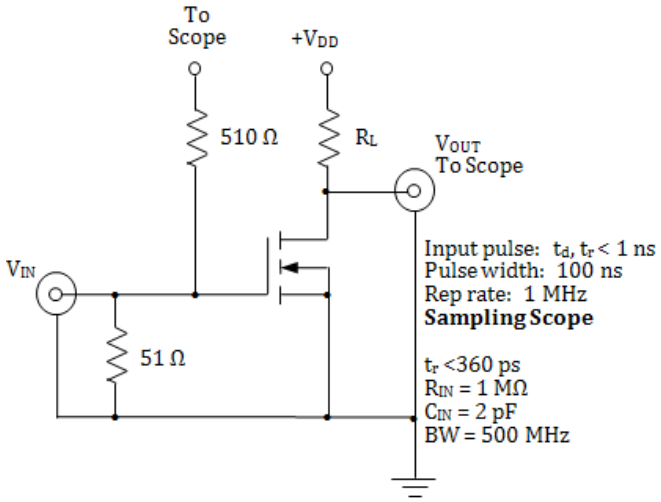
Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits SD5000 SD5400 Min	Limits SD5000 SD5400 Max	Limits SD5001 SD5401 Min	Limits SD5001 SD5401 Max	Unit
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	V_{GS}=V_{BS}=-5V, I_D=10nA		30	20		10		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	V_{GD}=V_{BD}=-5V, I_S=10nA		22	20		10		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	V_{GB}=0 V, I_D=10µA, Source Open		35	25		15		V
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	V_{GB}=0 V, I_S=10µA, Drain Open		35	25		15		V
Drain-Source Leakage	$I_{DS(off)}$	V_{GS}= V_{BS}=-5 V	V_{DS}= 10 V	0.4				10	nA
			V_{DS}= 15 V	0.7					nA
			V_{DS}= 20 V	0.9		10			nA
Source-Drain Leakage	$I_{SD(off)}$	V_{GD}= V_{BD}=-5 V	V_{SD}= 10 V	0.5				10	nA
			V_{SD}= 15 V	0.8					nA
			V_{SD}= 20 V	1		10			nA
Gate Leakage	I_{GBS}	V_{DB} = V_{SB} = 0 V, V_{GB} =30V		0.01		100		100	nA
Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = I µA, V_{SB} =0V		0.8	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{SB} = 0 V, I_D = 1 mA	SD5000 Series V_{GS} = 5 V	58		70		70	Ω
			SD5400 Series V_{GS} = 5 V	60		75		75	Ω
			V_{GS} = 10 V	38					Ω
			V_{GS} = 15 V	30					Ω
			V_{GS} = 20 V	26					Ω
Resistance Match	$\Delta r_{DS(on)}$		V_{GS} = 5 V	1		5		5	Ω
Dynamic									
Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{SB} = 0 V, I_D = 20 mA, f = 1 kHz	SD5000 Series	12	10		10		mS
			SD5400 Series	11	9		9		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V, f = 1 MHz, V_{GS} = V_{BS} = -15V	SD5000 Series	2.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			2.0		3		3	pF
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5		5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5	pF
Crosstalk		f = 3 kHz		-107					dB

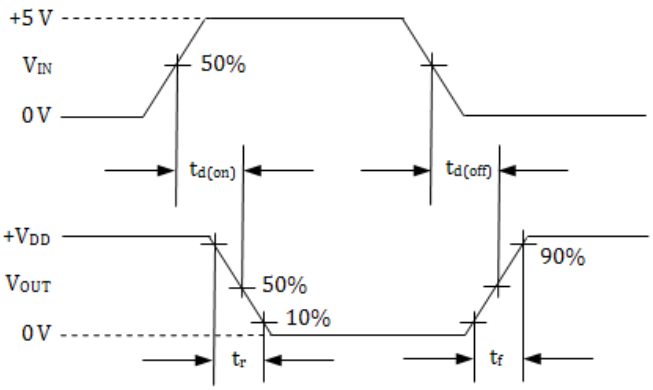
Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]	Typ[c]	Limits				Unit
				SD5000 SD5400		SD5001 SD5401		
				Min	Max	Min	Max	
Switching								
Turn-On Time	$t_{d(on)}$	V_{SB}= 1-5 Vin, V_{GN} 0 to 5 V, R_G = 25 Ω V_{DD} = 5 V, R_L = 680 Ω	0.5		1		1	ns
	t_r		0.6		1		1	
Turn-Off Time	$t_{d(off)}$		2					
	t_f		6					

Notes: DMCA
a. T_A = 25ºC unless otherwise noted.
b. B is the body (substrate) and $V_{(BR)}$ is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Switching Time Test Circuit





NOTES:

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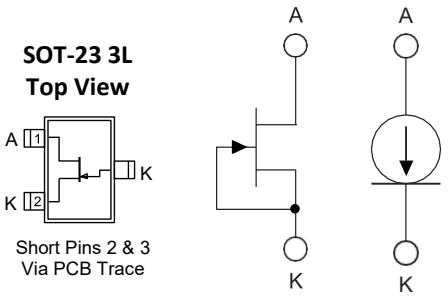
SST500 Series

Current Regulating Diodes

IDEAL CHOICE FOR TEST INSTRUMENTATION AND MEDICAL APPLICATIONS

FEATURES	
REPLACES SILICONIX/VISHAY SST502 SERIES	
WIDE CURRENT RANGE	0.19 to 5.6mA
BIASING NOT REQUIRED	V_{GS} = 0V
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to 150°C
Junction Operating Temperature	-55 to 150°C
Maximum Power Dissipation	
Continuous Power Dissipation[7]	350mW
Maximum Currents	
Forward Current	20mA
Reverse Current	50mA
Maximum Voltages	
Peak Operating Voltage	P_{OV} = 50V



Package Photo

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
P_{OV}	Peak Operating Voltage[6]	50			V	$I_F = 1.1I_{F\,(max)}$
V_R	Reverse Voltage		0.8		V	I_R = 1mA
C_F	Forward Capacitance		1.5		pF	V_F = 25V, *f* = 1MHz

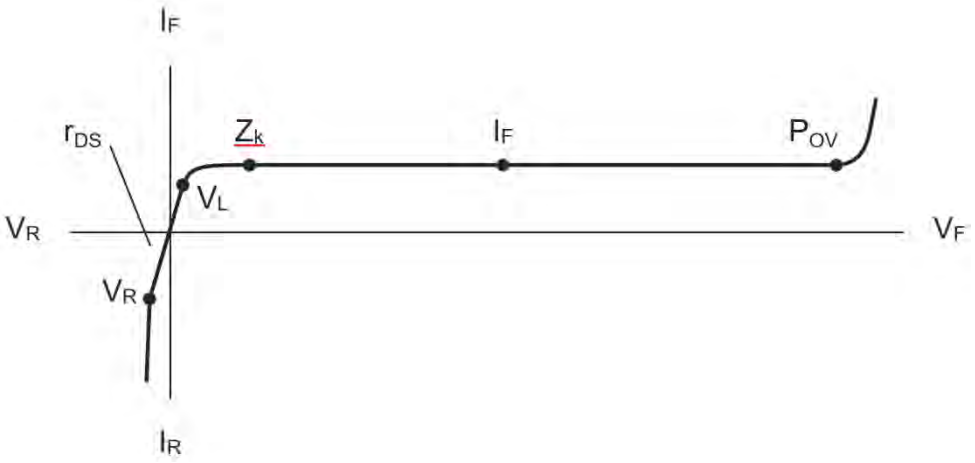
SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

PART	Forward Current[3] I_F(mA)			Dynamic Impedance[4] Z_d(MΩ)		Knee Impedance Z_k(MΩ)	Limiting Voltage[5] V_L(V)	
	V_F = 25V			V_F = 25V		V_F = 6V	$I_F = 0.8I_{F(min)}$	
	MIN	NOM	MAX	MIN	TYP	TYP	TYP	MAX
SST500	0.192	0.24	0.288	4.00	15	2.50	0.4	1.2
SST501	0.264	0.33	0.396	2.20	10	1.60	0.5	1.3
SST502	0.344	0.43	0.516	1.0	2.7	0.7	0.6	1.5
SST503	0.448	0.56	0.672	0.7	2.0	0.5	0.7	1.7
SST504	0.600	0.75	0.900	0.5	1.5	0.4	0.8	1.9
SST505	0.800	1.00	1.200	0.4	1.0	0.3	0.9	2.1
SST506	1.120	1.40	1.680	0.3	0.8	0.2	1.1	2.5
SST507	1.440	1.80	2.160	0.2	0.6	0.12	1.3	2.8
SST508	1.900	2.40	2.900	0.1	0.4	0.08	1.5	3.1
SST509	2.400	3.00	3.600	0.09	0.3	0.06	1.7	3.5
SST510	2.900	3.60	4.300	0.08	0.3	0.04	1.9	3.9
SST511	3.800	4.70	5.600	0.07	0.2	0.03	2.1	4.2

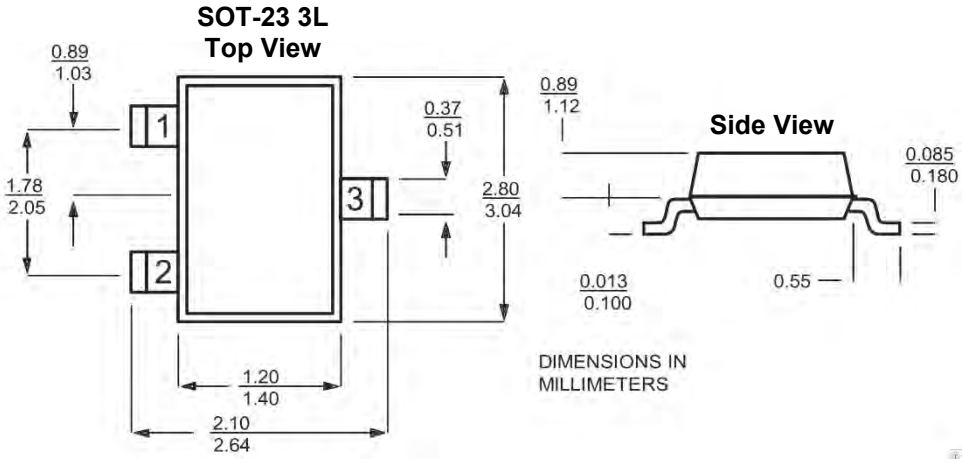
NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulsed, t = 2ms. Steady State currents may vary.
3. Pulsed, t = 2ms. Continuous currents may vary.
4. Pulsed, t = 2ms. Continuous impedances may vary.
5. Min V_F required to ensure $I_F = 0.8I_{F(min)}$.
6. Max V_F where If = 1.1 x I_F max is guaranteed. Pulsed test ≤2mS.
7. Derate 2.8 m W/°C above 25°C.

V-I Characteristics Current Regulating Diode



Packaging Details



Ordering Information

Standard Part Call-Out
SST500 SOT-23 3L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
SST500 SOT-23 3L RoHS SELXXXX

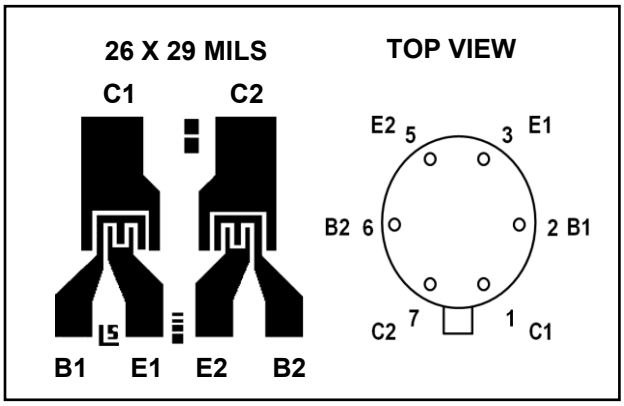
LINEAR SYSTEMS

Improved Standard Products®

IT120A IT120 IT121 IT122

MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
Direct Replacement for Intersil IT120 Series Pin for Pin Compatible		
ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C Collector-Current	10mA	
Maximum Temperatures		
Storage Temperature Range	-65°C to +150°C	
Operating Temperature Range	-55°C to +150°C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3W/°C



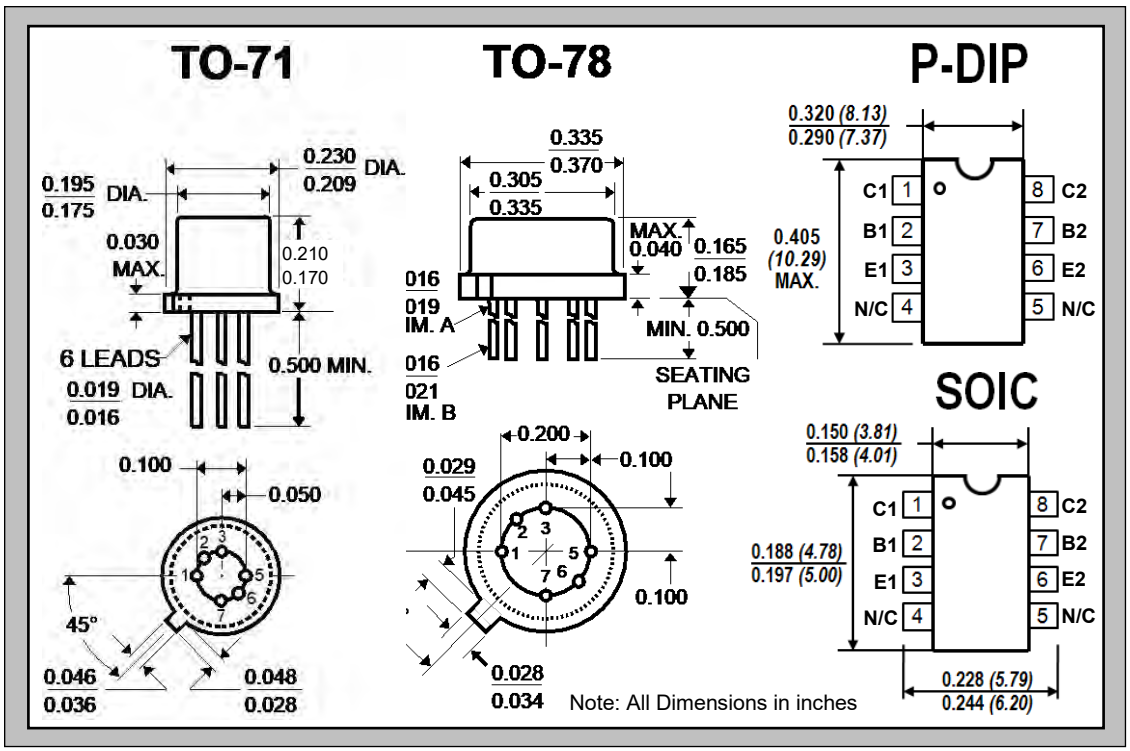
ELECTRICAL CHARACTERISTICS T_A= 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT120A	IT120	IT121	IT122		UNITS	CONDITIONS	
BV_{CBO}	Collector to Base Voltage	45	45	45	45	MIN.	V	I_C = 10µA	I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	45	45	45	45	MIN.	V	I_C = 10µA	I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	6.2	6.2	6.2	6.2	MIN.	V	I_E = 10µA	I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	60	60	60	60	MIN.	V	I_{CCO} = 10µA	$I_B = I_E$ = 0A
h_{FE}	DC Current Gain	200	200	80	80	MIN.		I_C = 10µA	V_{CE} = 5V
		225	225	100	100	MIN.		I_C = 1.0mA	V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	0.5	MAX.	V	I_C = 0.5mA	I_B = 0.05mA
I_{EBO}	Emitter Cutoff Current	1	1	1	1	MAX.	nA	I_C = 0	V_{EB} = 3V
I_{CBO}	Collector Cutoff Current	1	1	1	1	MAX.	nA	I_E = 0	V_{CB} = 45V
C_{OBO}	Output Capacitance[3]	2	2	2	2	MAX.	pF	I_E = 0	V_{CB} = 5V
C_{C1C2}	Collector to Collector Capacitance[3]	2	2	2	2	MAX.	pF	V_{CC} = 0	
I_{C1C2}	Collector to Collector Leakage Current	±500	±500	±500	±500	MAX.	nA	V_{CCO} = ±60V	$I_B = I_E$ = 0A
f_T	Current Gain Bandwidth Product[3]	220	220	180	180	MIN.	MHz	I_C = 1mA	V_{CE} = 5V
NF	Narrow Band Noise Figure[3]	3	3	3	3	MAX.	dB	I_C = 100µA BW = 200Hz, R_G = 10 KΩ f=1KHz	V_{CE} = 5V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT120A	IT120	IT121	IT122		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	2	3	5	MAX.	mV	I_C = 10 µA V_{CE} = 5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential Change with Temperature[3]	3	5	10	20	MAX.	µV/°C	I_C = 10 µA V_{CE} = 5V T = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	2.5	5	25	25	MAX.	nA	I_C = 10 µA V_{CE} = 5V

STANDARD PAKAGE DIMENSINS:



NOTES:

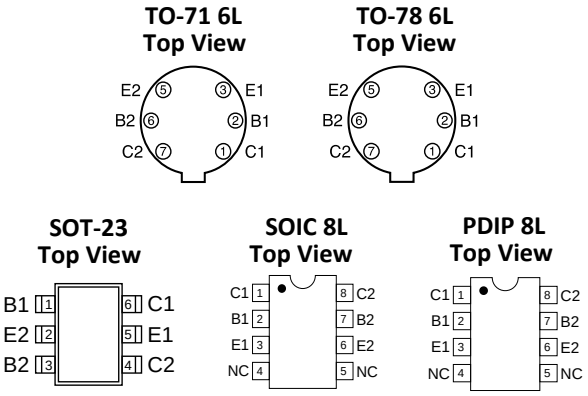
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. Not a production test.

LS3250A/B/C

Monolithic Dual Matched NPN Transistor

LOW NOISE AND THERMALLY MATCHED MONOLITHIC DUAL NPN TRANSISTOR

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Voltages	
Maximum Power Supply	45V
Collector to Collector	50V
Maximum Current	
Collector Current	50mA



Features

- Low Voltage Noise, 2.7nV-typ at f=100Hz
- Low Vbe Matching 2mV-max
- Low Vbe Temperature Drift 3µV/˚C-max
- High Current Gain 150-Min and 650-max
- High VCBO Breakdown Voltage-45V-min
- High VCEO Breakdown Voltage-45V-min
- High VCCO Breakdown Voltage +/-50V-min
- Refer to LS350/1/2 dual PNP for counterpart version

Benefits

- Unique Monolithic Dual Design Construction
- Improved System Noise Performance
- Wide Range of Parameter Operations
- High Frequency Performance
- Excellent Matching and Thermal Tracking
- Operation in High Voltage Applications

Applications

- Differential and Preamplifiers
- Multivibrator Circuits
- Music Synthesizers
- Current Sources
- Clocking Networks
- Voltage Controlled Oscillators
- Frequency Division
- Photon Generators

Description

The LS3250A/B/C monolithic dual matched NPN transistor offers excellent matching characteristics and high frequency performance up to 600MHz gain bandwidth product. Low 2pF-max Cobo output capacitance further improves frequency characteristics and decreases signal distortion at the output.

Tight current gain matching and high current gain, make the LS3250 an ideal choice for accurate current biasing and mirroring circuits and designs. LS3250 output stages do not need considerable error correction, due to their higher transconductance and have a positive temperature coefficient of current (Ib and Ic).

Low noise performance, low offset voltage and high bandwidth, make the LS3250 ideal for differential input stages and pre-amplifier applications.

Due to its high breakdown specifications, the LS3250 is suitable in high voltage applications requiring up to 45VMax. In addition to the very small outline SOT-23 6L package, the LS3250 is available in the TO-78 6L, TO-71 6L, PDIP 8L and SOIC 8L packages.

Furthermore, the LS3250 is offered with custom electrical specifications called SELXXXX. Contact our factory for modified electrical specifications for these special versions of the LS3250 SELXXXX.

Refer to the LS350/1/2 dual PNP for the counterpart version.

Electrical Characteristics @ 25 °C (Unless Otherwise Stated)

SYMBOL	CHARACTERISTIC	LS3250A		LS3250B		LS3250C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Differential	-	2	-	5	-	10	mV	I_C = 10µA, V_{CE} = 5V
$\frac{\lvert V_{BE1} - V_{BE2} \rvert}{\Delta T}$	Base to Emitter Voltage Differential Change with Temperature	-	3	-	5	-	15	µV/°C	I_C = 10µA, V_{CE} = 5V T_A = -40°C to +85°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential	-	10	-	10	-	10	nA	I_C = 10µA, V_{CE} = 5V
$\frac{\lvert I_{B1} - I_{B2} \rvert}{\Delta T}$	Base Current Differential Change with Temperature	-	0.5	-	0.5	-	1.0	nA/°C	I_C = 10µA, V_{CE} = 5V T_A = -40°C to +85°C
h_{FE1}/h_{FE2}	Current Gain Differential	-	10	-	10	-	15	%	I_C = 1mA, V_{CE} = 5V
BV_{CBO}	Collector to Base Breakdown Voltage	45	-	40	-	20	-	V	I_C = 10µA, I_E = 0A
BV_{CEO}	Collector to Emitter Breakdown Voltage	45	-	40	-	20	-		I_C = 10mA, I_B = 0
BV_{CCO}	Collector to Collector Breakdown Voltage	±50	-	±50	-	±50	-		I_C = ±1µA, I_E = I_B= 0A
BV_{EBO}	Emitter to Base Breakdown Voltage[3]	6.0	-	6.0	-	6.0	-		I_E = 10µA, I_C = 0A
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	-	0.35	-	0.35	-	1.2		I_C = 10mA, I_B = 1mA
h_{FE}	DC Current Gain	150	-	100	-	50	-	-	I_C = 1mA, V_{CE} = 5V
		150	650	80	-	40	-		I_C = 10mA, V_{CE} = 5V
		125	-	60	-	30	-		I_C = 35mA, V_{CE} = 5V
I_{CBO}	Collector Cutoff Current	-	0.35	-	0.35	-	-	nA	I_E = 0A, V_{CB} = 30V
		-	-	-	-	-	0.2		I_E = 0A, V_{CB} = 20V
I_{EBO}	Emitter Cutoff Current	-	0.35	-	0.35	-	0.35		I_E = 0A, V_{CB} = 3V
I_{C1C2}	Collector to Collector Leakage Current	-	±1	-	±1	-	±1	µA	V_{CC} = ±50V, I_E = I_B= 0A
C_{OBO}	Output Capacitance	-	2	-	2	-	2	pF	I_E = 0A, V_{CB} = 10V
f_T	Gain Bandwidth Product (Current)	-	600	-	600	-	600	MHz	I_C = 1mA, V_{CE} = 5V
en	Noise Voltage	-	2.7typ	-	2.7typ	-	2.7typ	nV/√Hz	V_{CE}==5V, IC=2mA F=100Hz, NBW=1Hz
en	Noise Voltage	-	0.7typ	-	0.7typ	-	0.7typ	nV/√Hz	V_{CE} ==5V, IC=2mA F=1kHz, NBW=1Hz

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

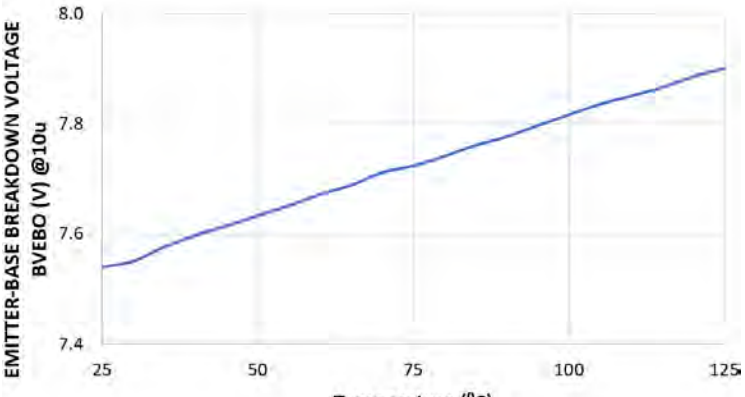


Figure-1 BVEBO(V) vs. Temperature

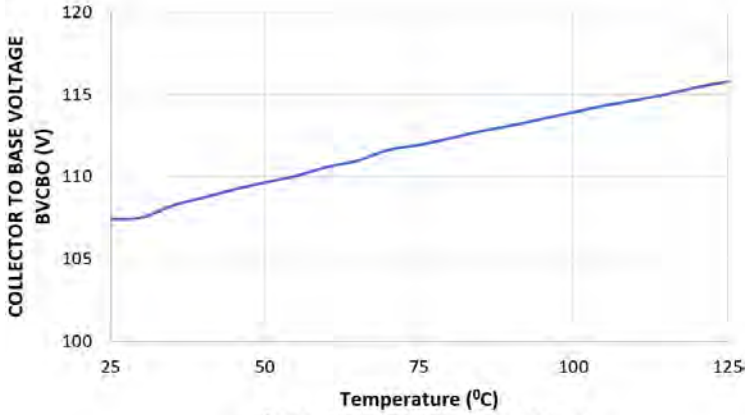


Figure-2 BVCBO(V) vs. Temperature

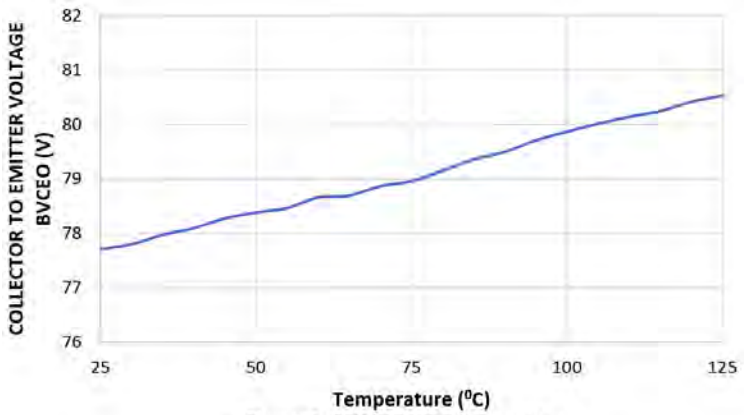


Figure-3 (BVCEO(V) vs. Temperature

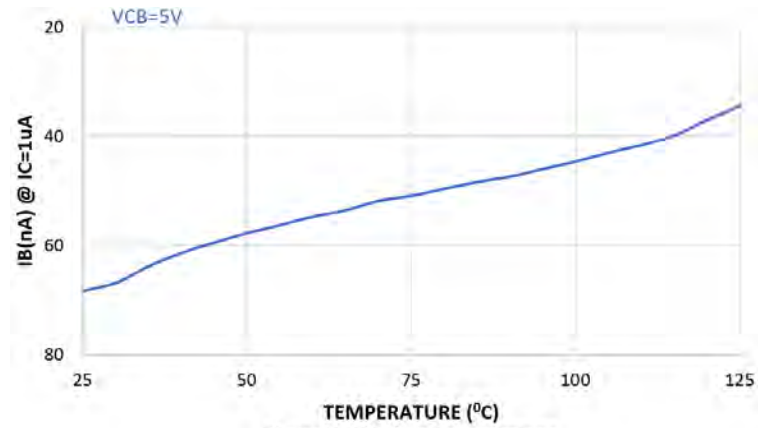


Figure-4 IB(nA) vs. Temperature

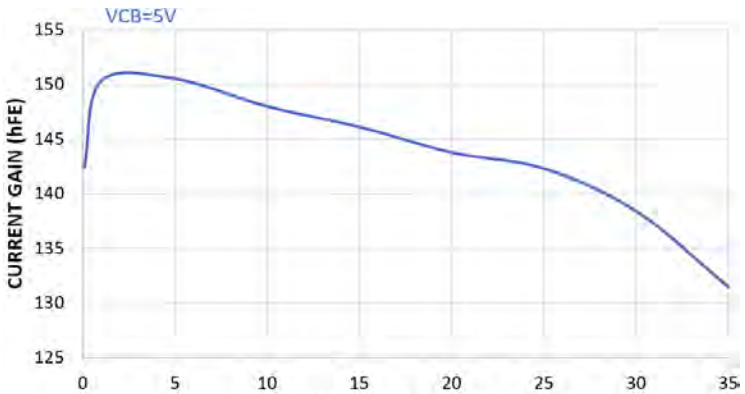


Figure-5 COLLECTOR CURRENT vs. CURRENT GAIN (hFE)

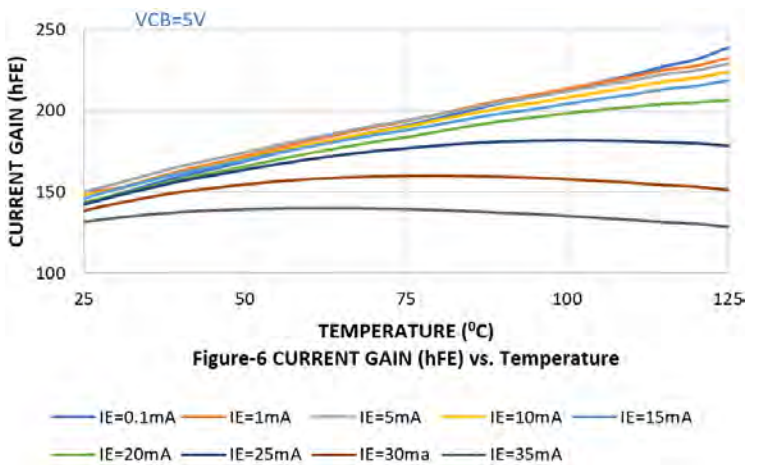


Figure-6 CURRENT GAIN (hFE) vs. Temperature

Typical Characteristics Continued

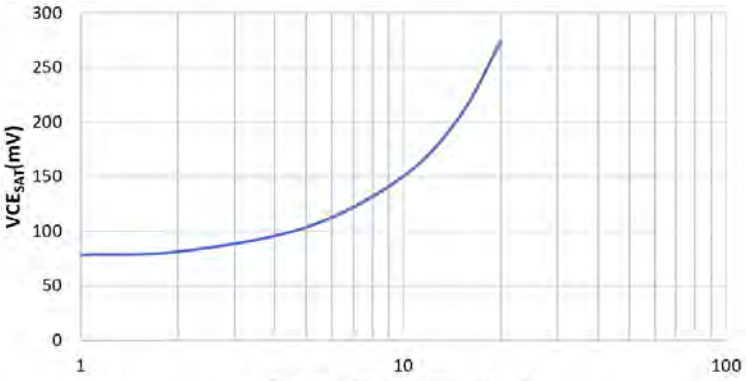


Figure-7 COLLECTOR CURRENT(mA) vs. VCE$_{SAT}$ (mV)

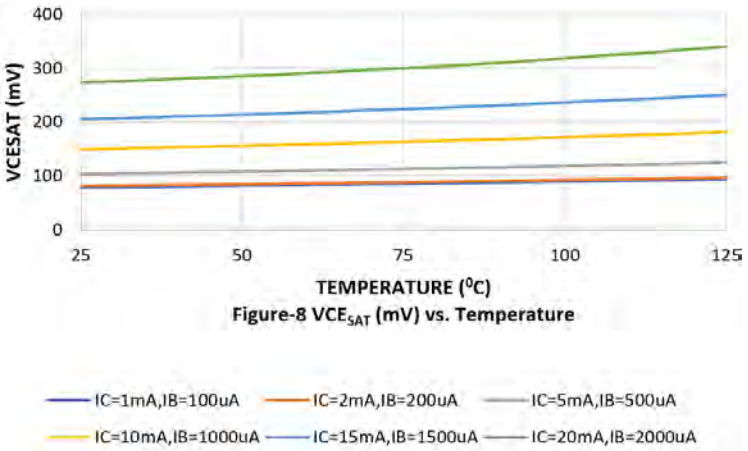


Figure-8 VCE$_{SAT}$ (mV) vs. Temperature

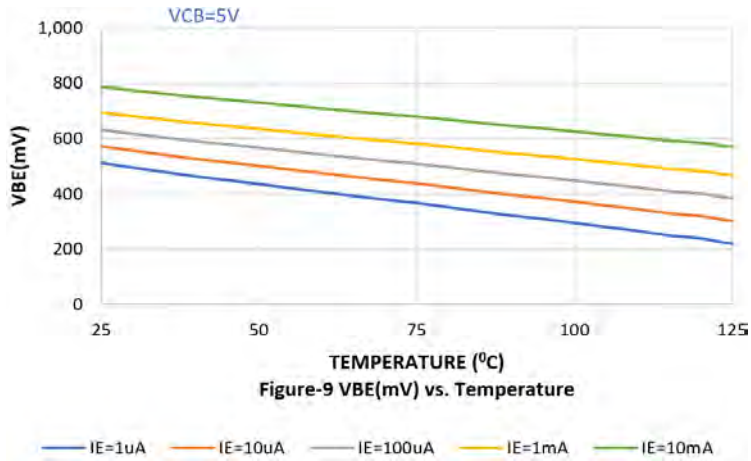


Figure-9 VBE(mV) vs. Temperature

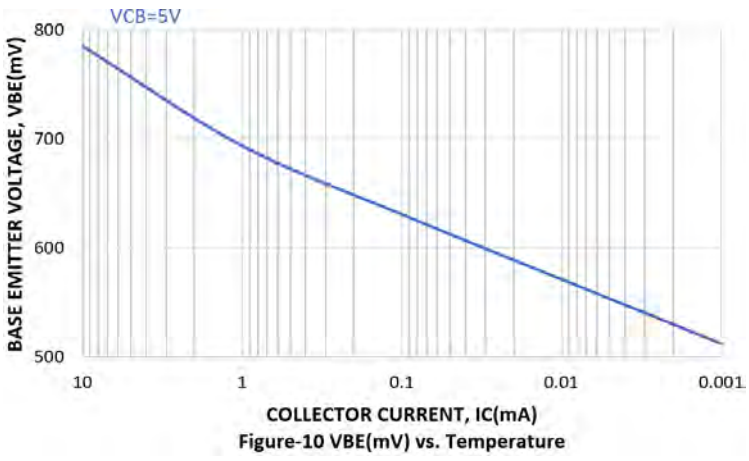


Figure-10 VBE(mV) vs. Temperature

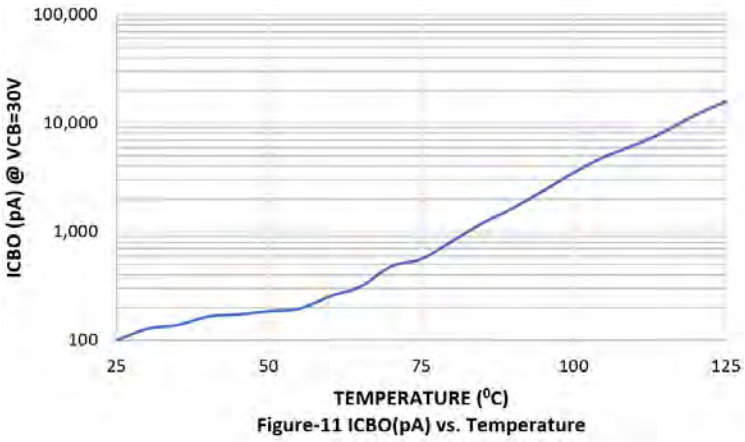


Figure-11 ICBO(pA) vs. Temperature

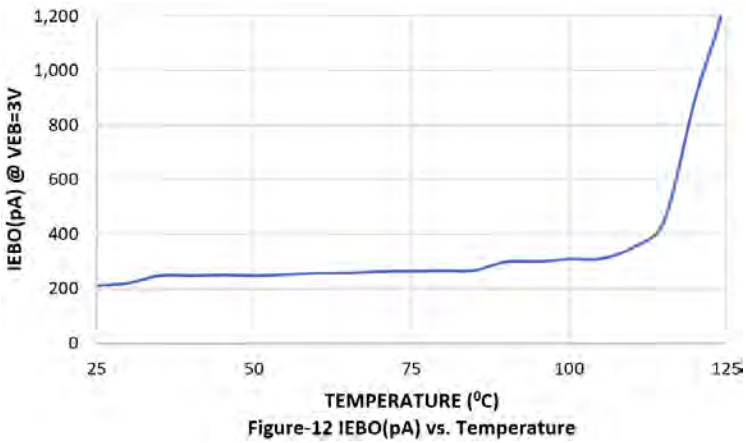


Figure-12 IEBO(pA) vs. Temperature

Typical Characteristics Continued

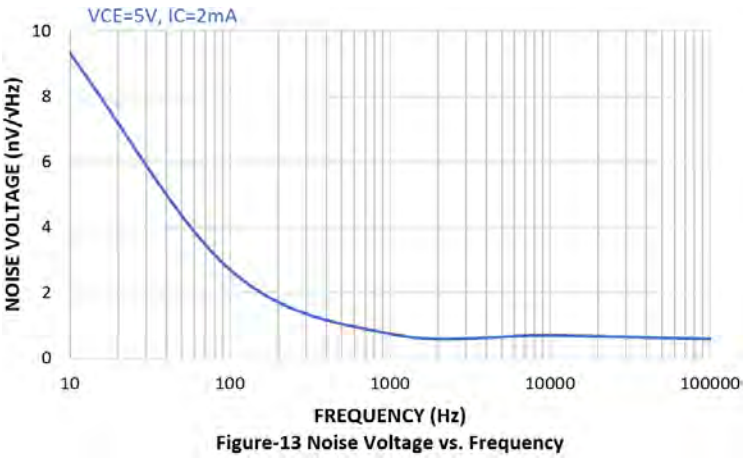


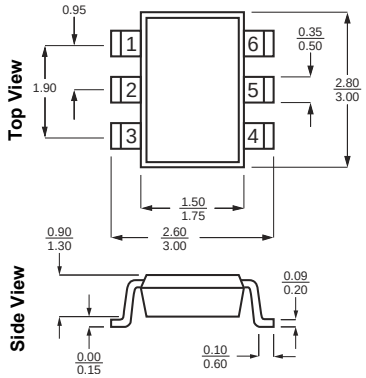
Figure-13 Noise Voltage vs. Frequency

Ordering Information

Standard Part Call-Out
LS3250A/B/C TO-71 6L RoHS
LS3250A/B/C TO-78 6L RoHS
LS3250A/B/C PDIP 8L RoHS
LS3250A/B/C SOIC 8L RoHS
LS3250A/B/C SOT-23 6L RoHS
Custom Part Call-out Custom parts include SEL+4 digit numeric code
LS3250A/B/C TO-71 6L RoHS SELXXXX
LS3250A/B/C TO-78 6L RoHS SELXXXX
LS3250A/B/C PDIP 8L RoHS SELXXXX
LS3250A/B/C SOIC 8L RoHS SELXXXX
LS3250A/B/C SOT-23 6L RoHS SELXXXX

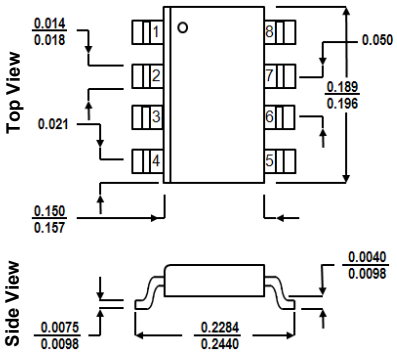
Package Dimensions

SOT-23 6 Lead



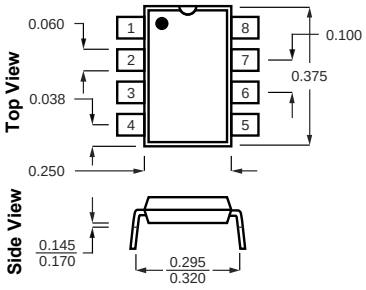
DIMENSIONS IN MILLIMETERS

SOIC-A 8 Lead



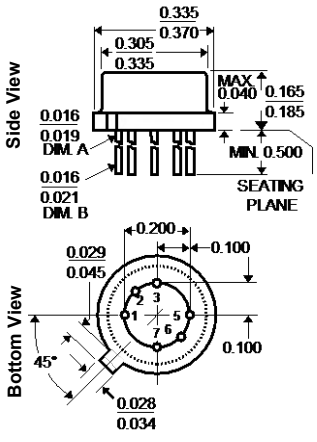
DIMENSIONS IN INCHES

PDIP 8 Lead



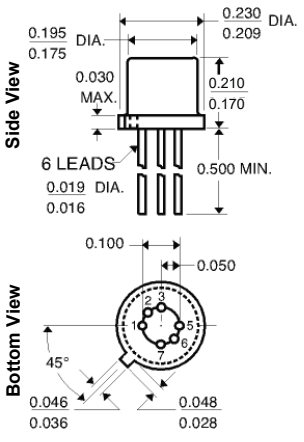
DIMENSIONS IN INCHES

TO-78 6 Lead



DIMENSIONS IN INCHES

TO-71 6 Lead



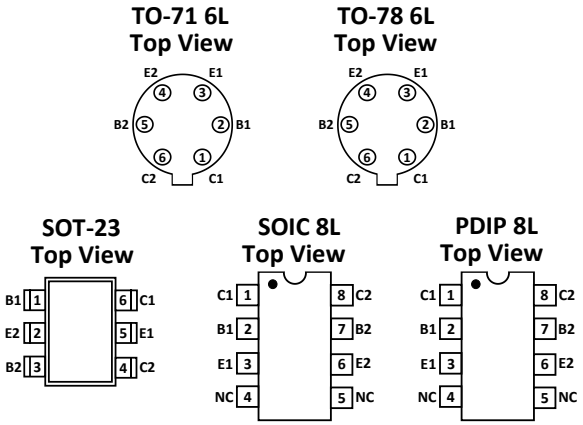
DIMENSIONS IN INCHES

LS310/311/312/313

Monolithic Dual Matched NPN Transistor

LOW NOISE AND THERMALLY MATCHED MONOLITHIC DUAL NPN TRANSISTOR

Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	400mW
Maximum Voltages	
Maximum Power Supply (LS312, see V_{CEO} for others)	60V
Collector to Collector (LS312, see V_{CEO} for others)	60V
Maximum Current	
Collector Current	40mA



Features

- Low Voltage Noise, 1.8nV/√Hz-typ at f=1kHz, IC=100μA
- Low Vbe Matching 0.5mV-max, 0.2mV-typ (LS312)
- Low Vbe Temperature Drift 0.5 μV/˚C-typ (LS312)
- High Current Gain 400-Min (LS313)
- High VCBO Breakdown Voltage-60V-min (LS312)
- High VCEO Breakdown Voltage-60V-min (LS312)
- High VCCO Breakdown Voltage +/-60V-min
- Dual PNP Counterpart Version: LS350/1/2

Benefits

- Unique Monolithic Dual Design Construction
- Improved System Noise Performance
- Wide Range of Parameter Operations
- Excellent Base-Emitter Voltage Differential (ΔVBE) and Drift
- Excellent Base Current Differential (IB1-IB2) and Drift
- High Frequency Performance
- Excellent Matching and Thermal Tracking
- High Voltage Operation-60V-min (LS312)

Applications

- Input Differential and Preamplifier Stages
- Multivibrator Circuits
- Music Synthesizers
- Current Sources
- Discreate Operational and Instrumentation Amplifiers
- Clocking Networks
- Voltage Controlled Oscillators
- Frequency Division

Description

The LS310/11/12/13 monolithic dual matched NPN transistors offer excellent matching characteristics and low voltage noise (refer to figure-14 for details.)

Low 2pF-max Cobo output capacitance further improves frequency characteristics and decreases signal distortion at the output. Low noise performance, low offset voltage and high bandwidth, make the products ideal for differential input stages and preamplifier applications.

Tight current gain matching, high current gain and high breakdown make the LS312 and LS313 an ideal choice for signal amplifying, accurate current biasing and mirroring circuits and designs.

LS310/11/12/13 output stages need very little error correction, due to their higher transconductance and have a positive temperature coefficient of current (Ib and Ic).

Due to high breakdown specifications, the products are suitable in high voltage applications requiring up to 60VMax. In addition to very small outline SOT-23 6L package, these products are available in TO-78 6L, TO-71 6L, PDIP 8L and SOIC 8L packages.

The LS310/11/12/13 is offered with custom electrical specifications called SELXXXX. Contact the factory for modified electrical specifications for these special versions of the LS310/11/12/13 SEL-XXXX.

Refer to LS350/1/2 products for dual PNP counterpart versions.

LS310 Series

Electrical Characteristics @ 25 °C (Unless Otherwise Stated)

SYMBOL	CHARACTERISTICS	LS310	LS311	LS312	LS313		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	25	45	60	45	MIN.	V	I_C = 10µA, I_E = 0
BV_{CEO}	Collector to Emitter Voltage	25	45	60	45	MIN.	V	I_C = 1mA, I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	6.0	6.0	6.0	MIN.	V	I_E = 10µA, I_C = 0
BV_{CCO}	Collector to Collector Voltage	45	45	60	45	MIN.	V	I_C = 10µA, I_E = I_B = 0A
h_{FE}	DC Current Gain	150	150	200	400 1000	MIN. MAX.	--	I_C = 10µA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	150	200	400	MIN.	--	I_C = 100µA, V_{CE} = 5V
h_{FE}	DC Current Gain	150	150	200	400	MIN.	--	I_C = 1mA, V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.25	0.25	0.25	0.25	MAX.	V	I_C = 1mA, I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	0.2	0.2	0.2	0.2	MAX.	nA	I_E = 0, V_{CB} = 5V
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	0.2	MAX.	nA	I_C = 0, V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	2	MAX.	pF	I_E = 0, V_{CB} = 5V, f = 1MHz
C_{C1C2}	Collector to Collector Capacitance	2	2	2	2	MAX.	pF	V_{CC} = 0V
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	1.0	MAX.	µA	V_{CC} = 30V
f_T	Current Gain Bandwidth Product	200	200	200	200	MIN.	MHz	I_C = 1mA, V_{CE} = 5V
en	Voltage Noise	1.3	1.3	1.3	1.3	TYP.	nV/√Hz	VCE = 5V, IC = 1mA F = 1kHz, NBW = 1Hz
en	Voltage Noise	1.5	1.5	1.5	1.5	TYP.	nV/√Hz	VCE = 5V, IC = 1mA f = 10Hz, NBW = 1Hz
en	Voltage Noise	1.8	1.8	1.8	1.8	TYP.	nV/√Hz	VCE = 5V, IC = 100µA F = 1kHz, NBW = 1Hz
en	Voltage Noise	3.8	3.8	3.8	3.8	TYP.	nV/√Hz	VCE = 5V, IC = 100µA F = 10Hz, NBW = 1Hz

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Typical Characteristics

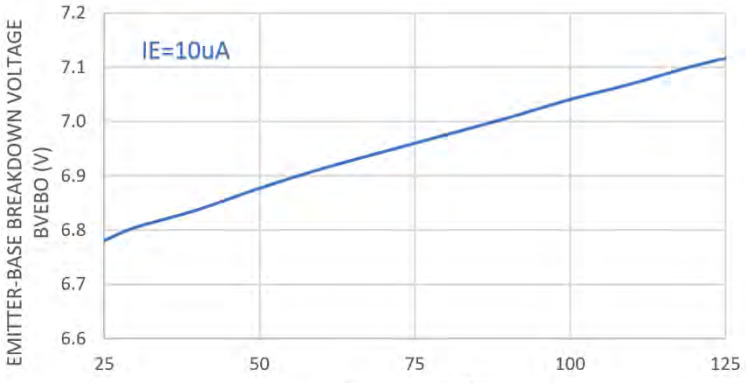


Figure-1 BVEBO(V) vs. Temperature

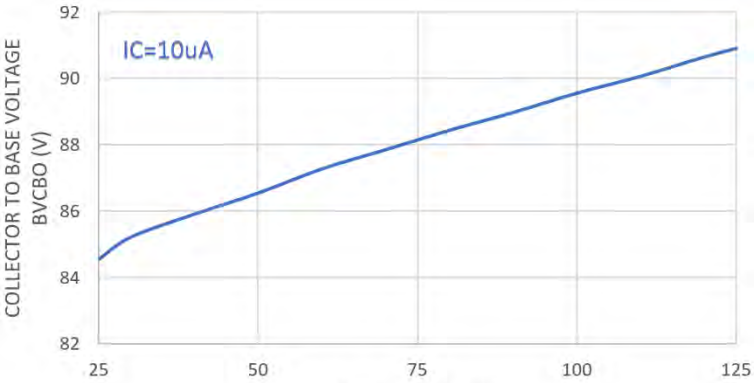


Figure-2 BVCBO(V) vs. Temperature

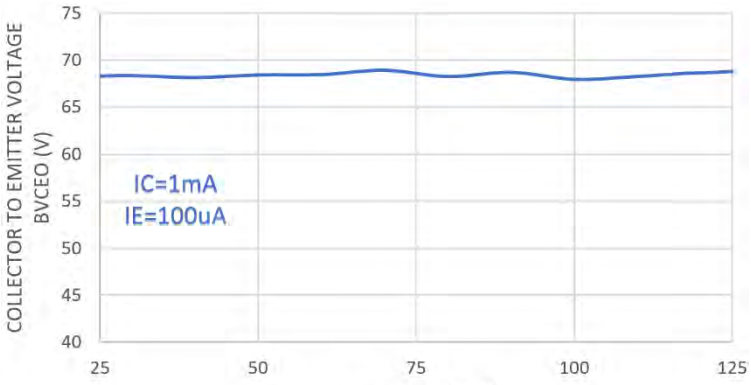


Figure-3 BVCEO(V) vs. Temperature

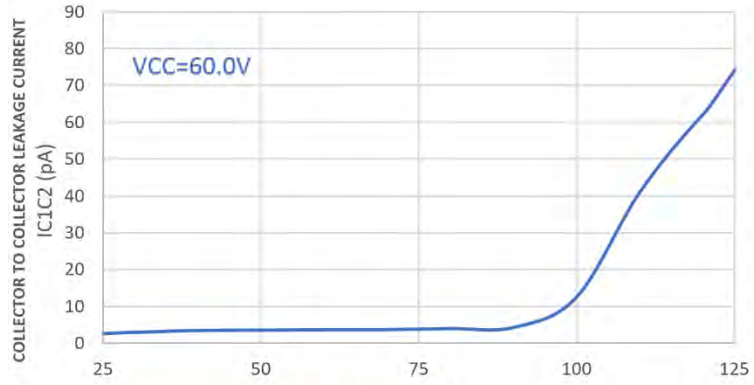


Figure-4 COLLECTOR TO COLLECTOR CURRENT LEAKAGE(pA) vs. Temperature

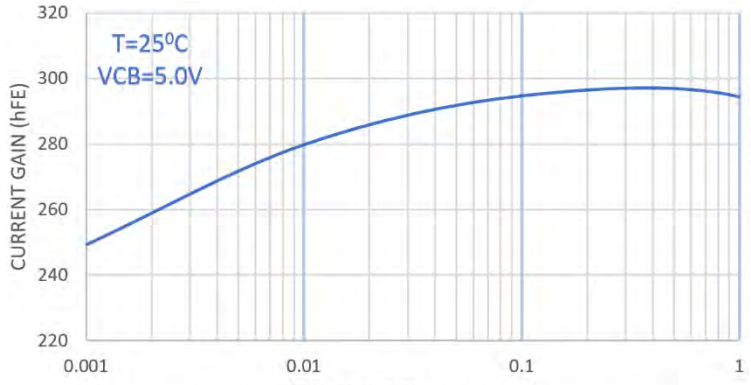


Figure-5 COLLECTOR CURRENT vs. CURRENT GAIN (hFE)

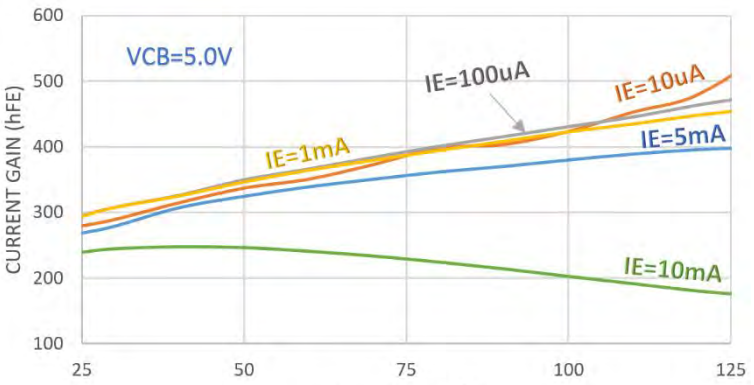


Figure-6 CURRENT GAIN(hFE) vs. Temperature

Typical Characteristics Continued

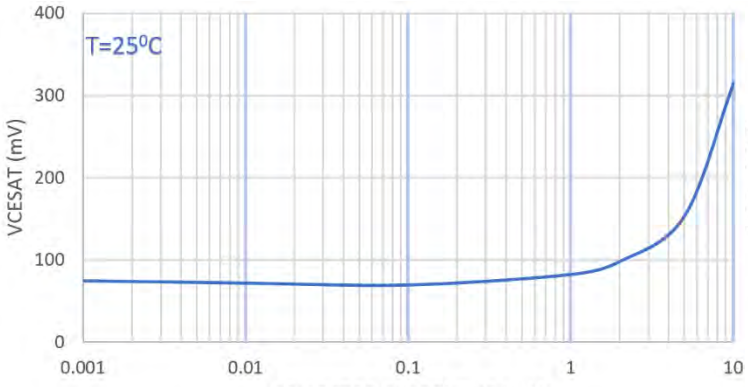


Figure-7 COLLECTOR CURRENT(mA) vs. VCE_{SAT}(mV)

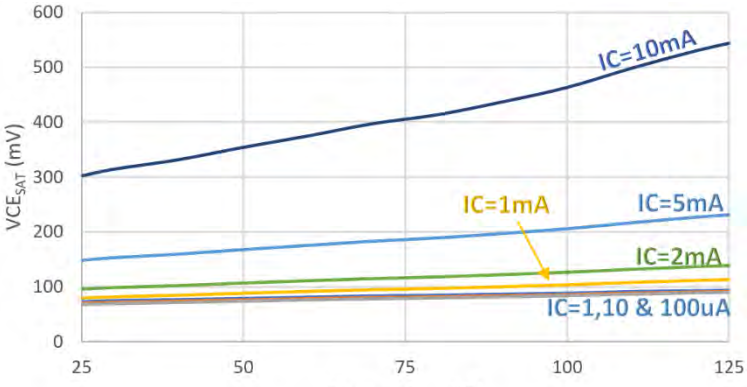


Figure-8 VCE_{SAT}(mV) vs. Temperature

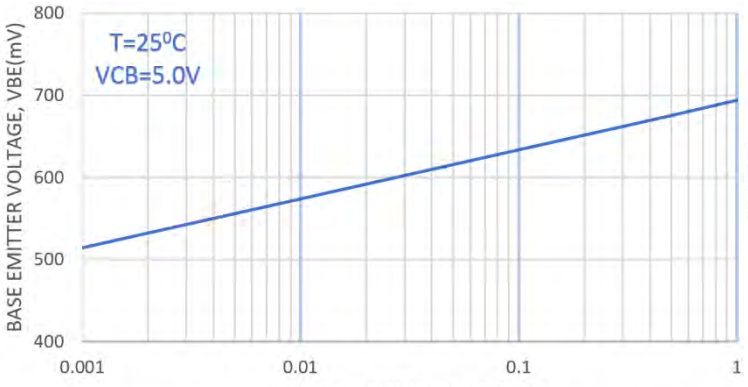


Figure-9 COLLECTOR CURRENT(mA) vs. BASE EMITTER VOLTAGE(V)

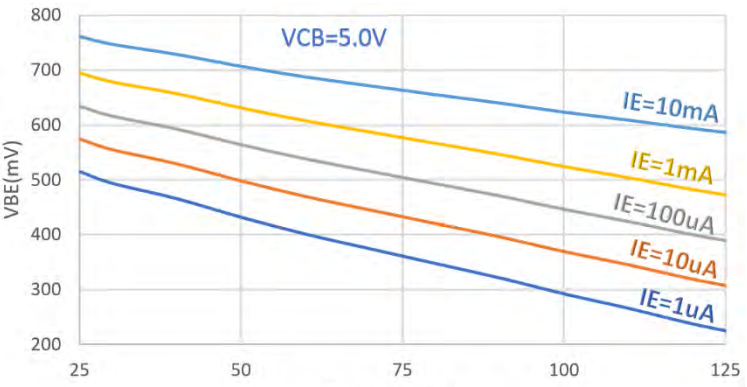


Figure-10 VBE(mV) vs. Temperature

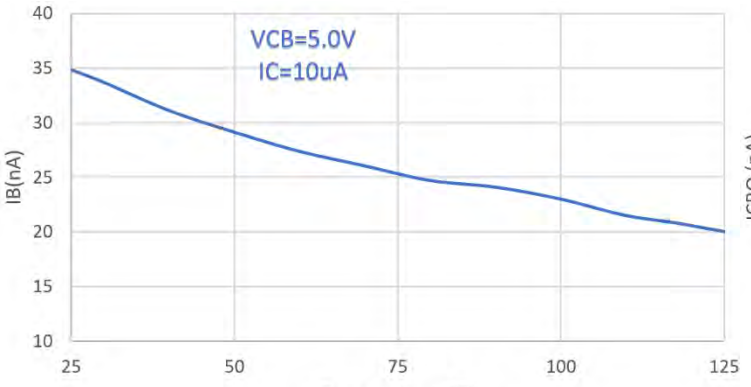


Figure-11 IB(nA) vs. Temperature

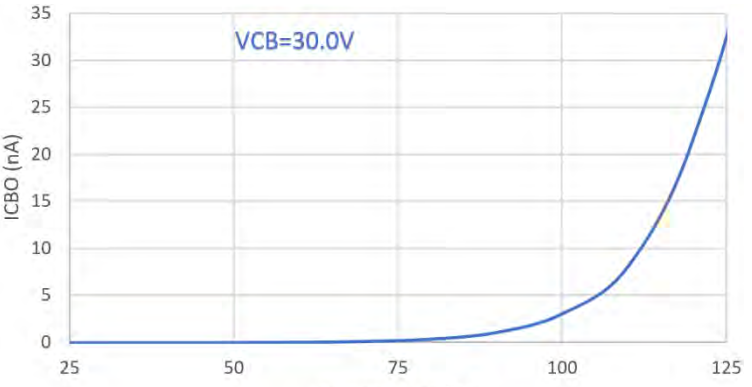


Figure-12 ICBO(nA) vs. Temperature

Typical Characteristics Continued

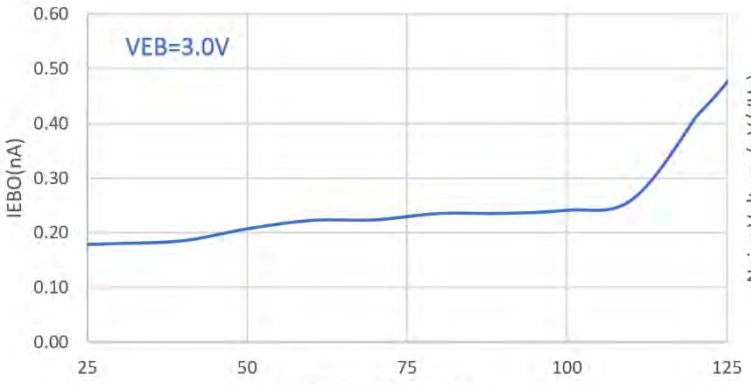


Figure-13 IEBO(nA) vs. Temperature

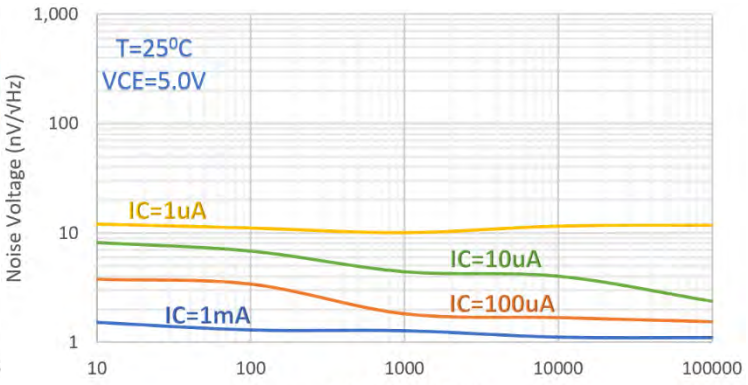


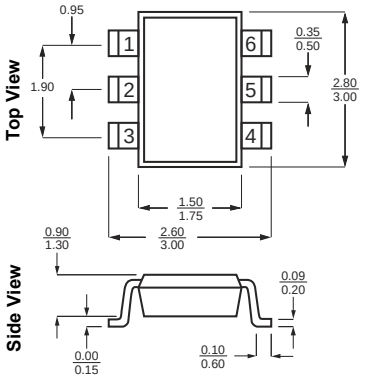
Figure-14 NOISE VOLTAGE vs. FREQUENCY

Ordering Information

Standard Part Call-Out
LS310/311/312/313 TO-71 6L RoHS
LS310/311/312/313 TO-78 6L RoHS
LS310/311/312/313 PDIP 8L RoHS
LS310/311/312/313 SOIC 8L RoHS
LS310/311/312/313 SOT-23 6L RoHS
Custom Part Call-out Custom Parts Include SEL+4 Digit Numeric Code
LS310/311/312/313 TO-71 6L RoHS SELXXXX
LS310/311/312/313 TO-78 6L RoHS SELXXXX
LS310/311/312/313 PDIP 8L RoHS SELXXXX
LS310/311/312/313 SOIC 8L RoHS SELXXXX
LS310/311/312/313 SOT-23 6L RoHS SELXXXX

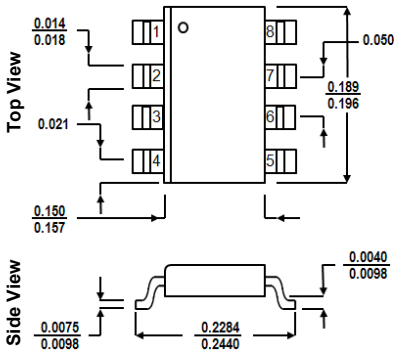
Package Dimensions

SOT-23 6 Lead



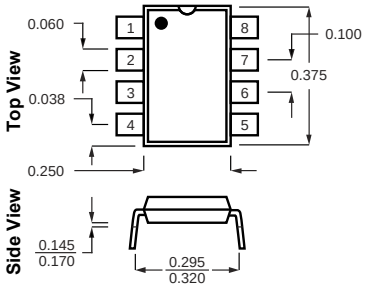
DIMENSIONS IN MILLIMETERS

SOIC-A 8 Lead



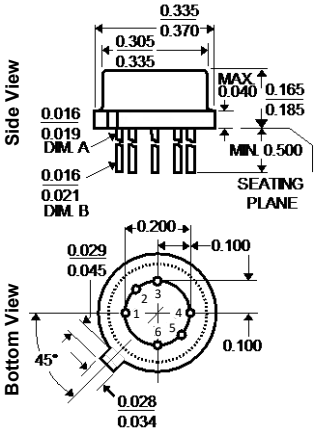
DIMENSIONS IN INCHES

PDIP 8 Lead



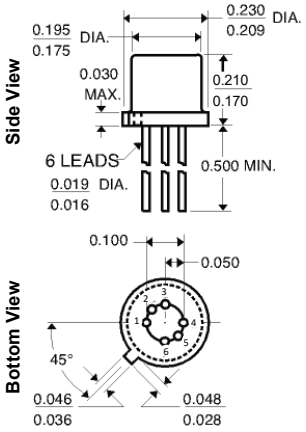
DIMENSIONS IN INCHES

TO-78 6 Lead



DIMENSIONS IN INCHES

TO-71 6 Lead



DIMENSIONS IN INCHES

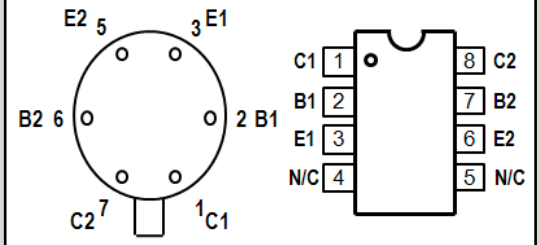
LINEAR SYSTEMS

Improved Standard Products®

LS301 LS302 LS303

HIGH VOLTAGE SUPER-BETA MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
VERY HIGH GAIN	h_{FE} 2000 @ 1.0μA TYP.	
LOW OUTPUT CAPACITANCE	C_{OBO} 2.0pF	
TIGHT V_{BE} MATCHING	$\lvert V_{BE1}-V_{BE2}\rvert$=0.2mV TYP.	
HIGH f_T	100 MHz	
ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise stated)		
I_C	**Collector Current**	**5mA**
Maximum Temperatures		
Storage Temperature	-55 to +150 °C	
Operating Junction Temperature	-55 to +150 °C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation @ Free Air	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO-71 & TO-78 TOP VIEW **SOIC TOP VIEW**

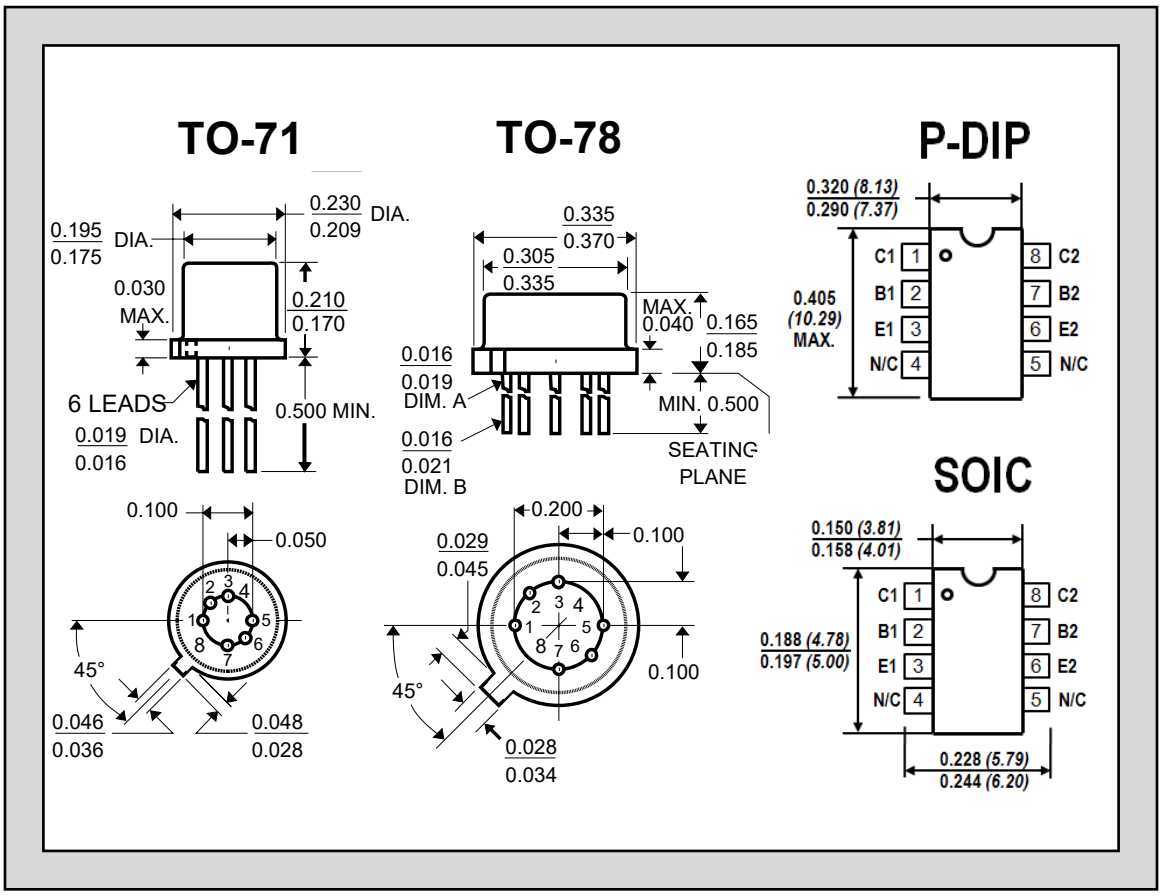
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	LS301	LS302	LS303		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	18	35	10	MIN.	V	I_C = 10μA I_E = 0
BV_{CEO}	Collector to Emitter Voltage	18	35	10	MIN.	V	I_C = 1mA I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	6.0	6.0	MIN.	V	I_E = 10μA I_C = 0 NOTE 2
BV_{CCO}	Collector To Collector Voltage	80	80	20	MIN.	V	I_C = 1μA I_E = I_B = 0
h_{FE}	DC Current Gain	2000	1000	2000	TYP.		I_C = 1μA V_{CE} = 5V
h_{FE}	DC Current Gain	2000	1000	2000	MIN.		I_C = 10μA V_{CE} = 5V
h_{FE}	DC Current Gain	2000	1000	2000	TYP.		I_C = 500μA V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	MAX.	V	I_C = 1mA I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	100	100	100	MAX.	pA	I_E = 0 V_{CB} = NOTE 3
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	MAX.	pA	I_E = 0 V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	MAX.	pF	I_E = 0 V_{CB} = 1V
C_{C1C2}	Collector to Collector Capacitance	2	2	2	MAX.	pF	V_{CC} = 0
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	MAX.	μA	V_{CC} = NOTE 4, I_E = I_B = 0
f_T	Current Gain Bandwidth Product	100	100	100	MIN.	MHz	I_C = 200μA V_{CE} = 5V
NF	Narrow Band Noise Figure	3	3	3	MAX.	dB	I_C = 10μA V_{CE} = 3V BW = 200Hz R_G = 10K f = 1KHz

MATCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LS301	LS302	LS303		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.2	0.2	0.2	TYP.	mV	I_C = 10µA V_{CE} = 5V
		1	1	1	MAX.	mV	
$\lvert(V_{BE1}-V_{BE2})\rvert/°C$	Base Emitter Voltage Differential	1	1	1	TYP.	µV/°C	I_C = 10µA V_{CE} = 5V
	Change with Temperature	5	5	5	MAX.	µV/°C	T = 55°C to +125°C
$\lvert I_{B1}- I_{B2}\rvert$	Base Current Differential	0.5	1	0.5	TYP.	nA	I_C = 10µA V_{CE} = 1V
		1	5	1.5	MAX.	nA	I_C = 10µA V_{CE} = 5V
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	5	5	TYP.	%	I_C = 10µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µAmps.
3. For LS301 & LS302: V_{CB}=10V; for LS303: V_{CB}=5V
4. For LS301 & LS302: V_{CC}=±80V; for LS303: V_{CC}=±20V

LINEAR SYSTEMS

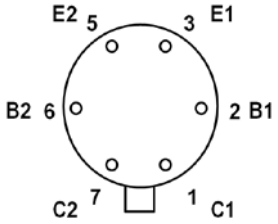
Improved Standard Products®

LS318

LOG CONFORMANCE MONOLITHIC DUAL NPN TRANSISTORS

FEATURES		
LOG CONFORMANCE	Δre =1 TYP.	
ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	10mA
Maximum Temperatures		
Storage Temperature Range		-55°C to +150°C
Operating Junction Temperature		-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO 71 & TO 78
TOP VIEW

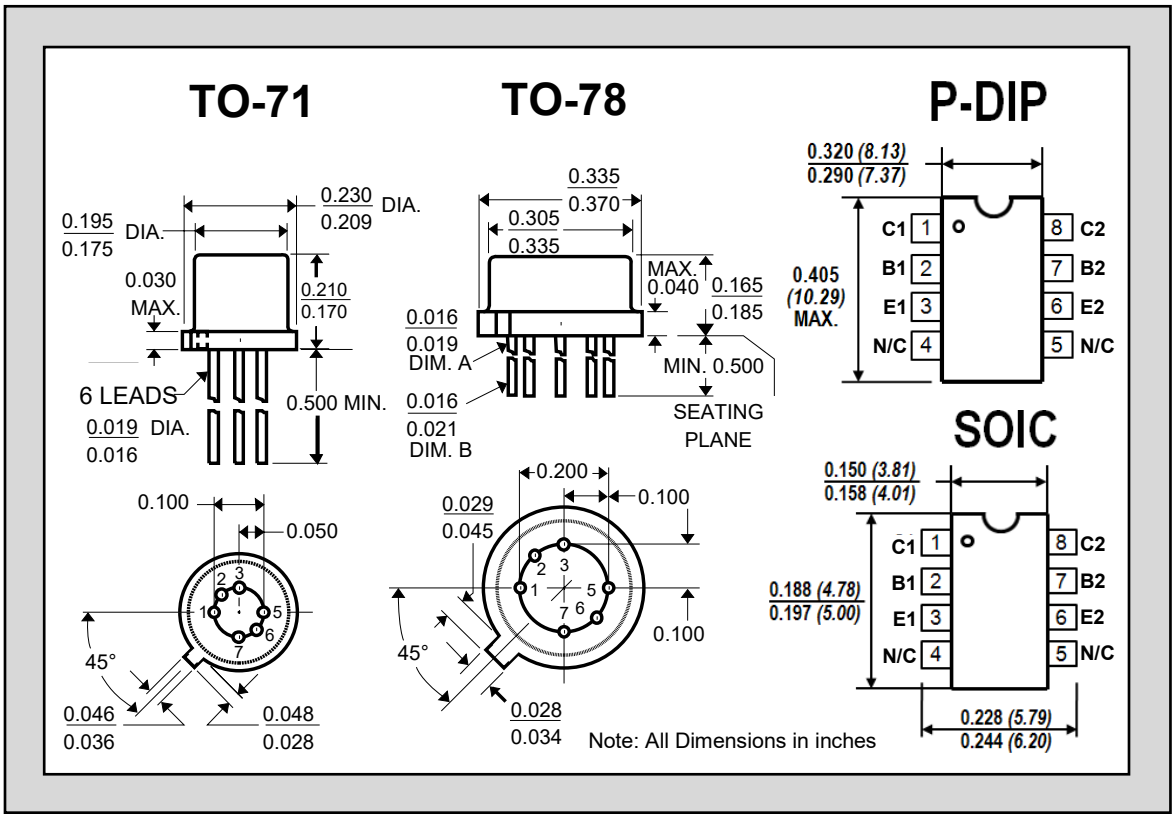
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS318		UNITS	CONDITIONS
Δre	Log Conformance	1.5	MAX.	Ω	I_C = 10-100-1000μA V_{CE} = 5V
BV_{CBO}	Collector-Base Breakdown Voltage	25	MIN.	V	I_C = 10μA I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	25	MIN.	V	I_C = 100μA I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	6.0	MIN.	V	I_E = 10μA I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	45	MIN.	V	I_C = 10μA I_B = I_E =0A
h_{FE}	DC Current Gain	150 600	MIN. MAX.		I_C = 10μA V_{CE} = 5V
h_{FE}	DC Current Gain	150 600	MIN. MAX.		I_C = 100μA V_{CE} = 5V
h_{FE}	DC Current Gain	150	MIN.		I_C = 1mA V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.25	MAX.	V	I_C = 1mA I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current	0.2	MAX.	nA	I_E = 0A V_{CB} = 20V
I_{EBO}	Emitter Cutoff Current	0.2	MAX.	nA	I_C = 0A V_{EB} = 3V
C_{OBO}	Output Capacitance	1.8		pF	I_E = 0A V_{CB} = 3V f=1MHz **NOTE 3**
C_{C1C2}	Collector to Collector Capacitance	1.8		pF	V_{CC} = 0V f=1MHz **NOTE 3**
I_{C1C2}	Collector to Collector Leakage Current	0.5	MAX.	μA	V_{CC} = ±45V I_B = I_E = 0A
f_T	Current Gain Bandwidth Product	220		MHz	I_C = 1mA V_{CE} = 5V **NOTE 3**
NF	Narrow Band Noise Figure	3	MAX.	dB	I_C = 100μA V_{CE} = 5V **NOTE 3** BW = 200Hz, R_G = 10 K f=1KHz

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS318		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.4 1	TYP. MAX.	mV mV	I_C = 10 µA V_{CE} = 5V
$\lvert (V_{BE1}-V_{BE2})\rvert$ /ºC	Base Emitter Voltage Differential Change with Temperature	1	TYP.	µV/°C	I_C = 10 µA V_{CE} = 5V T_A = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	10	MAX.	nA	I_C = 10 µA V_{CE} = 5V
$\lvert (I_{B1}-I_{B2})\rvert$ /ºC	Base Current Differential Change with Temperature	0.4	TYP.	nA/ºC	I_C = 10 µA V_{CE} = 5V T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	TYP.	%	I_C = 10 µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. Not tested; guaranteed by design.
4. All MIN/TYP/MAX values are absolute numbers. Negative signs indicate electrical polarity only.

LINEAR SYSTEMS

Improved Standard Products®

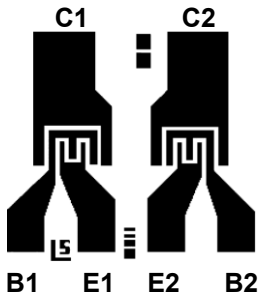
IT130A IT130 IT131 IT132

MONOLITHIC DUAL PNP TRANSISTORS

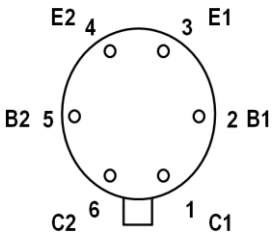
FEATURES
Direct Replacement for Intersil IT130 Series Pin for Pin Compatible

ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	-10mA
Maximum Temperatures		
Storage Temperature Range		-65°C to +150°C
Operating Junction Temperature		-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3W/°C



26 X 29 MILS



TOP VIEW

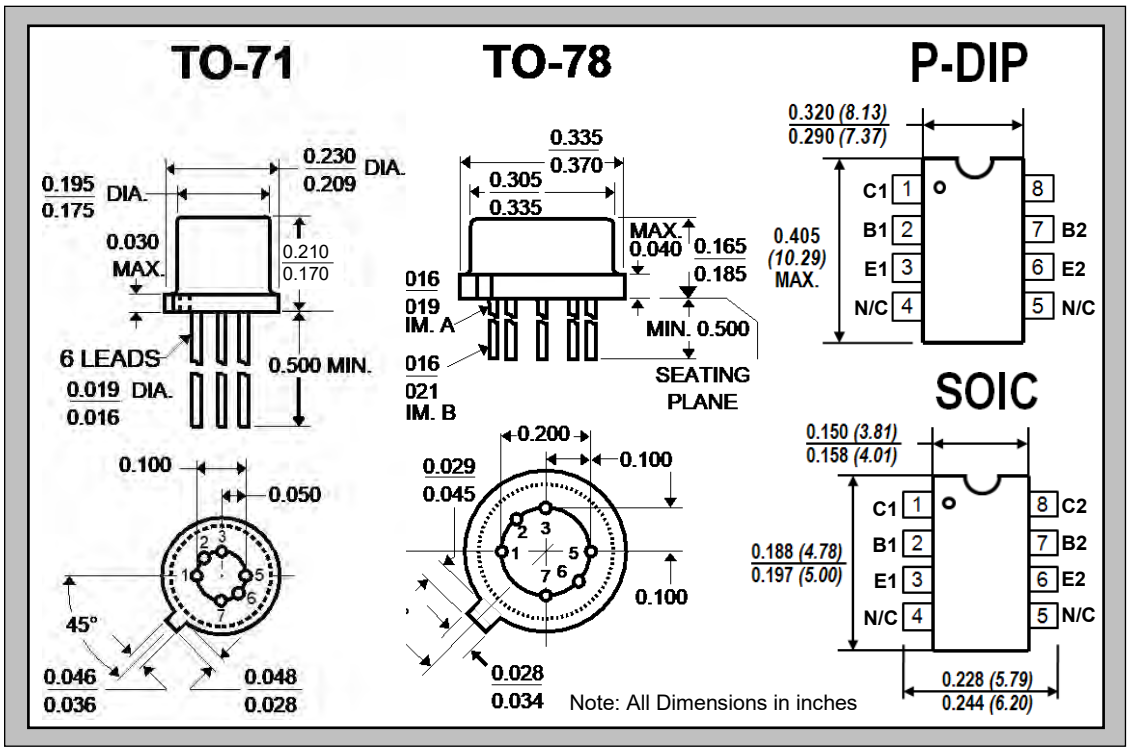
ELECTRICAL CHARACTERISTICS T_A= 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT130A	IT130	IT131	IT132		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	-45	-45	-45	-45	MIN.	V	I_C = -10µA I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	-45	-45	-45	-45	MIN.	V	I_C = -10µA I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	-6.2	-6.2	-6.2	-6.2	MIN.	V	I_E = -10µA I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	±60	±60	±60	±60	MIN.	V	I_{CCO} = ±10µA I_B= I_E=0A
h_{FE}	DC Current Gain	200	200	80	80	MIN.		I_C = -10µA V_{CE} = -5V
		225	225	100	100	MIN.		I_C = -1.0mA V_{CE} = -5V
V_{CE}(SAT)	Collector Saturation Voltage	-0.5	-0.5	-0.5	-0.5	MAX.	V	I_C = -0.5mA I_B = -0.05mA
I_{EBO}	Emitter Cutoff Current	-1	-1	-1	-1	MAX.	nA	I_C = 0A V_{EB} = -3V
I_{CBO}	Collector Cutoff Current	-1	-1	-1	-1	MAX.	nA	I_E = 0A V_{CB} = -45V
C_{OBO}	Output Capacitance[4]	2	2	2	2	MAX.	pF	I_E = 0A V_{CB} = -5V
C_{C1C2}	Collector to Collector Capacitance[4]	4	4	4	4	MAX.	pF	V_{CC} = 0V
I_{C1C2}	Collector to Collector Leakage Current	±500	±500	±500	±500	MAX.	nA	V_{CC} = ±60V, I_B= I_E=0A
f_T	Current Gain Bandwidth Product[4]	110	110	90	90	MIN.	MHz	I_C = -1mA V_{CE} = -5V
NF	Narrow Band Noise Figure[4]	3	3	3	3	MAX.	dB	I_C = -100µA V_{CE} = -5V BW = 200Hz, R_G = 10 KΩ f=1KHz

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	IT130A	IT130	IT131	IT132		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	2	3	5	MAX.	mV	I_C = -10 µA V_{CE} = -5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert/\Delta T$	Base Emitter Voltage Differential	3	5	10	20	MAX.	µV/°C	I_C = 10 µA V_{CE} = 5V
	Change with Temperature[4]							T = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	2.5	5	25	25	MAX.	nA	I_C = -10 µA V_{CE} = -5V

STANDARD PACKAGE DIMENSIONS:



NOTES:

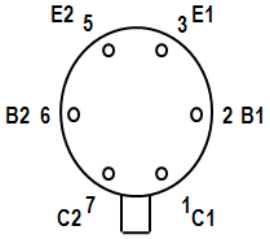
1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Not a production test.

LS350, LS351 & LS352

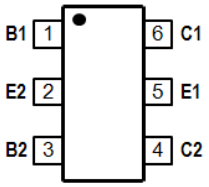
Monolithic Dual PNP Transistors

GENERAL PURPOSE

FEATURES		
HIGH GAIN	h_{FE} 200 @ 10µA - 1mA	
TIGHT V_{BE} MATCHING	$\|V_{BE1}-V_{BE2}\|$=0.2mV TYP.	
HIGH f_T	275 MHz TYP. @ 1mA	
ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise stated)		
I_C	**Collector Current**	**10mA**
Maximum Temperatures		
Storage Temperature	-55° to +150°C	
Operating Junction Temperature	+150°C	
Maximum Power Dissipation	**ONE SIDE**	**BOTH SIDES**
Device Dissipation @ Free Air	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



TO-71 & TO-78 6L
Top View



SOT-23 6 L
Top View

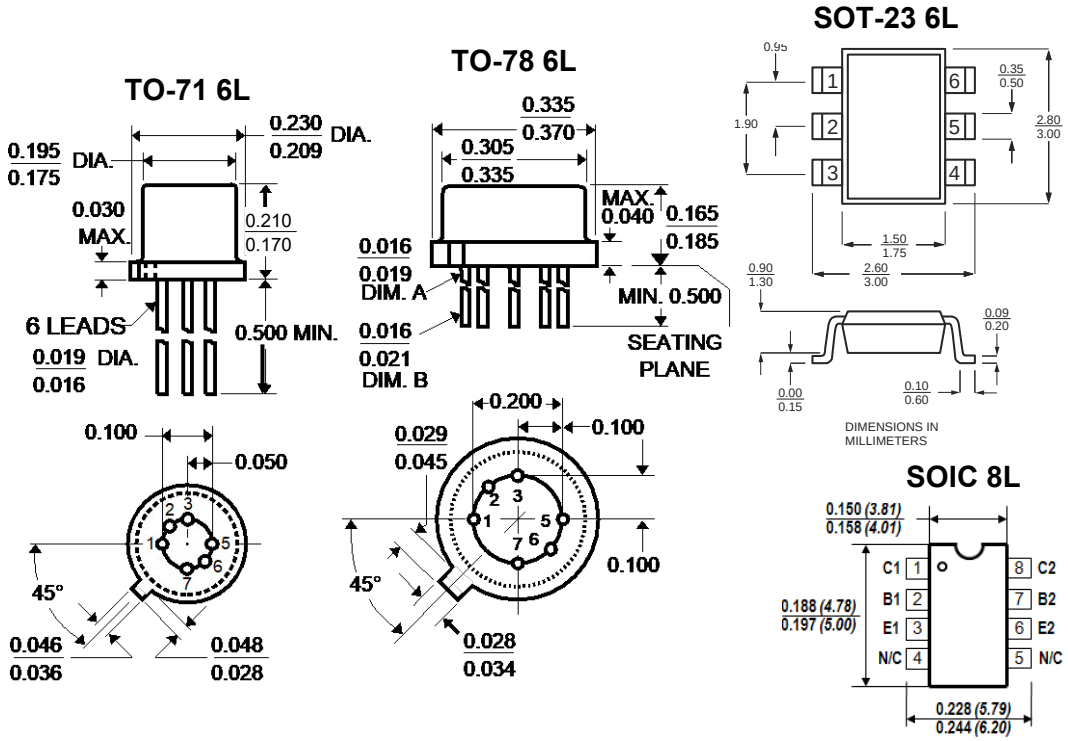
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	LS350	LS351	LS352		UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	25	45	60	MIN.	V	I_C = 10µA I_E = 0
BV_{CEO}	Collector to Emitter Voltage	25	45	60	MIN.	V	I_C = 1mA I_B = 0
BV_{EBO}	Emitter to Base Voltage	6.0	6.0	6.0	MIN.	V	I_E = 10µA I_C = 0 NOTE 2
BV_{CCO}	Collector to Collector Voltage	±25	±45	±80	MIN.	V	I_C = ±1µA I_E = 0 = I_B = 0
h_{FE}	DC Current Gain	100	150 600	200 600	MIN. MAX.		I_C = 10µA V_{CE} = 5V
h_{FE}	DC Current Gain	100	150 600	200 600	MIN. MAX.		I_C = 100µA V_{CE} = 5V
h_{FE}	DC Current Gain	100	150	200	MIN.		I_C = 1mA, V_{CE} = 5V
V_{CE}(SAT)	Collector Saturation Voltage	0.5	0.5	0.5	MAX.	V	I_C = 1mA I_B = 0.1mA
I_{CBO}	Collector Cutoff Current	0.2	0.2	0.2	MAX.	nA	I_E = 0 V_{CB} = NOTE 3
I_{EBO}	Emitter Cutoff Current	0.2	0.2	0.2	MAX.	nA	I_C = 0 V_{EB} = 3V
C_{OBO}	Output Capacitance	2	2	2	MAX.	pF	I_E = 0 V_{CB} = 5V
C_{C1C2}	Collector to Collector Capacitance	2	2	2	MAX.	pF	V_{CC} = 0
I_{C1C2}	Collector to Collector Leakage Current	1.0	1.0	1.0	MAX.	µA	V_{CC} = NOTE 4
f_T	Current Gain Bandwidth Product	200	200	200	MIN.	MHz	I_C = 1mA V_{CE} = 5V
NF	Narrow Band Noise Figure	3	3	3	MAX.	dB	I_C = 100µA V_{CE} = 5V BW = 200Hz R_G = 10K f = 1KHz

MATCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LS350 SOT-23	LS351	LS352		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	1	0.4	0.2	TYP.	mV	I_C = 10 µA V_{CE} = 5V
		5	1.0	0.5	MAX.	mV	
$\lvert(V_{BE1}-V_{BE2})\rvert$/°C	Base Emitter Voltage Differential	2	1	0.5	TYP.	µV/°C	I_C = 10 µA V_{CE} = 5V
	Change with Temperature	20	10	2	MAX.	µV/°C	T_A = -55°C to +125°C
$\lvert I_{B1}- I_{B2}\rvert$	Base Current Differential		5	5	MAX.	nA	I_C = 10µA V_{CE} = 5V
$\lvert(I_{B1}- I_{B2})\rvert$/°C	Base Current Differential		0.5	0.3	MAX.	nA/°C	I_C = 10 µA, V_{CE} = 5V
	Change with Temperature						T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	10	5	5	TYP.	%	I_C = 10µA V_{CE} = 5V

STANDARD PACKAGE DIMENSIONS



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. For LS350: V_{CB}=20V; for LS351 & LS352: V_{CB}=30V.
4. For LS351: V_{CC}=±45V; for LS352: V_{CC}=±80V; for LS350: V_{CC}=±25V.
5. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

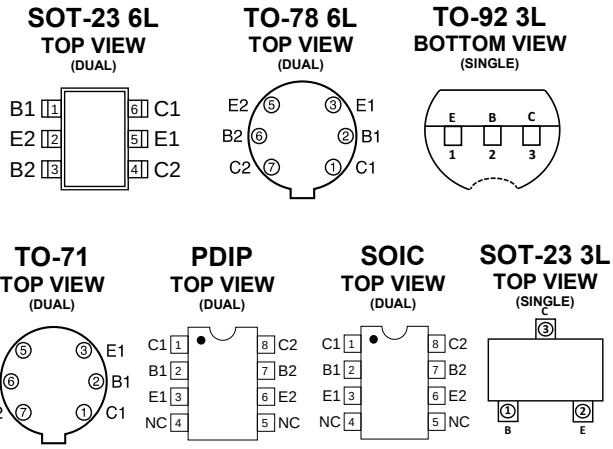
LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

LS3550 SERIES

MONOLITHIC DUAL & SINGLE PNP TRANSISTORS

FEATURES	
6 LEAD SOT-23 SURFACE MOUNT PACKAGE*	
TIGHT MATCHING[1]	2mV
EXCELLENT THERMAL TRACKING[1]	3µV/°C
ABSOLUTE MAXIMUM RATINGS[2] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation	
Continuous Power Dissipation	TBD
Maximum Currents	
Collector Current	50mA
Maximum Voltages	
Collector to Collector Voltage	60V



MATCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated) * MATCHING ELECTRICAL CHARACTERISTICS FOR DUALS ONLY

SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Differential		2		5		10	mV	I_C = -100µA, V_{CE} = -5V
$\frac{\lvert V_{BE1} - V_{BE2} \rvert}{\Delta T}$	Base to Emitter Voltage Differential Change with Temperature		3		5		15	µV/°C	I_C = -100µA, V_{CE} = -5V T_A = -40°C to +85°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential		10		10		10	nA	I_C = -10µA, V_{CE} = -5V
$\frac{\lvert I_{B1} - I_{B2} \rvert}{\Delta T}$	Base Current Differential Change with Temperature		0.5		0.5		1.0	nA/°C	I_C = -10µA, V_{CE} = -5V T_A = -40°C to +85°C
h_{FE1}/h_{FE2}	Current Gain Differential		10		10		15	%	I_C = -1mA, V_{CE} = -5V

ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

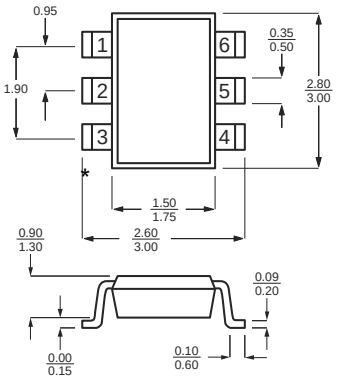
SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{CBO}	Collector to Base Breakdown Voltage	-45		-40		-20		15	I_C = -10µA, I_E = 0A
BV_{CEO}	Collector to Emitter Breakdown Voltage	-45		-40		-20		16	I_C = -5mA, I_B = 0A
BV_{CCO}	Collector to Collector Breakdown Voltage	±60		±60		±60		V	I_{CC} = -±1µA, I_B=I_C =0A
BV_{EBO}	Emitter to Base Breakdown Voltage[3]	-6.0		-6.0		-6.0			I_E = -10µA, I_C = 0A
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage		-0.50		-0.50		-1.2		I_C = -10mA I_B = -1mA

ELECTRICAL CHARACTERISTICS CONT. @25 °C (unless otherwise stated)

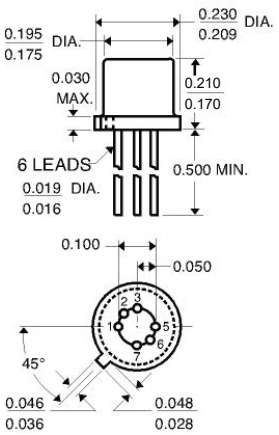
SYMBOL	CHARACTERISTIC	LS3550A		LS3550B		LS3550C		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		100		50			I_C = -1mA, V_{CE} = -5V
		120		80		40			I_C = -10mA, V_{CE} = -5V
		100		60		30			I_C = -35mA, V_{CE} = -5V
I_{CBO}	Collector Cutoff Current		-0.35		-0.35			nA	I_E = 0A, V_{CB} = -30V
							-0.35		I_E = 0A, V_{CB} = -20V
I_{EBO}	Emitter Cutoff Current		-0.35		-0.35		-0.35		I_E = 0A, V_{CB} = -3V
I_{C1C2}	Collector to Collector Leakage Current		±1		±1		±1	µA	V_{CC} = ±60V, I_B=I_C =0A
C_{OBO}	Output Capacitance		2		2		2	pF	I_E = 0A, V_{CB} = -10V
f_T	Gain Bandwidth Product (Current)		600		600		600	MHz	I_C = -1mA, V_{CE} = -5V
NF	Noise Figure (Narrow Band)		3		3		3	dB	I_C = -100µA, V_{CE} = -5V BW = 200Hz R_B = 10Ω, *f* = 1kHz

STANDARD PACKAGE DIMENSIONS:

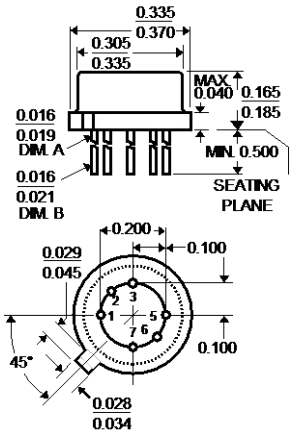
SOT-23 6L



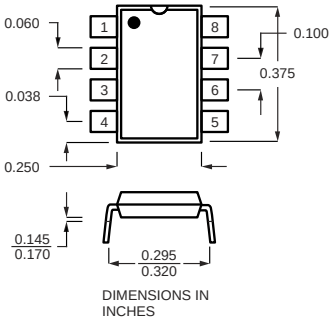
TO-71 6L



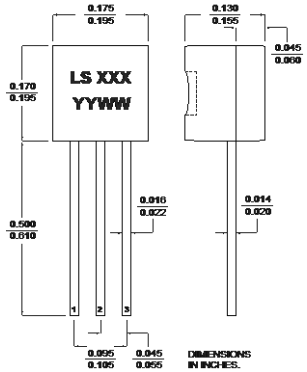
TO-78 6L



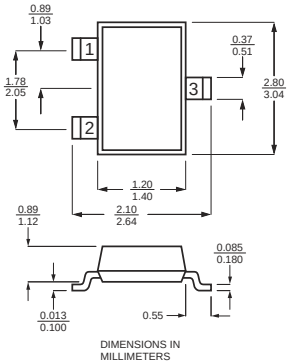
PDIP 8L



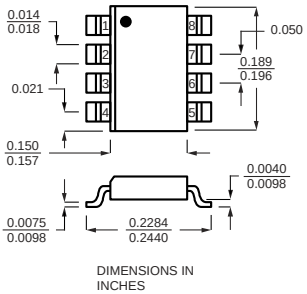
TO-92 3L



SOT-23 3L



SOIC 8L



NOTES:

1. Maximum rating for LS3550A, SOT-23-6L.
2. Absolute maximum ratings are limiting values above which serviceability may be impaired.
3. The reverse Base-to-Emitter voltage must never exceed -6.0 Volts. The reverse Base-to-Emitter current must never exceed -10µA.

LINEAR SYSTEMS

Improved Standard Products®

LS358

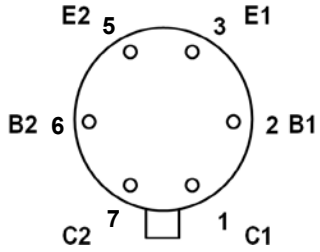
LOG CONFORMANCE MONOLITHIC DUAL PNP TRANSISTORS

FEATURES	
LOG CONFORMANCE	∆re ≤1Ω from ideal TYP.

ABSOLUTE MAXIMUM RATINGS NOTE 1 (T_A= 25°C unless otherwise noted)		
I_C	Collector-Current	-10mA

Maximum Temperatures	
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	-55°C to +150°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation T_A=25°C	250mW	500mW
Linear Derating Factor	2.3mW/°C	4.3mW/°C



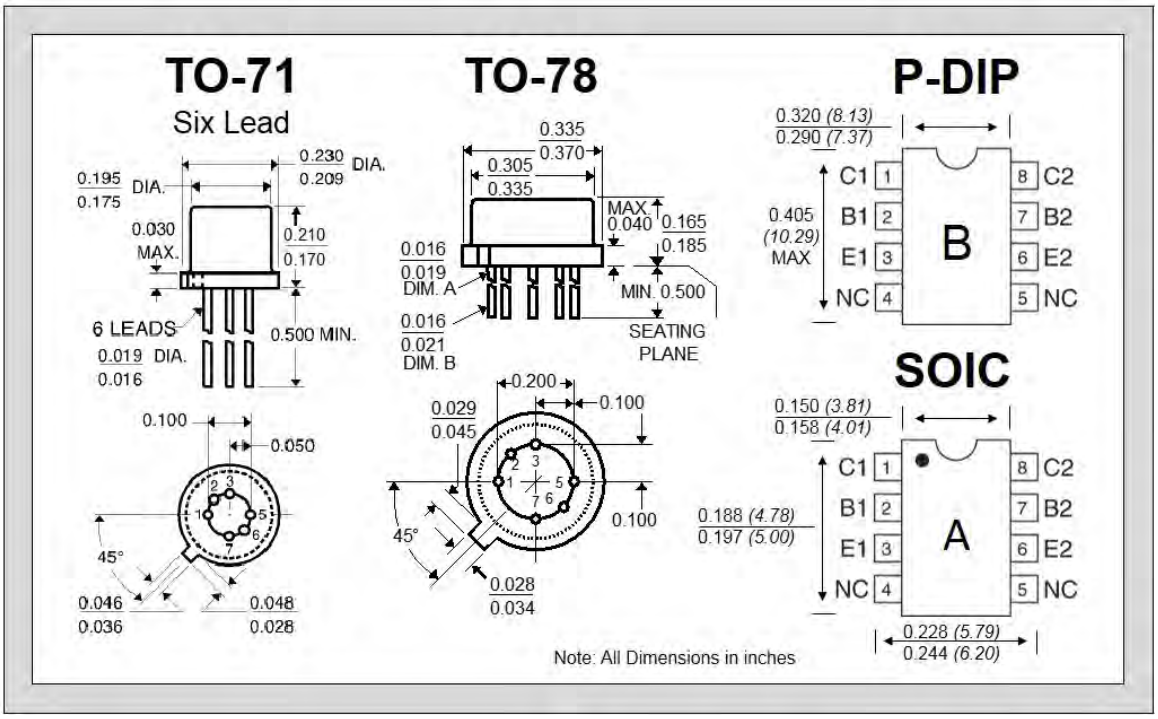
TO-71 & TO-78
TOP VIEW

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS358		UNITS	CONDITIONS	
∆re	Log Conformance	1.5		Ω	I_C = -10-100-1000µA	V_{CE} = -5V
BV_{CBO}	Collector-Base Breakdown Voltage	-20	MIN.	V	I_C = -10µA	I_E = 0A
BV_{CEO}	Collector to Emitter Voltage	-20	MIN.	V	I_C = -1mA	I_B = 0A
BV_{EBO}	Emitter-Base Breakdown Voltage	-6.0	MIN.	V	I_E = -10µA	I_C = 0A **NOTE 2**
BV_{CCO}	Collector to Collector Voltage	45	MIN.	V	I_C = ±10µA, I_B=I_E = 0A	
h_{FE}	DC Current Gain	100 600	MIN. MAX.		I_C = -10µA	V_{CE} = -5V
h_{FE}	DC Current Gain	100 600	MIN. MAX.		I_C = -100µA	V_{CE} = -5V
h_{FE}	DC Current Gain	100	MIN.		I_C = -1mA	V_{CE} = -5V
V_{CE}(SAT)	Collector Saturation Voltage	-0.5	MAX.	V	I_C = -1mA	I_B = -0.1mA
I_{CBO}	Collector Cutoff Current	-0.2	MAX.	nA	I_E = 0A	V_{CB} = -15V
I_{EBO}	Emitter Cutoff Current	-0.2	MAX.	nA	I_C = 0A	V_{EB} = -3V
C_{OBO}	Output Capacitance[4]	2.0	MAX.	pF	I_E = 0A	V_{CB} = -5V
C_{C1C2}	Collector to Collector Capacitance[4]	2.0	MAX.	pF	V_{CC} = 0V	
I_{C1C2}	Collector to Collector Leakage Current	±0.5	MAX.	µA	V_{CC} = ±45V	I_B = I_E = 0A
f_T	Current Gain Bandwidth Product[4]	200	MIN.	MHz	I_C = -1mA	V_{CE} = -5V
NF	Narrow Band Noise Figure[4]	3.0	MAX.	dB	I_C = -100µA BW = 200Hz f=1KHz	V_{CE} = -5V R_G = 10 KΩ

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS358		UNITS	CONDITIONS
$\lvert V_{BE1}-V_{BE2}\rvert$	Base Emitter Voltage Differential	0.4 1	TYP. MAX.	mV mV	I_C = -10 µA V_{CE} = -5V
$\Delta\lvert (V_{BE1}-V_{BE2})\rvert$/°C	Base Emitter Voltage Differential[4] Change with Temperature	1	TYP.	µV/°C	I_C = -10 µA V_{CE} = -5V T_A = -55°C to +125°C
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential	5	MAX.	nA	I_C = -10 µA V_{CE} = -5V
$\lvert \Delta (I_{B1}-I_{B2})\rvert$/°C	Base Current Differential[4] Change with Temperature	0.5	TYP.	nA/°C	I_C = -10 µA V_{CE} = -5V T_A = -55°C to +125°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	5	TYP.	%	I_C = -10 µA V_{CE} = -5V



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. The reverse base-to-emitter voltage must never exceed 6.0 volts; the reverse base-to-emitter current must never exceed 10 µA.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Not tested; guaranteed by design.

LINEAR SYSTEMS

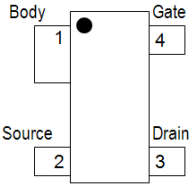
Improved Standard Products®

3N170 3N171

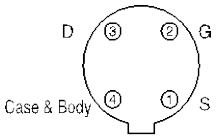
N-CHANNEL MOSFET ENHANCEMENT MODE

FEATURES	
Direct Replacement for INTERSIL 3N170 & 3N171	
LOW DRAIN TO SOURCE RESISTANCE	$r_{ds(on)} \leq 200\Omega$
FAST SWITCHING	$t_{d(on)} \leq 3.0ns$
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
Maximum Current	
Drain to Source	30mA
Maximum Voltages	
Drain to Gate	±35V
Drain to Source	25V
Gate to Source	±35V

3N170 & 3N171
SOT-143 4L
Top View



3N170 & 3N171
TO-72 4L
Top View



ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated) (V_{SB} = 0V unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage		25			V	I_D = 10µA, V_{GS} = 0V
$V_{DS(on)}$	Drain to Source "On" Voltage				2.0		I_D = 10mA, V_{GS} = 10V
$V_{GS(th)}$	Gate to Source Threshold Voltage	3N170	1.0		2.0		V_{DS} = 10V, I_D = 10µA
		3N171	1.5		3.0		
I_{GSS}	Gate Leakage Current				10	pA	V_{GS} = -35V, V_{DS} = 0V
I_{DSS}	Drain Leakage Current "Off"				10	nA	V_{DS} = 10V, V_{GS} = 0V
$I_{D(on)}$	Drain Current "On"		10			mA	V_{GS} = 10V, V_{DS} = 10V
g_{fs}	Forward Transconductance		1000			µS	V_{DS} = 10V, I_D = 2.0mA, *f* = 1.0kHz
$r_{ds(on)}$	Drain to Source "On" Resistance				200	Ω	V_{GS} = 10V, I_D = 100µA, *f* = 1.0kHz
C_{rss}	Reverse Transfer Capacitance				1.3	pF	V_{DS} = 0V, V_{GS} = 0V, *f* = 1.0MHz
C_{iss}	Input Capacitance				5.0		V_{DS} = 10V, V_{GS} = 0V, *f* = 1.0MHz
C_{db}	Drain to Body Capacitance				5.0		V_{DB} = 10V, *f* = 1.0MHz

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$	Turn On Delay Time			3.0	ns	V_{DD} = 10V, $ID_{D(on)}$ = 10mA, $V_{GS(on)}$ = 10V, $V_{GS(off)}$ = 0V R_G = 50Ω
t_r	Turn On Rise Time			10		
$t_{d(off)}$	Turn Off Delay Time			3.0		
t_f	Turn Off Fall Time			15		

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.

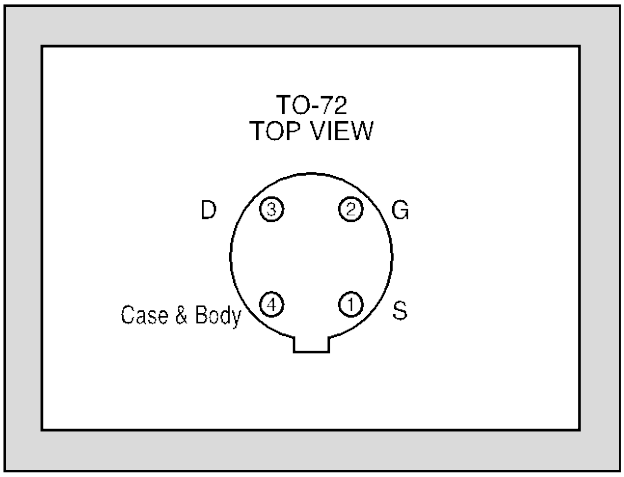
LINEAR SYSTEMS

Improved Standard Products®

2N4351

N-CHANNEL MOSFET ENHANCEMENT MODE

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL 2N4351	
HIGH DRAIN CURRENT	I_D = 20mA
HIGH GAIN	g_{fs} = 1000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +150 °C
Maximum Power Dissipation, T_A=25°C	
Continuous Power Dissipation[3]	350mW
Maximum Current	
Drain to Source	20mA
Maximum Voltages	
Drain to Body	25V
Drain to Source	25V
Gate to Source	±30V

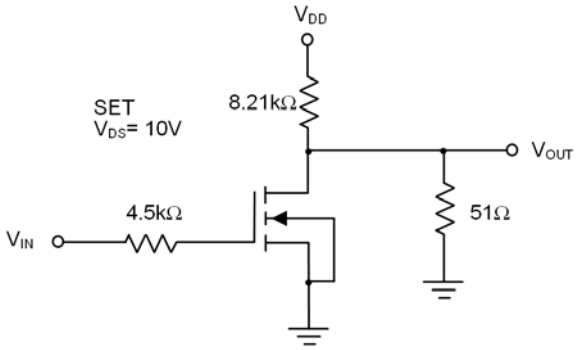


ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated) (V_{SB} = 0V unless otherwise stated)

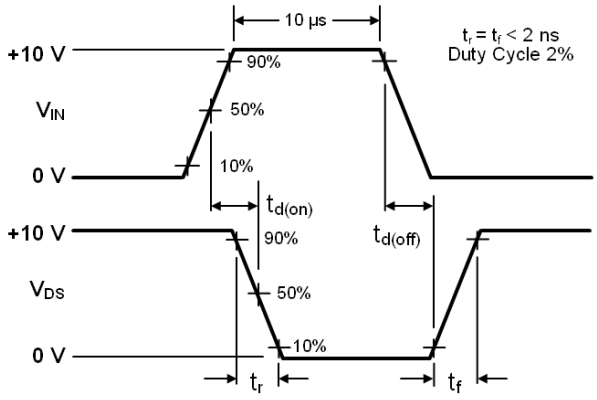
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	25			V	I_D = 10µA, V_{GS} = 0V
$V_{DS(on)}$	Drain to Source "On" Voltage			1		I_D = 2mA, V_{GS} = 10V
$V_{GS(th)}$	Gate to Source Threshold Voltage	1		5		V_{DS} = 10V, I_D = 10µA
I_{GSS}	Gate Leakage Current			±10	pA	V_{GS} = ±30V, V_{DS} = 0V
I_{DSS}	Drain Leakage Current "Off"			10	nA	V_{DS} = 10V, V_{GS} = 0V
$I_{D(on)}$	Drain Current "On"	3			mA	V_{GS} = 10V, V_{DS} = 10V
g_{fs}	Forward Transconductance	1000			µS	V_{DS} = 10V, I_D = 2mA, *f* = 1kHz
$r_{ds(on)}$	Drain to Source "On" Resistance			300	Ω	V_{GS} = 10V, I_D = 100uA, *f* = 1kHz
C_{rss}	Reverse Transfer Capacitance[2]			1.3	pF	V_{DS} = 0V, V_{GS} = 0V, *f* = 140kHz
C_{iss}	Input Capacitance[2]			5.0		V_{DS} = 10V, V_{GS} = 0V, *f* = 140kHz
C_{db}	Drain to Body Capacitance[2]			5.0		V_{DB} = 10V, *f* = 140kHz

SYMBOL	CHARACTERISTIC	MAX	UNITS
$t_{d(on)}$	Turn On Delay Time[2]	45	ns
t_r	Turn On Rise Time[2]	65	
$t_{d(off)}$	Turn Off Delay Time[2]	60	
t_f	Turn Off Fall Time[2]	100	

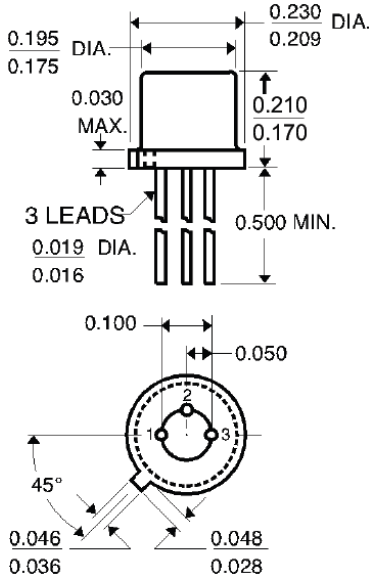
SWITCHING TEST CIRCUIT



TIMING WAVEFORMS



TO-72
4 LEAD



DIMENSIONS IN INCHES

NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.

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2. Not a production test. Guaranteed by design.
3. Derate 2.8 mW ºC above 25 ºC.

LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

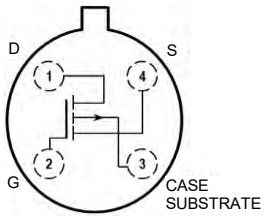
3N163 and 3N164

P-Channel Enhancement Mode MOSFET

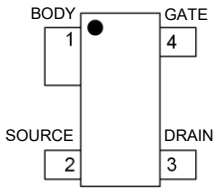
VERY HIGH INPUT IMPEDANCE, HIGH GATE BREAKDOWN, FAST SWITCHING, LOW CAPACITANCE

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
FAST SWITCHING	
LOW CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS	
@ 25°C (unless otherwise stated)	
Drain-Source or Drain-Gate Voltage	
3N163	-40V
3N164	-30V
Drain Current	50mA
Storage Temperature	-55ºC to +150ºC
Power Dissipation TO-72 case	375mW[2]
Power Dissipation SOT-143 case	350mW[3]

TO-72 4L
TOP VIEW



SOT-143 4L
TOP VIEW



TO-72 4L
PACKAGE
PHOTO

SOT-143 4L
TOP VIEW

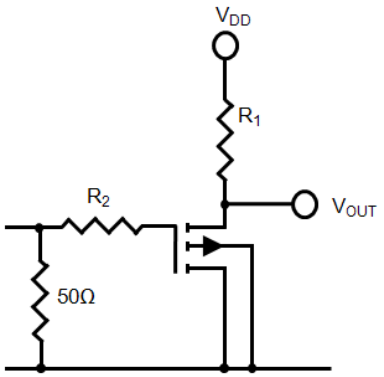
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	3N163		3N164		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Leakage Current		-10		-10	pA	V_{GS}=-40V, V_{DS}=0 (3N163), V_{SB}=0V
	T_A=+125ºC		-25		-25		V_{GS}=-30V, V_{DS}=0 (3N164), V_{SB}=0V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30			I_D=-10µA V_{GS}=0, V_{BS}=0
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30		V	I_S=-10µA V_{GD}=0, V_{BD}=0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0		V_{DS}=V_{GS} I_D=-10µA, V_{SB}=0V
V_{GS}	Gate Source Voltage (on)	-3.0	-6.5	-3.0	-6.5		V_{DS}=-15V I_D=-0.5mA, V_{SB}=0V
I_{DSS}	Zero Gate Voltage, Drain Current (off)		-200		-400	pA	V_{DS}=-15V V_{GS}=0, V_{SB}=0V
I_{SDS}	Zero Gate Voltage, Source Current		-400		-800		V_{SD}=-15V V_{GS}=0, V_{DB}=0V
$R_{DS(on)}$	Drain-Source on Resistance		250		300	ohms	V_{GS}=-20V I_D=-100µA, V_{SB}=0V
$I_{D(on)}$	On Drain Current	-5.0	-30	-3.0	-30	mA	V_{DS}=-15V V_{GS}=-10V, V_{SB}=0V
g_{fs}	Forward Transconductance	2.0	4.0	1.0	4.0	mS	V_{DS}=-15V I_D=-10mA f=1kHz
g_{og}	Output Admittance		250		250	µS	
C_{iss}	Input Capacitance-Output Shorted		3.5		3.5	pF	V_{DS}=-15V I_D=-10mA [1] f=1MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7		
C_{oss}	Output Capacitance Input Shorted		3.0		3.0		

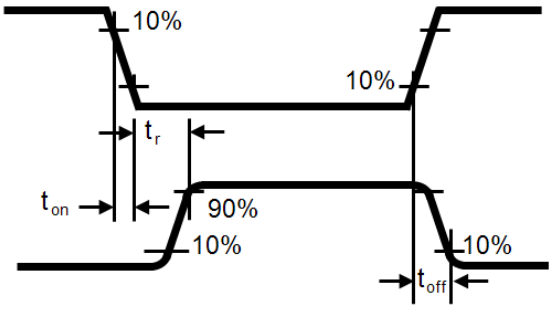
SWITCHING CHARACTERISTICS T_A=25°C and V_{BS}=0 (unless otherwise noted)

SYMBOL	CHARACTERISTIC	3N163		3N164		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{on}	Turn-On Delay Time		12		12	ns	V_{DD}=-15V, V_{SB}=0V $I_{D(on)}$=-10mA[1] R_G=R_L=1.4K
t_r	Rise Time		24		24		
t_{off}	Turn-Off Time		50		50		

Switching Times Test Circuit



TYPICAL SWITCHING WAVEFORM

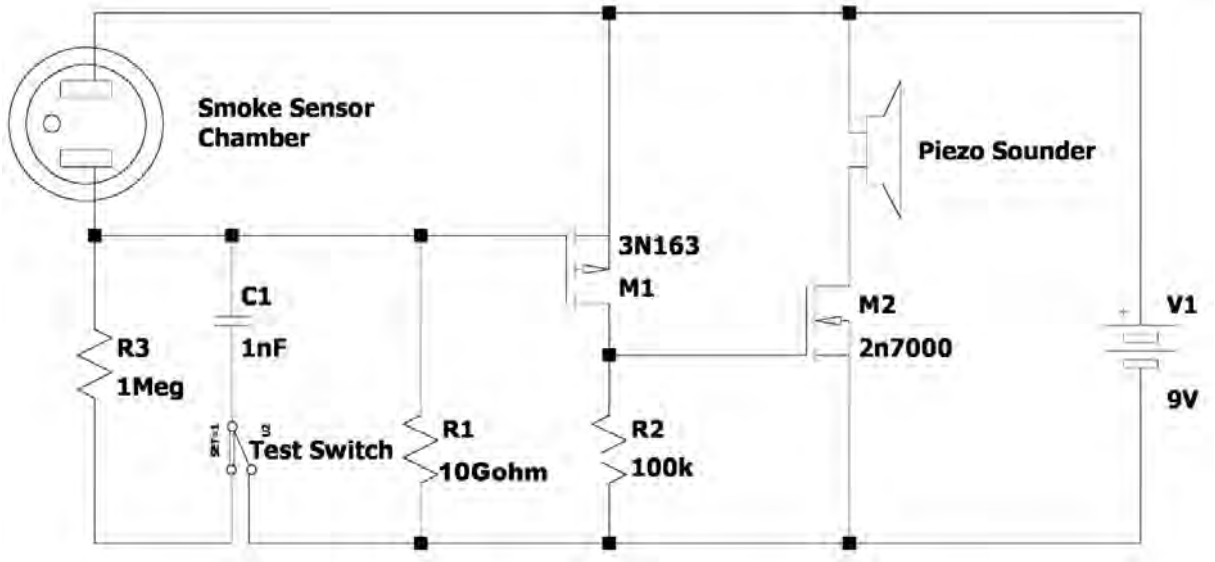


INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Simplest Possible Smoke Detector

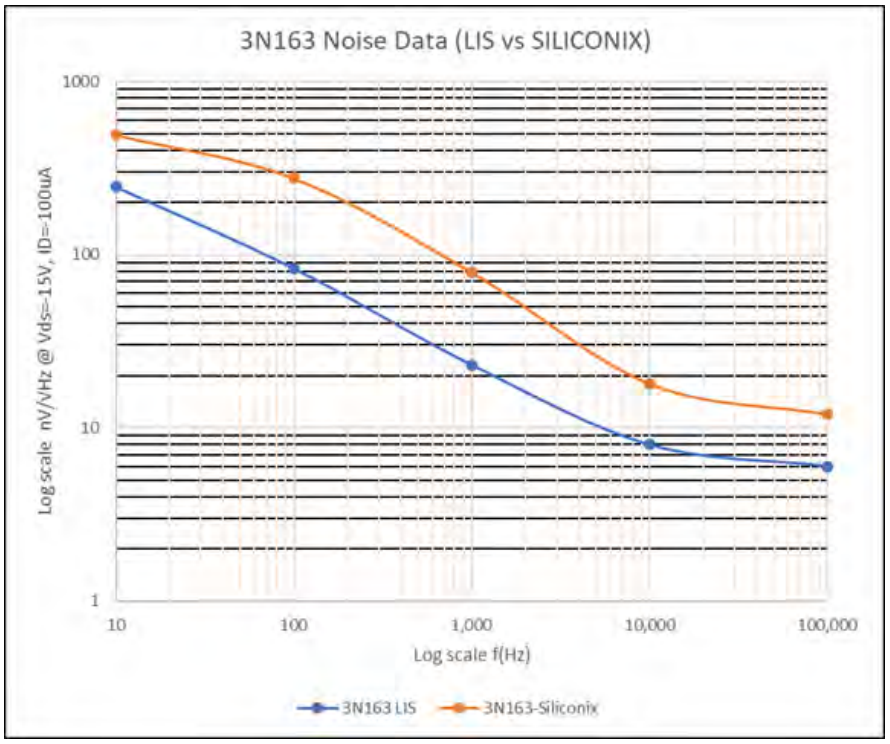
KRL 09/26/2021



NOTES:

1. For design reference only, not 100% tested.
2. Derate 3mW/ºC above 25ºC
3. Derate 3.5mW/ºC above 25ºC
4. All min/max limits are absolute numbers. Negative signs indicate electrical polarity only.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



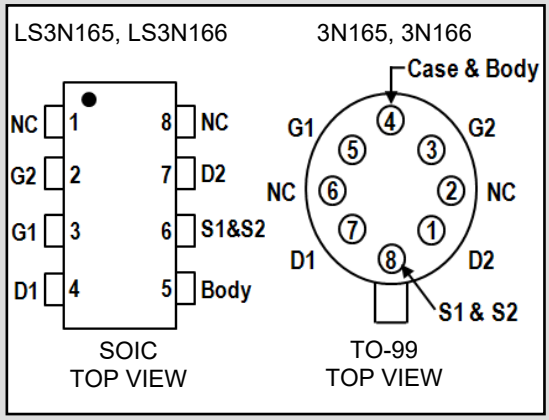
LINEAR SYSTEMS

Improved Standard Products®

3N/LS165, 3N/LS166

MONOLITHIC DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
LOW CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS (NOTE 1) (T_A=25°C unless otherwise noted)	
Drain-Source or Drain-Gate Voltage **(NOTE 2)**	
3N165	40 V
3N166	30 V
Gate-Gate Voltage	±80 V
Drain Current **(NOTE 2)**	50 mA
Storage Temperature	-55ºC to +150ºC
Operating Temperature	-55ºC to +150ºC
Lead Temperature (Soldering, 10 sec.)	+300ºC
Power Dissipation (One Side)	300 mW
Total Derating above 25ºC	4.2 mW/ºC

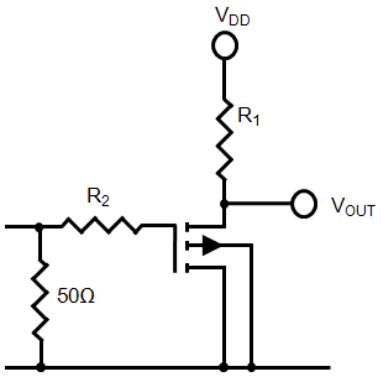


ELECTRICAL CHARACTERISTICS (T_A=25°C and V_{BS}=0 unless otherwise noted)

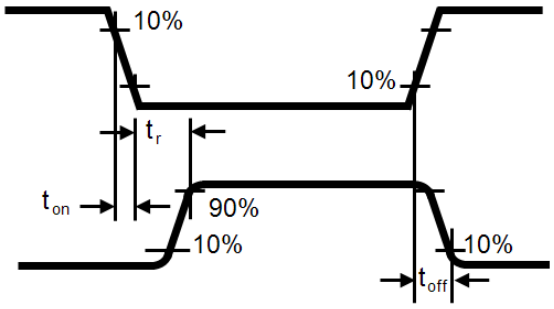
SYMBOL	CHARACTERISTIC	3N165 & 3N166 MIN	3N165 & 3N166 MAX	LS3N165 & LS3N166 MIN	LS3N165 & LS3N166 MAX	UNITS	CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current	--	10	--	100	pA	V_{GS}=40V
I_{GSSF}	Gate Forward Leakage Current	--	-10	--	-100	pA	V_{GS}=-40V
		--	-25	--	--	pA	T_A=+125ºC
I_{DSS}	Drain to Source Leakage Current	--	-200		-200	pA	V_{DS}=-20 V, V_{GS}=V_{BS}=0V
I_{SDS}	Source to Drain Leakage Current	--	-400	--	-400	pA	V_{SD}=-20 V, V_{GD}=V_{DB}=0V
$I_{D(on)}$	On Drain Current	-5	-30	-5	-30	mA	V_{DS}=-15V V_{GS}=-10 V V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=-15V I_D=-10µA V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=V_{GS} I_D=-10µA V_{SB}=0V
$r_{DS(on)}$	Drain Source ON Resistance	--	300	--	300	ohms	V_{GS}=-20V I_D=-100µA V_{SB}=0V
g_{fs}	Forward Transconductance	1500	3000	1500	3000	µS	V_{DS}=-15V I_D=-10mA f=1kHz
g_{os}	Output Admittance	--	300	--	300	µS	V_{SB}=0V
C_{lss}	Input Capacitance	--	3.0	--	3.0	pF	
C_{rss}	Reverse Transfer Capacitance	--	0.7	--	1.0	pF	V_{DS}=-15V I_D=-10mA f=1MHz
C_{oss}	Output Capacitance	--	3.0	--	3.0	pF	**(NOTE 3)** V_{SB}=0V
$R_E(Y_{ls})$	Common Source Forward Transconductance	1200	--			µS	V_{DS}=-15V I_D=-10mA f=100MHz **(NOTE 3)** V_{SB}=0V

MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
G_{fs1}/G_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS}=-15V I_D=-500 µA f=1kHz V_{SB}=0V
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS}=-15V I_D=-500 µA V_{SB}=0V
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/ºC	V_{DS}=-15V I_D=-500 µA V_{SB}=0V T_A=-55ºC to = +125ºC



TYPICAL SWITCHING WAVEFORM



INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Typical Switching Time Test Circuit

NOTES:

1. MOS field effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
   To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.
2. Per transistor.
3. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3N190/3N191

Dual P-Channel Enhancement Mode MOSFET

LOW TOTAL HARMONIC DISTORTION (THD) AND VOLTAGE NOISE MOSFET

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL 3N190 & 3N191	
LOW GATE LEAKAGE CURRENT	I_{GSS} ≤ ±10pA
LOW TRANSFER CAPACITANCE	C_{rss} ≤ 1.0pF
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150 °C
Operating Junction Temperature	-55 to +135 °C
Maximum Power Dissipation @ TA=25ºC	
Continuous Power Dissipation One Side	300mW
Continuous Power Dissipation Both Sides	525mW
Maximum Current	
Drain to Source[2]	30mA
Maximum Voltages	
Drain to Gate[2]	40V
Drain to Source[2]	40V
Gate to Gate	±60V

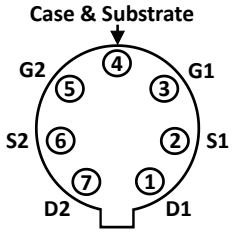
Package Photo

TO-78 7L

Side View

Pin Configuration

TO-78 7L



Top View

Features

- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance
- High Switching Frequency

Benefits

- Minimal Response Time.
- Generates less heat loss compared to BJT at high currents.
- Great at amplifying analog signals.
- Reduces design complexity in medium and low power applications.
- Ideal Choice for high-side switches.
- Simplified gate driving technique reduces overall cost.

Applications

- Switching Applications
- Amplifying Circuits
- Chopper Circuits
- High-Frequency Amplifier
- Voltage Regulator Circuits
- Inverter
- DC Brushless Motor Drives
- DC Relay
- Digital Circuits

Description

The 3N190/3N191 Series is a Dual, P-Channel, Enhancement Mode MOSFET. The MOSFET is a voltage controlled solid state device. The simplicity of the design is advantageous for non-isolated POL(Point of Load) power supplies and low-voltage drives applications, where space is limited. The simplified gate driving technique is often a beneficial characteristic for designers because it reduces overall cost. The 3N190/3N191 Series has a very high switching frequency so that they are used in high-speed load switching, given their minimal response time. The 3N190/3N191 can be used for digital control of higher current and higher voltage loads than the ratings that a microcontroller can withstand. They are great at amplifying analog signals, especially in audio applications. They have multiple functions in different types of applications and can also be used as a chopper or regulator. The 3N190 and 3N191 are the same products as a second source for Intersil products.

MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
g_{fs1}/g_{fs2}	Forward Transconductance Ratio	0.85	-	1.0	-	V_{DS} = -15V, I_D = -500µA, *f* = 1kHz
V_{GS1-2}	Gate to Source Threshold Voltage Differential	-	-	100	mV	V_{DS} = -15V, I_D = -500µA
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate to Source Threshold Voltage Differential with Temperature[4]	-	50	-	µV/°C	V_{DS} = -15V, I_D = -500µA T_S = -55 to +25 °C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate to Source Threshold Voltage Differential with Temperature[4]	-	50	-		V_{DS} = -15V, I_D = -500µA T_S = +25 to +125 °C

ELECTRICAL CHARACTERISTICS @ 25 °C

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40	-	-	V	I_D = -10µA
BV_{SDS}	Source to Drain Breakdown Voltage	-40	-	-		I_S = -10µA, V_{BD} = 0V
V_{GS}	Gate to Source Voltage	-3.0	-	-6.5		V_{DS} = -15V, I_D = -500µA
$V_{GS(th)}$	Gate to Source Threshold Voltage	-2.0	-	-5.0		V_{DS} = V_{GS}, I_D = -10µA
		-2.0	-	-5.0		V_{DS} = -15V, I_D = -500µA
I_{GSSR}	Reverse Gate Leakage Current	-	-	10	pA	V_{GS} = 40V
I_{GSSF}	Forward Gate Leakage Current	-	-	-10		V_{GS} = -40V
I_{DSS}	Drain Leakage Current "Off"	-	-	-200		V_{DS} = -15V
I_{SDS}	Source to Drain Leakage Current "Off"	-	-	-400		V_{SD} = -15V, V_{DB} = 0V
$I_{D(on)}$	Drain Current[2]	-5.0	-	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
I_{G1G2}	Gate to Gate Isolation Current	-	-	±1.0	µA	V_{G1G2} = ±80V, I_D = I_S = 0 = mA
g_{fs}	Forward Transconductance[4]	1500	-	4000	µS	V_{DS} = -15V, I_D = -5mA, *f* = 1kHz
g_{os}	Output Admittance	-	-	300		
$r_{ds(on)}$	Drain to Source "On" Resistance	-	-	300	Ω	V_{DS} = -20V, I_D = -100µA
C_{rss}[3]	Reverse Transfer Capacitance	-	-	1.0	pF	V_{DS} = -15V, I_D = -5mA, *f* = 1MHz
C_{iss}[3]	Input Capacitance Output Shorted	-	-	4.5		
C_{oss}[3]	Output Capacitance Input Shorted	-	-	3.0		

3N190/191 P-CHANNEL ENHANCEMENT MODE MOSFET

TO-78 7L Substrate (Case) Pin-4 Biasing Recommendation

In order to improve the overall product performance, we strongly recommend Substrate (Case) pin to be connected to highest VCC potential at Pin-4 with an optional 10KΩ resistor. This ensures strong reverse biasing of junction isolation diode and resulting improvement in Total Harmonic Distortion (THD) and Voltage Noise (Vn) performances. This applied voltage must be maximum 38V which is 2.0V less than device BVDSS breakdown voltage of 40V-max.

SWITCHING CHARACTERISTICS

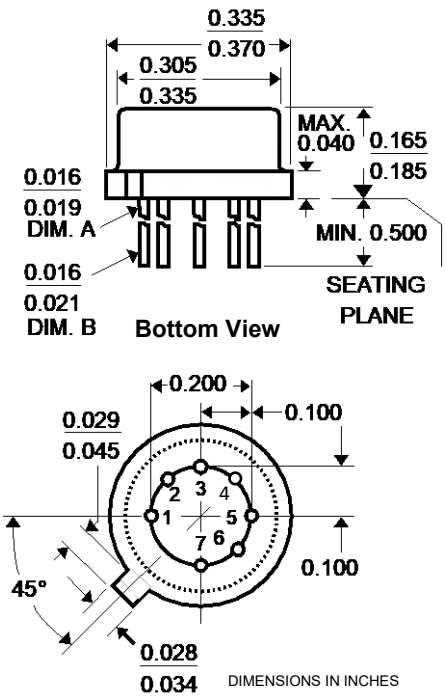
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$[3]	Turn On Delay Time	-	-	15	ns	V_{DD} = -15V, $I_{D(on)}$ = -5mA,
t_r[3]	Turn On Rise Time	-	-	30		R_G = R_L = 1.4kΩ
t_{off}[3]	Turn Off Time	-	-	50		

Notes

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Per Transistor.
3. For design reference only. Not 100% tested.
4. Measured at end points, T_A and T_B.
5. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

TO-78 7 Lead



Ordering Information

Standard Part Call-Out
3N190 TO-78 7L RoHS
3N191 TO-78 7L RoHS
Custom Part Call-Out (Custom Parts Include SEL + 4 Digit Numeric Code)
3N190 TO-78 7L RoHS SELXXXX
3N191 TO-78 7L RoHS SELXXXX

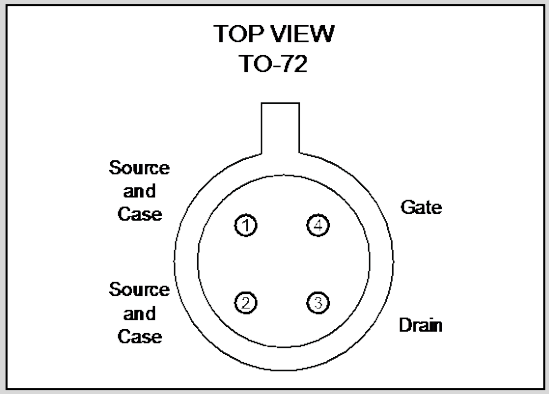
LINEAR SYSTEMS

Over 30 Years of Quality Through Innovation

LS320

HIGH INPUT IMPEDANCE BIFET AMPLIFIER

FEATURES	
HIGH INPUT IMPEDANCE	r_{Gs} = 100GΩ
HIGH TRANSCONDUCTANCE	Y_{FS} = 30,000µS
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Operating Junction Temperature	-55 to +125 °C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25 °C	200mW
Maximum Currents	
Drain Current	I_D = 25mA
Maximum Voltages	
Drain to Source[1]	V_{DSO} = 20V
Gate to Source	V_{GSS} = 20V



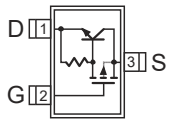
ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DS}	Drain to Source Voltage	-20			V	I_{DS} = 100µA, V_{GS} = 0V
V_{GS}	Gate to Source Voltage	-7	-10	-12	V	I_{DS} = 10mA, V_{DS} = -10V[2,3]
g_{fs}	Common Source Forward Transconductance	30,000			µS	I_{DS} = 10mA, V_{DS} = -10V, *f* = 1kHz
g_{oss}	Common Source Output Conductance		300		µS	I_{DS} = 10mA, V_{DS} = -10V, *f* = 1kHz
r_{Gs}	Gate to Source Input Resistance	100			GΩ	V_{GS} = 0 to 20V, T_J to 125 °C
C_{ISS}	Input Capacitance		8		pF	I_{DS} = 10mA, V_{DS} = -10V
C_{RSS}	Reverse Transfer Capacitance		1.5		pF	I_{DS} = 10mA, V_{DS} = -10V
e_n	Noise Voltage		25		µV	I_{DS} = 10mA, V_{DS} = 10V BW = 50 to 15kHz

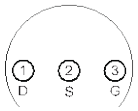
All limits are absolute numbers. Negative signs indicate electrical polarity.

PACKAGE OPTIONS

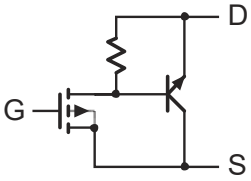
SOT-23
TOP VIEW



TO-92
TOP VIEW



FUNCTIONAL



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The gate to source voltage must never exceed 100V, t < 10ms.
3. Additional screening available

LINEAR SYSTEMS

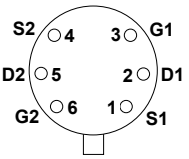
Improved Standard Products®

VCR11N

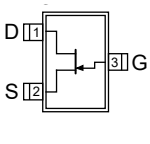
N-Channel JFET, Voltage Controlled Resistor

Simplify your Gain Control and Attenuation Designs Using Fewer Parts

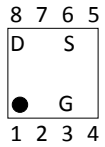
ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-65 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	300mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = -25V
Gate to Drain	V_{GDS} = -25V



TO-71 6L
Top View



SOT-23 6L
Top View



DFN 8L
Top View

Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation
- Pin-for-Pin Replacement for Siliconix VCR11N

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Amplifier Gain Control
- Oscillator Amplitude Control
- Small Signal Attenuations
- Filters

Description

A voltage-controlled resistor (VCR) is a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third. The VCR is capable of operation as a symmetrical resistor with no dc bias voltage in the signal loop, an ideal characteristic for many applications.

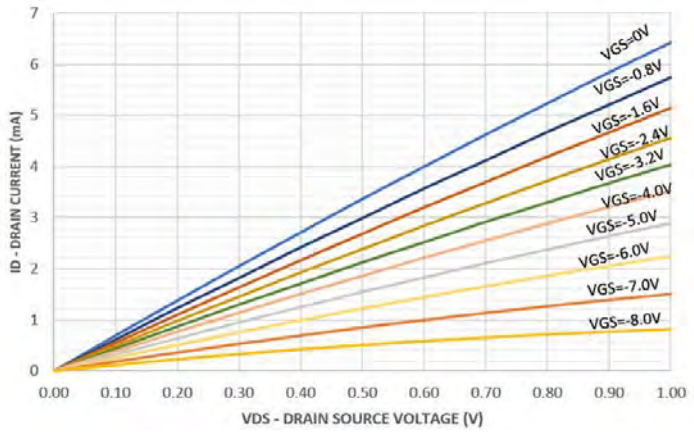
The VCR11N is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change with no change in V_{GS} voltage. The VCR11N is available in the TO-71 6 lead package.

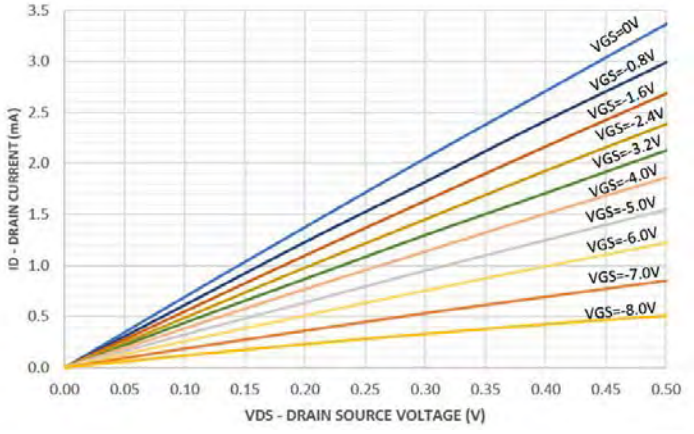
Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-8		-12	V	I_D = 1µA, V_{DS} 10V
I_{GSS}	Gate to Source Leakage Current			-0.2	nA	V_{GS} = -15V, V_{DS} = 0V
$r_{DS(on)}$	Dynamic Drain to Source "ON" Resistance	100		200	Ω	V_{GS} =0V, I_D=500µA
		100		200	Ω	V_{GS} =0V, I_D=1mA
r_{DS1}/r_{DS2}	Static Drain to Source "ON" Resistance Ratios	0.95		1		V_{GS} =0V, I_D=500µA
		0.95		1		V_{GS} =0V, I_D=1mA
C_{dgo}	Drain to Gate Capacitance			8	pF	V_{GD} =-10V, I_s=0A, *f*=1MHz
C_{dgo}	Source to Gate Capacitance			8	pF	V_{GS} =-10V, I_D=0A, *f*=1MHz

Typical Characteristics

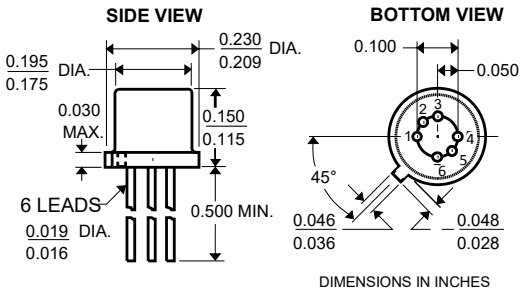
Output Characteristics
VCR11N



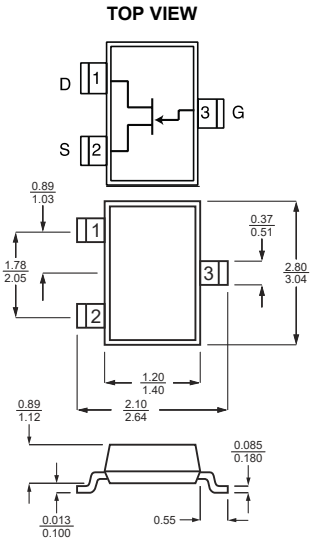


Standard Package Dimensions

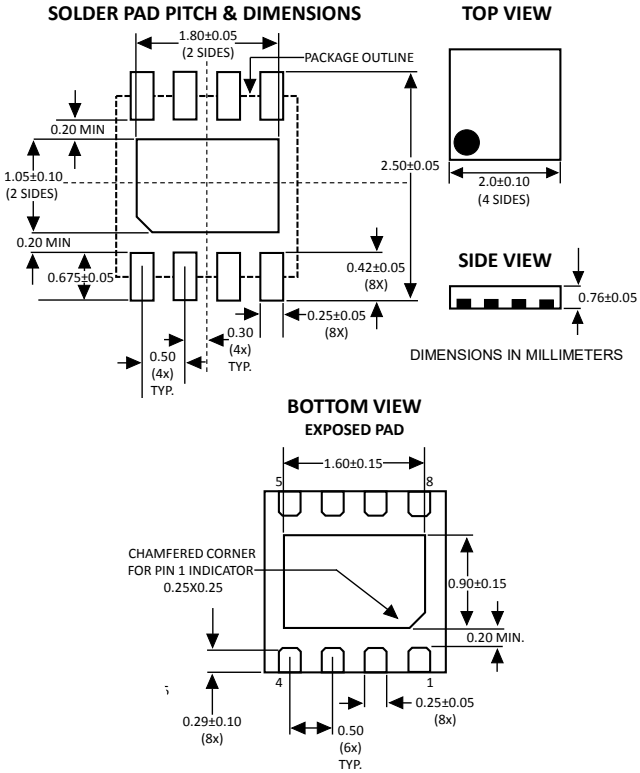
TO-71 6 Lead



SOT-23 6 Lead



DFN 8 Lead



Ordering Information

STANDARD PART CALL-OUT
VCR11N TO-71 6L RoHS
VCR11N SOT-23 6L RoHS
VCR11N DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
VCR11N TO-71 6L RoHS SELXXXX
VCR11N SOT-23 6L RoHS SELXXXX
VCR11N DFN 8L RoHS SELXXXX

Notes

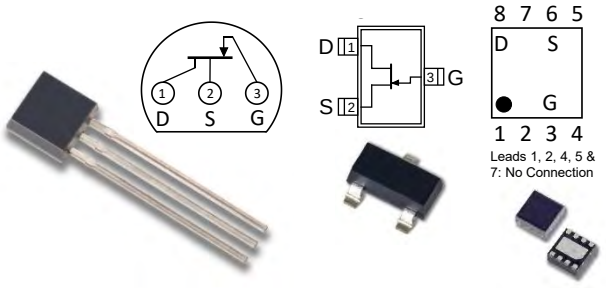
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300μs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.
4. When ordering include the full Linear Systems part number and package type. Linear Systems creates custom parts on a case by case basis. To learn whether Linear Systems can meet your requirements, please send your drawing along with a detailed description of the device specifications to sales@linearsystems.com. One of our qualified representatives will contact you.
5. All standard parts are RoHS compliant. Contact the factory for availability of non-RoHS parts.
6. Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

LS26VNS

N-Channel JFET, Voltage Controlled Resistor

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = -40V
Gate to Drain	V_{GDS} = -40V

TO-92 (3L) **SOT-23 (3L)** **DFN (8L)**



Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Variable Gain Amplifiers
- Automatic Gain Control
- Voltage Controlled Oscillator
- Small Signal Attenuations
- Filter Range Control

Description

The LS26VNS N-Channel Single JFET voltage controlled resistor has a drain-source resistance that is controlled by a DC bias voltage (V_{GS}) applied to a high impedance gate terminal. Minimum RDS of 14 Ω occurs when V_{GS} = -1.0V. As V_{GS} approaches the pinch-off voltage of -6.0V RDS rapidly increases to the maximum value or RDS = 38 Ω.

The LS26VNS is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change from14 to 38 Ω with no change in V_{GS} voltage. The LS26VNS is available in TO-92 (3 Lead), SOT-23 (3 Lead) and small foot-print DFN (8 Lead) packages.

Static Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-40			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.0		-6.0	V	V_{DS} = 10V, I_D = 1µA
I_{GSS}	Gate to Source Leakage Current			-1.0	nA	V_{GS} = -20V, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		V	I_G = 1mA, I_D = 0A
$R_{DS(on)1}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} =0.5V, I_D=2.5mA
$R_{DS(on)2}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} =0.5V, I_D=5.0mA
R_{DS1}/R_{DS2}	Static $R_{DS(on)}$ Ratio	0.90		1.0		

LS26VNS

Dynamic Electrical Characteristics @ 25°C (unless otherwise stated)

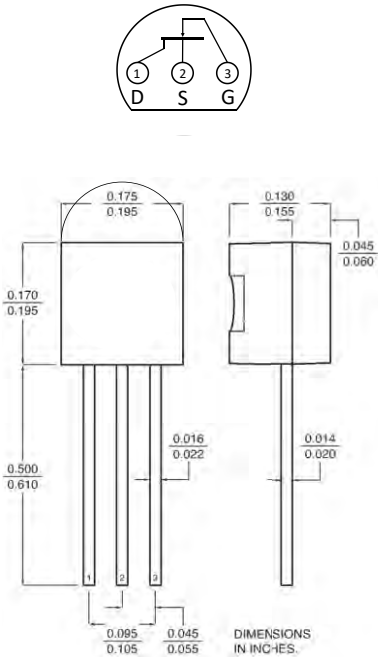
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$R_{DS(on)ac}$	Drain to Source "ON" Resistance	14		38	Ohms	V_{DS} = 0.50V, I_D = 300 µA, *f* = 1kHz
C_{ISS}	Common Source Input Capacitance		13		pF	V_{DS} = 20V, V_{GS} = 0V, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		3.6		pF	V_{DS} = 0V, V_{GS} = -12V , *f* = 1MHz

Notes

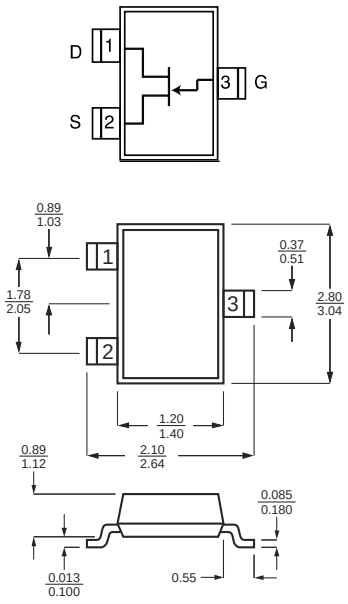
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

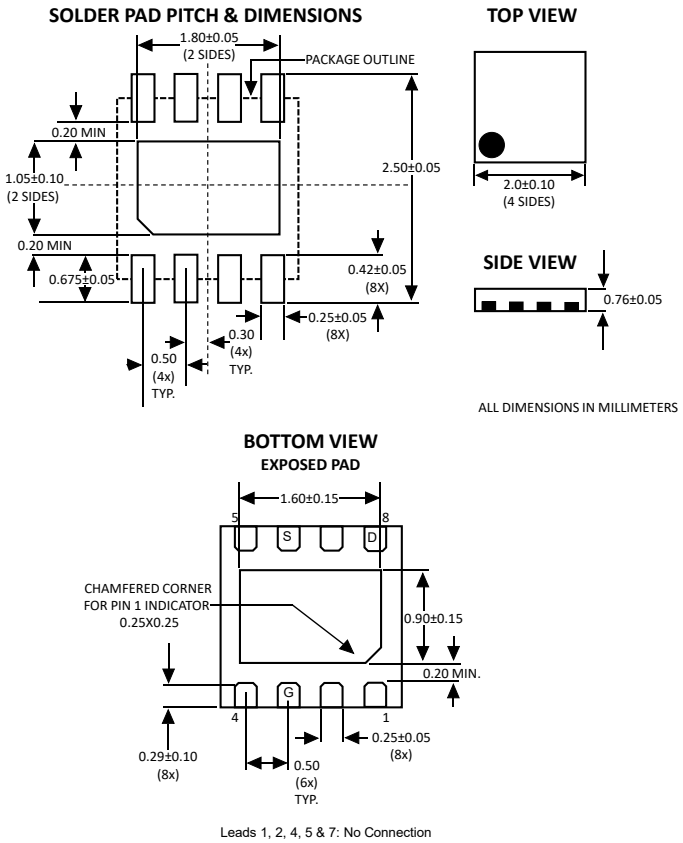
TO-92 3 Lead



SOT-23 3 Lead

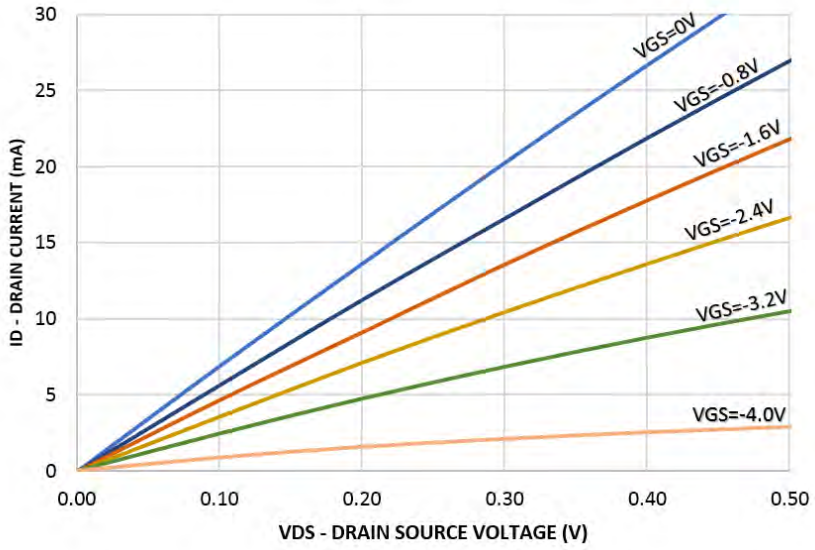


DFN 8 Lead



Typical Characteristics

Output Characteristics
LS26VNS



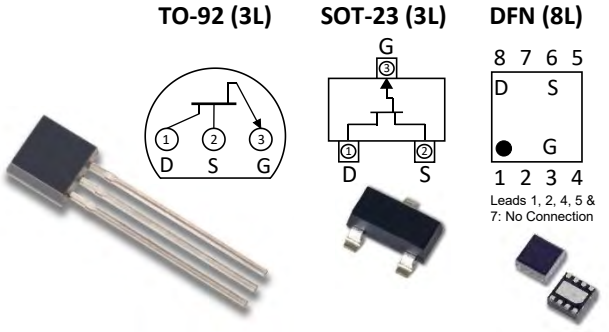
Ordering Information

STANDARD PART CALL-OUT
LS26VNS TO-92 3L RoHS
LS26VNS SOT-23 3L RoHS
LS26VNS DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LS26VNS TO-92 3L RoHS SELXXXX
LS26VNS SOT-23 3L RoHS SELXXXX
LS26VNS DFN 8L RoHS SELXXXX

LS26VPS

P-Channel JFET, Voltage Controlled Resistor

ABSOLUTE MAXIMUM RATINGS[1] @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ Ta= +25°C	350mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = +40V
Gate to Drain	V_{GDS} = +40V



Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance
- Gain Ranging Capability
- Simplified Drive Voltage Capabilities
- No Circuit Interaction
- Wide Range Signal Attenuation

Benefits

- Wide Range Signal Attenuation
- Gain Ranging
- Simplified Gate Drive
- High Breakdown Voltage
- No Circuit Interaction

Applications

- Variable Gain Amplifiers
- Automatic Gain Control
- Voltage Controlled Oscillator
- Small Signal Attenuations
- Filter Range Control

Description

The LS26VPS P-Channel Single JFET voltage-controlled resistor has a drain-source resistance that is controlled by a DC bias voltage (V_{GS}) applied to a high impedance gate terminal. Minimum RDS of 20 Ω occurs when V_{GS} = 3.0V. As V_{GS} approaches the pinch-off voltage of 7.5V, RDS rapidly increases to the maximum value or RDS = 50 Ω.

The LS26VPS is specially intended for applications where the drain-source voltage is a low-level AC signal with no DC component. The key device performance is the predictable RDS change from 20 to 50 Ω with no change in V_{GS} voltage. The LS26VPS is available in TO-92 (3 Lead), SOT-23 (3 Lead) and small foot-print DFN (8 Lead) packages.

Static Electrical Characteristics @ Tj= 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	+40			V	I_G = +1μA, V_{DS} = 0V
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	3.0		7.5	V	V_{DS} = -10V, I_D = -1μA
I_{GSS}	Gate to Source Leakage Current			1.0	nA	V_{GS} = +20V, V_{DS} = 0V
$V_{GS(F)}$	Gate to Source Forward Voltage		0.7		V	I_G = 1mA, I_D = 0A
$R_{DS(on)1}$	Drain to Source "ON" Resistance	20	35	50	Ohms	V_{DS} = -0.5V, I_D= -2.5mA
$R_{DS(on)2}$	Drain to Source "ON" Resistance	20		50	Ohms	V_{DS} = -0.5V, I_D= -5.0mA
R_{DS1}/R_{DS2}	Static $R_{DS(on)}$ Ratio	0.90		1.0		

LS26VPS

Dynamic Electrical Characteristics @ 25°C (unless otherwise stated)

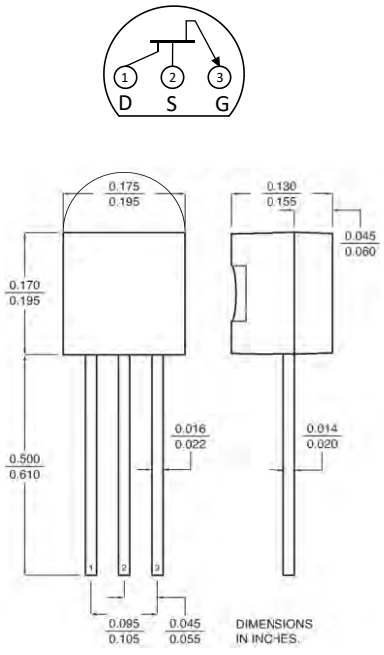
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$R_{DS(on)ac}$	Drain to Source "ON" Resistance	20		50	Ohms	V_{DS} = -0.50V, I_D = -300 µA, *f* = 1kHz
C_{ISS}	Common Source Input Capacitance		13		pF	V_{DS} = -20V, V_{GS} = 0V, *f* = 1MHz
C_{RSS}	Common Source Reverse Transfer Cap.		3.6		pF	V_{DS} = 0V, V_{DS} = +12V , *f* = 1MHz

Notes

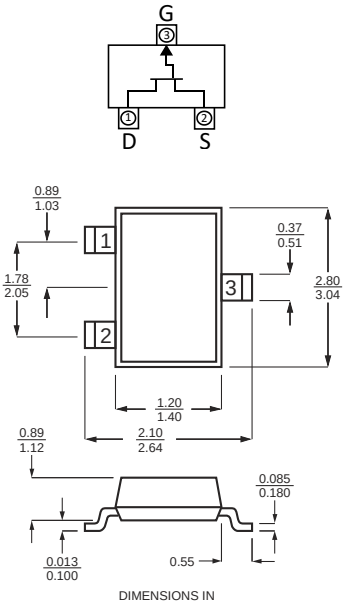
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: PW ≤ 300µs, Duty Cycle ≤ 3%
3. All characteristics MIN/TYP/MAX numbers are absolute values. Negative values indicate electrical polarity only.

Package Dimensions

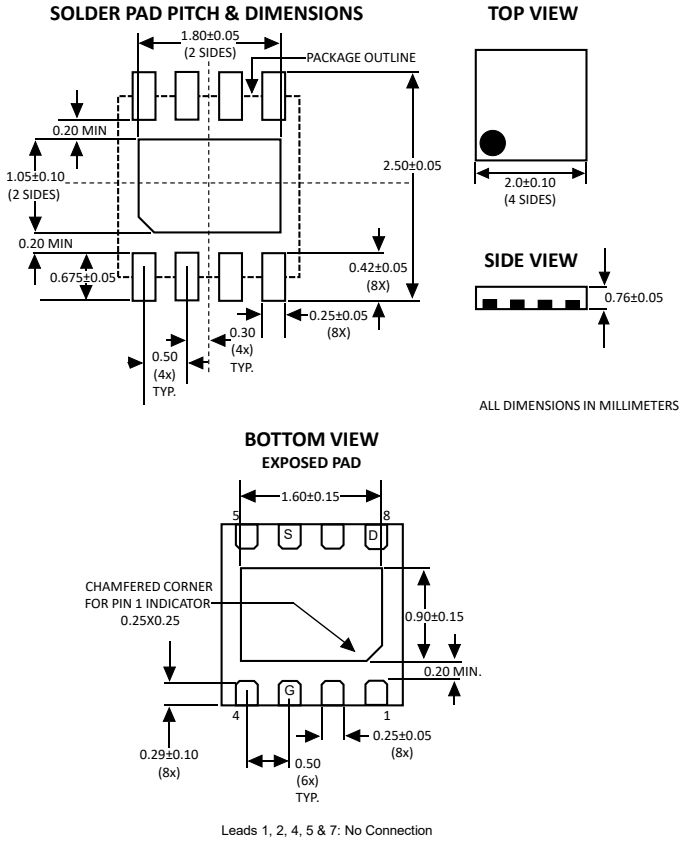
TO-92 3 Lead



SOT-23 3 Lead

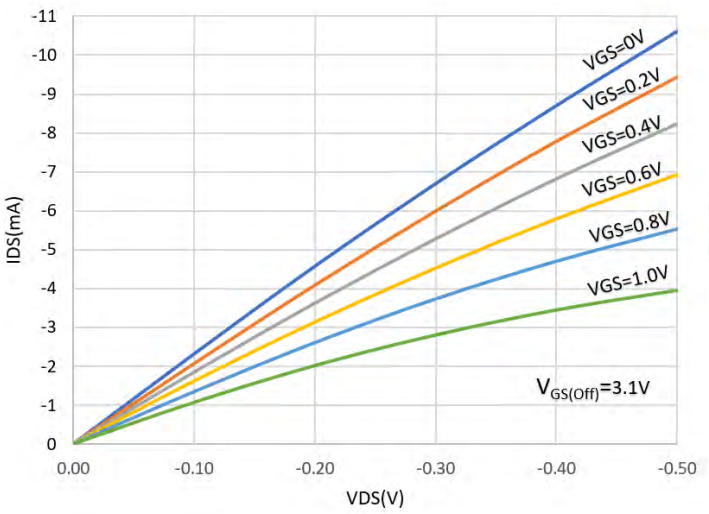


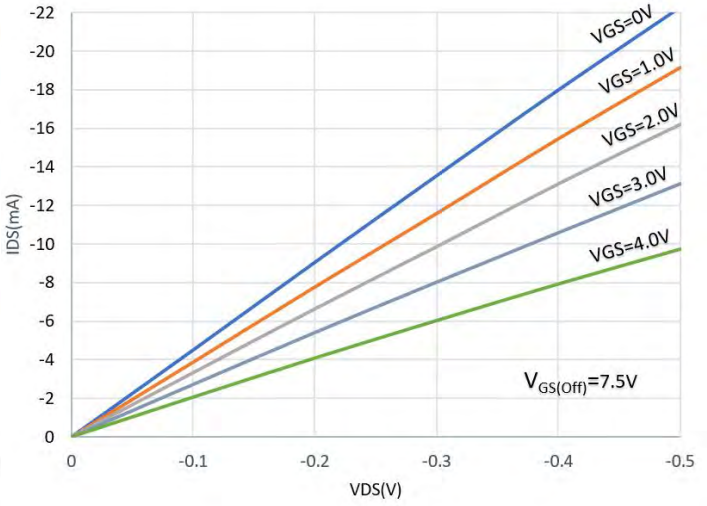
DFN 8 Lead



Typical Characteristics

Output Characteristics
LS26VPS

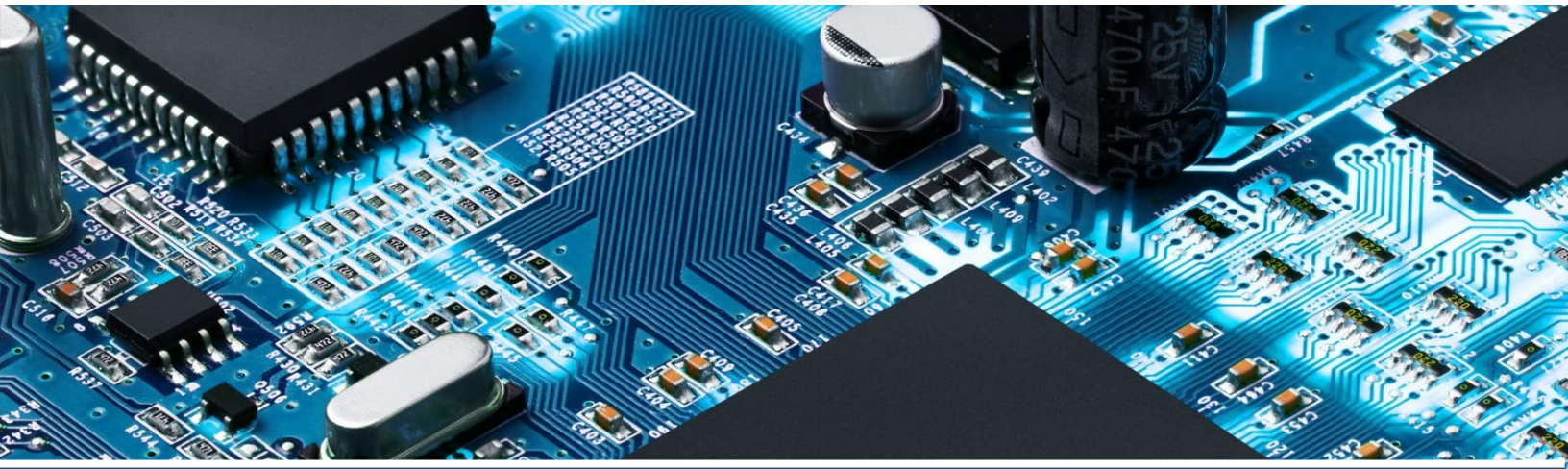




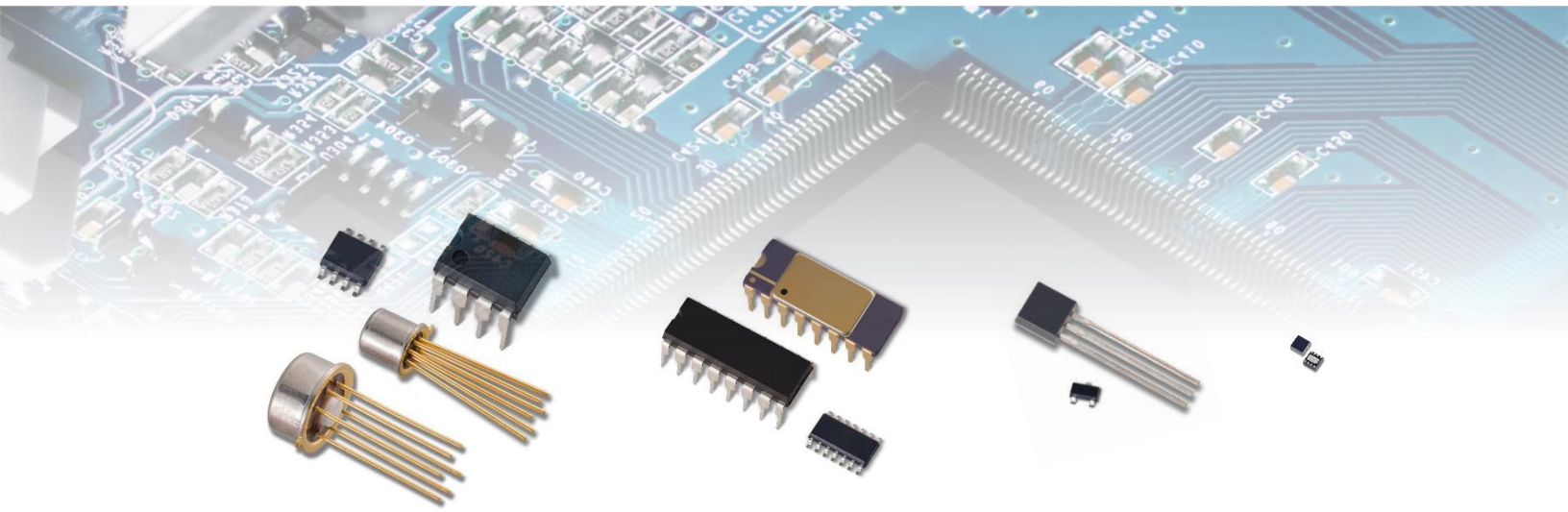
Ordering Information

STANDARD PART CALL-OUT
LS26VPS TO-92 3L RoHS
LS26VPS SOT-23 3L RoHS
LS26VPS DFN 8L RoHS
CUSTOM PART CALL-OUT
(CUSTOM PARTS INCLUDE SEL + 4 DIGIT NUMERIC CODE)
LS26VPS TO-92 3L RoHS SELXXXX
LS26VPS SOT-23 3L RoHS SELXXXX
LS26VPS DFN 8L RoHS SELXXXX

LINEAR SYSTEMS **Quality Through Innovation Since 1987**

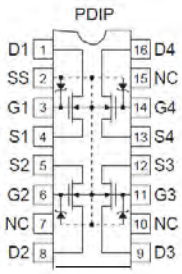


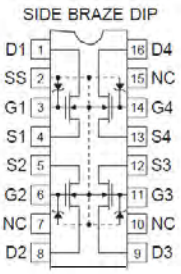
PACKAGE OPTIONS

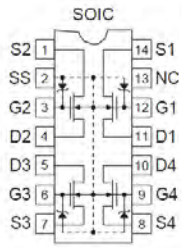


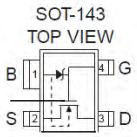
Package Options

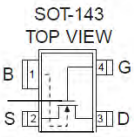
Lateral DMOS Switch Packages

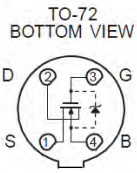


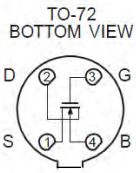


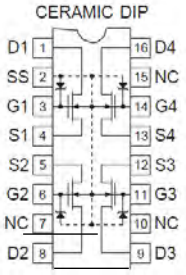


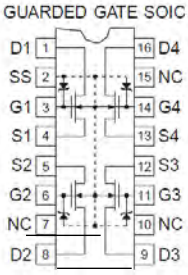




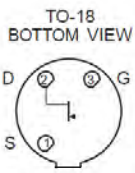


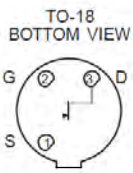


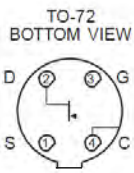


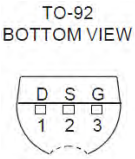


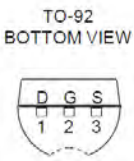
Single JFET Packages

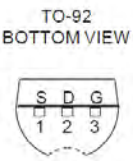


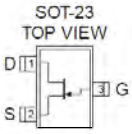


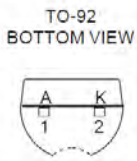


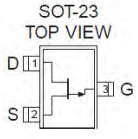




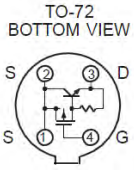


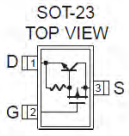


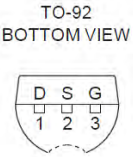




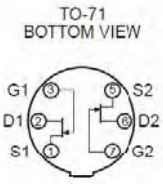
BIFET Amplifier Packages

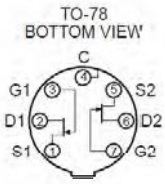


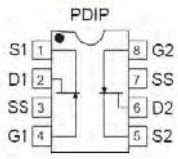


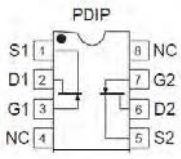


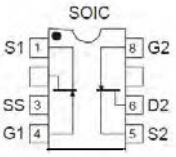
Dual JFET Packages

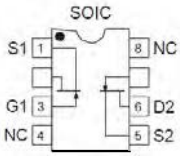


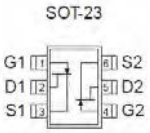


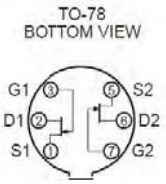




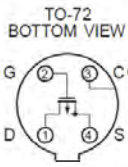


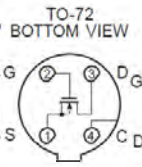


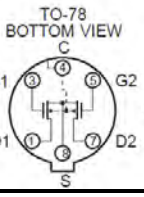


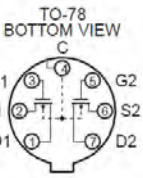


MOSFET Packages

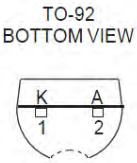


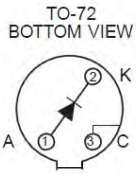


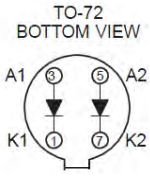


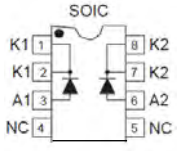


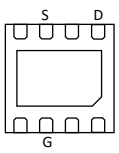
Diode Packages



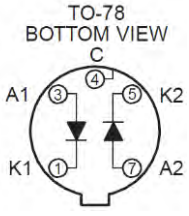


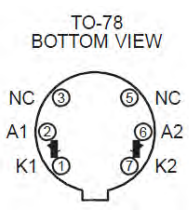






DFN 8L
BOTTOM VIEW
EXPOSED PAD





BJT Packages

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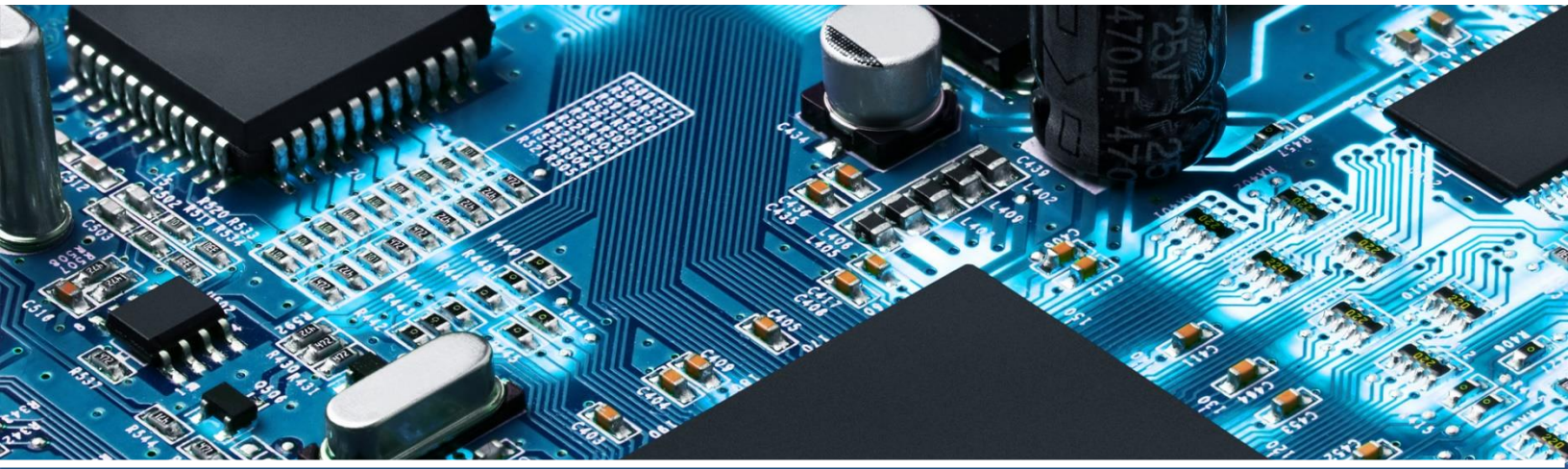
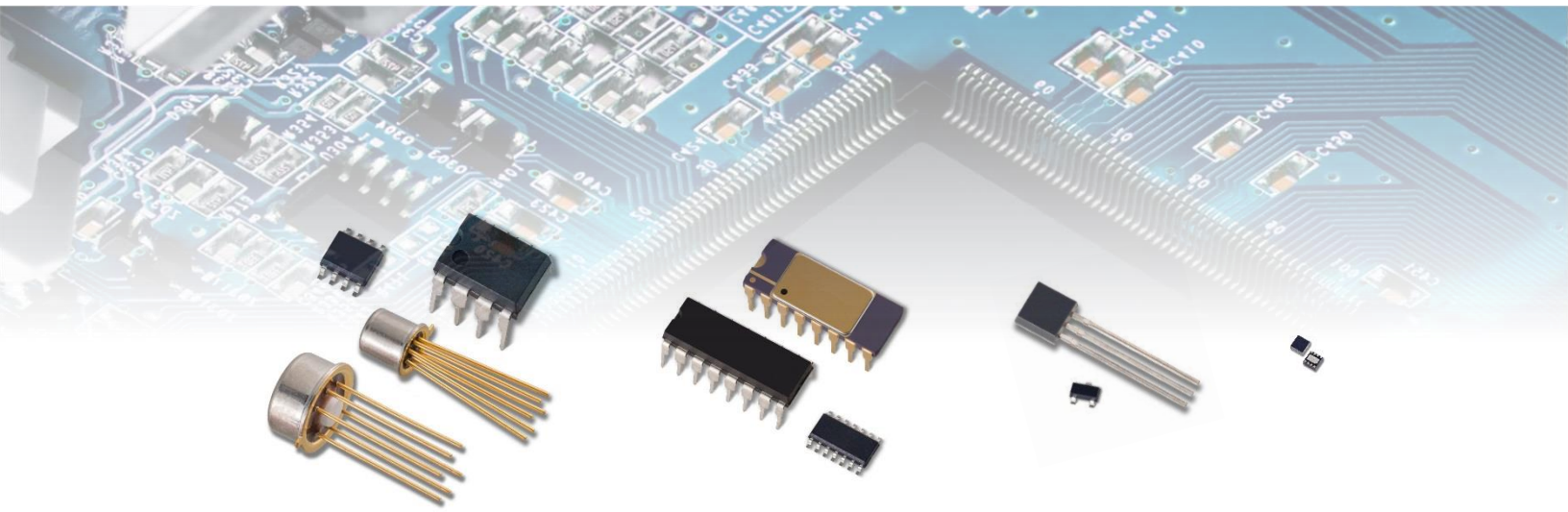


APPLICATION NOTES



LINEAR SYSTEMS

Quality Through Innovation Since 1987

LSK389

APPLICATION NOTE

DUAL MONOLITHIC JFET FOR ULTRA-LOW NOISE APPLICATIONS

By: Bob Cordell

Features

- Low Wideband Noise
- Low *1/f* Noise
- High Transconductance
- Well-Matched Threshold Voltages
- High *gm*/Capacitance Ratio
- Industry's First 100% Noise-Tested JFET

Applications

- Low Noise Amplifiers
- Differential Amplifiers
- High Input Impedance Amplifiers
- Phono and Other Audio Preamps
- Condenser Microphone Preamps
- Electrometers
- Piezoelectric Sensor Preamps
- Front-end for Low-Noise Op Amps

Introduction

The LSK389 is the industry's lowest noise Dual N-Channel JFET, 100% tested, guaranteed to meet 1/*f* and broadband noise specifications, while eliminating burst (RTN or popcorn) noise entirely. The product displays high transconductance and very good matching. It is the JFET of choice for low noise applications, especially those requiring a differential amplifier input stage.

LSK389 Key Specifications

- 1.3 nV/√Hz input noise at 1 kHz, I_D = 2 mA
- 1.5 nV/√Hz at 10 Hz, I_D = 2 mA
- 14 mS transconductance at I_D = 2 mA
- Improved DC offset ±15 mV max.
- C_{ISS} = 25 pF typ.
- C_{RSS} = 5.5 pF typ.
- Breakdown voltage = 40 V min.
- 4 grades of I_{DSS} available (A, B, C, D)

N-Channel JFET Basics

The simplified equation below describes the DC operation of a JFET [1]. The term V_t is the threshold voltage. The term β is the transconductance coefficient of the JFET (not to be confused with BJT current gain). The terms V_t and β are key SPICE parameters that define basic JFET DC operation. The simple relationship below is valid for $V_{ds} > V_t$ and does not take into account the influence of V_{ds} that is responsible for output resistance of the device. The equation is valid only for positive values of $V_{gs} - V_t$.

$$I_d = \beta(V_{gs} - V_t)^2$$

At V_{gs} = 0, we have I_{DSS}, which is the maximum current that will flow when the device is in its saturation region, where V_{ds} is much larger than V_t:

$$I_{DSS} = \beta(V_t)^2$$

β can be seen from I_{DSS} and V_t to be:

$\beta = I_{DSS} / (V_t)^2$

The operating transconductance *gm* is easily seen to be:

$gm = 2 * \sqrt{\beta * I_d}$

This last relationship is important, because transconductance of the JFET is what is most often of importance to circuit operation [2]. For a given transconductance parameter β, *gm* is largely independent of I_{DSS} and V_t, and goes up as the square root of drain current. This is in contrast to a bipolar transistor where *gm* is proportional to collector current. The value of β for JFETs ranges from about 1e-3 to 100e-3.

These simplified equations do not take into account the effect that the parameter lambda has on output conductance G_{os} of the JFET. In other words, in the saturation region, the drain current does increase slightly as V_{ds} increases. G_{os} for the LSK389 is about 40 µS when I_d = 2 mA and V_{ds} = 10 V. This corresponds to about 25 kΩ. The equations also do not account for ohmic source resistance, which can reduce transconductance a bit, since it acts like source degeneration.

A typical LSK389 low noise JFET showed a measured I_{DSS} of 13.8 mA and transconductance of 14.6 mS at an operating current of 2 mA. Gate voltage at that operating point was –0.50 V. With a 1-kΩ load, the un-degenerated common-source LSK389 provides gain of 14.6. With a 10-kΩ load, the gain is 108, which is quite high for a single common source JFET amplifier stage. This amount of gain in an LSK389 first-stage can help make the most of the inherently low input-referred noise of the LSK389 in a multi-stage preamplifier. This stage has a 3-dB bandwidth of 700 kHz when driving a 10-pF load, for a gain-bandwidth product of 76 MHz.

JFET Noise

JFET noise results primarily from *thermal channel noise* [1, 3 - 6]. That noise is modeled as an equivalent input resistor r_n whose resistance is equal to approximately 0.6/*gm* [7]. If we model the effect of *gm* as *rs'* (analogous to *re'* for a BJT), we have r_n = 0.6*rs'*. This is remarkably similar to the equivalent voltage noise source for a BJT, which is the voltage noise of a resistor whose value is 0.5*re'*. The voltage noise of a BJT goes down as the square root of I_c because *gm* is proportional to I_c, and *re'* goes down linearly with I_c as well. However, the *gm* of a JFET increases only as the square root of I_d. As a result, JFET input voltage noise goes down as the one-fourth power of I_d. The factor 0.6/*gm* in modeling the equivalent input noise resistance is approximate, and SPICE modeling of some JFETs suggests that the number is closer to 0.67. That is the number that will be used here.

At I_d = 2.0 mA, *gm* for the measured LSK389 dual monolithic JFET described above is 14.6 mS, corresponding to a resistance *rs'* of 68.5 Ω. Multiplying by the factor 0.67, we have an equivalent noise resistance r_n of 45.9 Ω. Recognizing that a 1 kΩ resistor has thermal noise voltage of 4.2 nV/√Hz, and that thermal noise goes as the square root of resistance ratio, the 45.9 Ω resistance represents theoretical input-referred noise for the LSK389 of 0.9 nV/√Hz. JFET input voltage noise will also include a thermal noise contribution from ohmic gate and source resistances, but this is fairly small.

The noise measurement circuit shown in Figure 1 was implemented to measure the noise of the LSK389 at 2.0 mA. It comprises two stages of amplification implemented with the two JFETs in the LSK389. Total gain of the amplifier is 880. With the input of the amplifier shorted, the output was connected to an A-weighted noise measurement meter with an equivalent noise bandwidth (ENBW) of 13.5 kHz. The use of A weighting minimizes contributions from hum and provides a well-defined ENBW. Measured noise at the output of the amplifier was 120 µV. Dividing by the gain of 880, we have 136 nV. Dividing by the number of root Hz in an ENBW of 13.5 kHz (116/√Hz), we have 1.17 nV/√Hz. This was achieved with a completely un-shielded circuit using no extraordinary measures. Given other circuit and environmental noise contributors, it is likely that the LSK389 was performing at about 1 nV/√Hz.

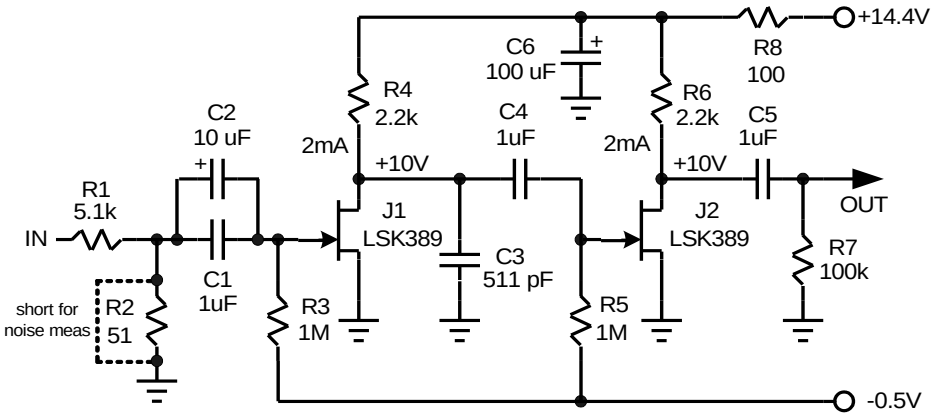


Figure 1: JFET noise measurement circuit

The theoretical thermal channel noise for a JFET operating at *gm* = 14.6 mS is 0.9 nV/√Hz, as can be calculated in the discussion below. However, a JFET also has ohmic resistances in the source, drain and gate, which can contribute thermal noise. By partial example, the source-drain resistance of the LSK389 measured above is 36 Ω when there is no bias. Under operating conditions, and depending on device geometry and doping profiles, a portion of this resistance remains as effective ohmic source resistance that can add thermal noise. Ohmic source resistance of only 10 Ω would contribute 0.4 nV/√Hz.

JFET input voltage noise is a function of drain current because it is a function of transconductance. It decreases as drain current increases, in accordance with the discussion below. Table 1 shows the gain and input noise of the noise measurement preamplifier as a function of the drain current of each JFET in the LSK389. The applied gate voltage for each condition is also listed for reference.

Table 1

I_d, mA	V_{gs}, V	Gain	Gain/stage	noise, nV/√Hz
0.5	0.62	200	14	1.72
1.0	0.57	450	21	1.44
2.0	0.50	880	30	1.17
4.0	0.39	1400	37	1.11
8.0	0.22	1980	45	1.07

It can be seen that the noise goes down at increased drain current, but not quite as fast as thermal channel noise theory below would predict. This is likely due to the contribution of thermal noise from ohmic gate and source resistances. The presence of source resistance can also be seen by the fact that when I_d is doubled, gain does not go up fully by √2. It is also notable that the LSK389 was running a little bit hot when drain current for each device was 8 mA and V_{ds} was 10 V, for total dissipation of 160 mW. Higher operating temperature increases noise and decreases transconductance. Operating the device at V_{ds} = 5 V will halve dissipation and reduce noise somewhat.

Although noise decreases with increased bias current, Table 1 shows that there is a point of diminishing returns. For example, two LSK389 devices in parallel, each operating at 4 mA, will deliver a 3-dB noise reduction compared to one device, reducing noise to about 0.8 nV/√Hz, superior to a single device operating at 8 mA, which will have noise on the order of 1.07 nV/√Hz.

JFET Noise Sources

In order to understand low-noise JFETs, it is helpful to briefly review the 5 major sources of noise in JFETs [1, 3, 4, 7].

1. Thermal channel noise
2. Gate current shot noise
3. *1/f* noise
4. Generation-recombination noise
5. Impact ionization noise

The first two sources of noise are largely fundamental to the device, while the remaining three sources are largely the result of device imperfections. Examples of such imperfections include lattice damage and charge traps.

Thermal Channel Noise

Thermal channel noise, as discussed above, is akin to the Johnson noise of the resistance of the channel [2]. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the

point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, and can vary with the individual device geometry [3]. It is often a bit smaller than 0.67.

Gate Shot Noise Current

JFET input current noise results from the shot noise associated with the gate junction leakage current. Shot noise increases as the square root of DC current passing through a semiconductor junction. A useful relationship is that I_{shot} = 0.57 pA/√Hz/√μA [7]. Alternately, I_{shot} = 0.57 fA/√Hz/√pA. Gate shot noise is white, and usually has no *1/f* component [8].

I_{shot} = 0.57 fA/√Hz/√pA

This noise is normally very small, on the order of fA/√Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Consider a circuit with a 100-MΩ resistive source impedance and a JFET with input noise current of 4 fA/√Hz at 25°C. Thermal noise of the 100-MΩ resistor will be 1330 nV/√Hz. The voltage noise resulting from the shot noise flowing in the source resistance will be 400 nV/√Hz. Leakage current doubles every 10°C, so at 65°C the leakage current goes up by a factor of 16 and the noise contributor will go up by a factor of 4 to about 1600 nV/√Hz. The two contributors are now comparable. Always bear in mind that the junction temperature will be higher than the ambient temperature, depending on device dissipation. For even higher source resistances in the GΩ range, the shot noise contributor could be comparable to, or greater than, the thermal noise contributor, even at room temperature.

Finally, consider a purely capacitive source of 50 pF, as from a condenser microphone, where there is theoretically no thermal noise contributor from the signal source (ignore biasing arrangements for the moment). At 32 Hz, the source impedance is 100 MΩ reactive and the shot noise contribution is still 400 nV/√Hz, far exceeding the voltage noise contribution of the JFET.

1/f Noise

At very low frequencies the input noise power of a JFET amplifier rises as the inverse of frequency. That is why this noise is referred to as *1/f* noise. When expressed as noise voltage, this means that the noise rises at a rate of 3 dB/octave as frequency decreases. In a good JFET, the *1/f* spot noise voltage at 10 Hz may be twice the spot noise at 1 kHz (up 6 dB) when expressed as nV/√Hz. The noise might typically be up by 3 dB at 40 Hz. *1/f* noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice [4]. Improved processing contributes to reduced *1/f* noise. In fact, the amount of *1/f* noise is sometimes considered as an indication of process quality.

By comparison, a good JFET IC op amp with input noise of 10 nV/√Hz at 1 kHz may have its noise up by 3 dB at 100 Hz and the spot noise at 10 Hz might be up by 10 dB to 32 nV/√Hz. At 1Hz that op amp may have spot noise on the order of 65 nV/√Hz.

Figure 2 is a plot of voltage noise versus frequency for a hypothetical JFET (not an LSK389). The *1/f* corner frequency is defined as the frequency where the *1/f* noise contribution equals the flat band noise. Put another way, it is where the –3 dB/octave *1/f* noise line intersects the flat band noise line. At this frequency, the voltage noise will be up by 3 dB.

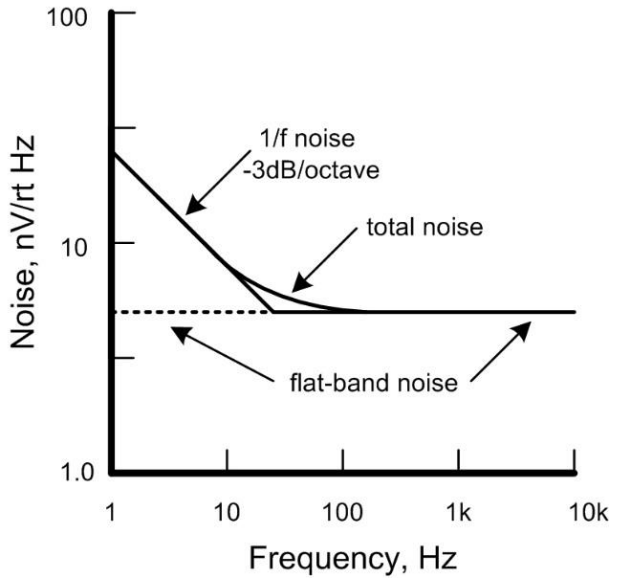


Figure 2: *1/f* noise voltage of a hypothetical JFET

Generation-recombination Noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as *G-R* noise [4]. This *excess noise* is discussed in the LSK489 application note [7]. Thanks to Linear Systems' advanced processing this source of noise is very low in the LSK389.

Impact Ionization Noise

An electron traveling in a strong electric field can be accelerated to the point where it has enough kinetic energy to knock another electron out of its valence band into the conduction band if it impacts an atom in the crystal lattice [4, 6, 8]. For convenience, the electron corresponding to normal current flow can be called a "seed" electron, since it starts the process. This collision creates a new hole-electron pair. This process is called impact ionization. The new hole and electron then act as additional charge carriers and add to the current flow. The new carriers may also be accelerated to the point where they themselves create an impact ionization event, so the process may be multiplied. This is what is called an avalanche effect. Impact ionization often occurs in a p-n junction that is under a high reverse bias voltage that creates a large electric field. Impact ionization noise is discussed in more detail in the LSK489 application note [7].

Single-ended Amplifier with JFETs in Parallel

Figure 3(a) shows a simple single-ended JFET amplifier stage. In a practical implementation, the –0.29-V bias voltage must be controlled by some form of feedback to maintain the desired operating point of 2.0 mA. It is well known that operating two JFETs in parallel will reduce input-referred noise by 3 dB. This, of course, requires that the JFETs be matched, as in the case of both JFETs in an LSK389 dual monolithic matched pair. This is straightforward in a single-ended amplifier application, as in (b). In (c), a parallel-connected JFET pair is combined with an op amp and negative feedback to implement an amplifier with a gain of 1000.

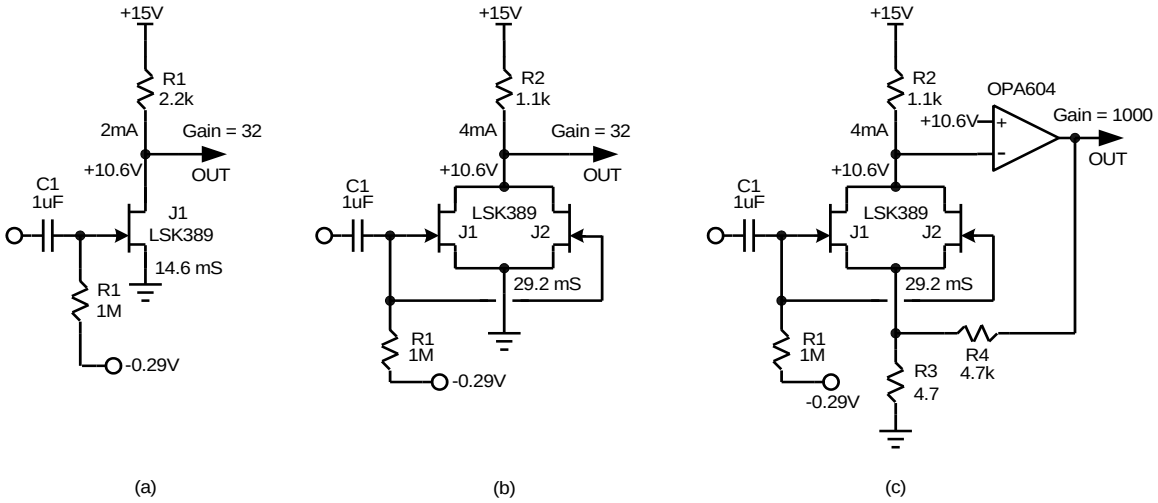


Figure 3: Single-ended JFET amplifier stages

Conversely, when an LSK389 is used as a differential pair, both JFETs are effectively in series as far as the signal is concerned (halving net transconductance), and input-referred noise increases by 3 dB over that of a single JFET in a single-ended arrangement, a significant noise disadvantage of the differential pair.

Given the use of an LSK389 in both cases, the single-ended amplifier using both devices in parallel is thus a full 6 dB quieter than the differential amplifier. This is a steep price to pay for differential operation. In both cases, the total current consumption is the same.

Simple Differential Pair Amplifier

Figure 4(a) shows a simple differential amplifier stage implemented with an LSK389. This non-feedback circuit provides a very high impedance differential input and a differential output. Its gain will, however, vary somewhat depending on the transconductance of the individual JFET.

Fortunately, transconductance of a given JFET type is much less variable than parameters like I_{DSS} and threshold voltage. Recall that

$$gm = 2 * \sqrt{\beta * I_d}$$

where the parameter β is similar for JFETs from the same process. Stabilizing the gain by the introduction of source degeneration resistors will seriously compromise the noise performance as a result of the thermal noise contributions from the source resistors.

If each JFET is operating at 2 mA, *gm* will be about 14 mS for each device. Differential gain will then be 2 * 14 mS * 2.2 k Ω = 61.6. Actual gain will be a bit lower due to the output conductance G_{os} of the JFETs. Input noise of the stage will be about 3 dB higher than that of each JFET, which will come to about 1.5 nV/√Hz. Noise contributions from the current source will be largely canceled by the differential nature of the circuit, but use of a low-noise current source is nevertheless recommended. Similarly, use of a current source with very high output impedance, such as one that is cascoded, is recommended in order to preserve good common mode rejection.

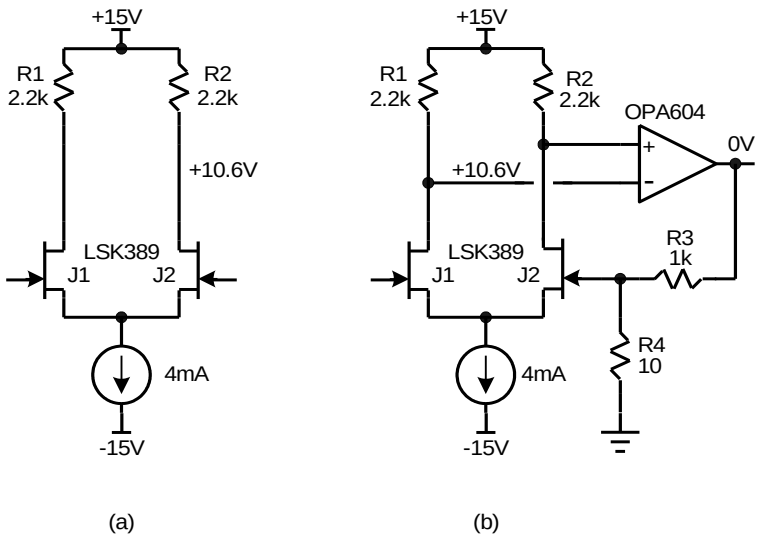


Figure 4: Simple LSK389 differential amplifiers

In Figure 4(b) the LSK389 is used as the input stage for a closed-loop feedback amplifier with a gain of 100. Most of the open loop gain for the amplifier is provided by the operational amplifier, which can be one of many different types, such as the OPA604. The main advantage of this arrangement is that the JFET input stage provides a low-noise front-end with extremely high input impedance. It provides enough initial gain to minimize noise contributions from the thermal noise of the load resistors and the input voltage noise of the following op amp stage.

The combination of the gain provided by the input stage and the op amp increases the loop gain and the unity gain frequency of the feedback amplifier. This means that caution must be exercised in choosing the closed loop gain to be large enough to keep the unity loop gain frequency from becoming so large as to introduce instability.

Cascoding and Driven Cascodes

Figure 5 (a), (b) and (c) show a differential pair that is cascoded 3 different ways. In (a), a conventional BJT cascode stage increases output impedance and eliminates Miller effect due to gate-drain capacitance in the JFETs. The cascode also allows the LSK389 to be used in circuits with higher voltages.

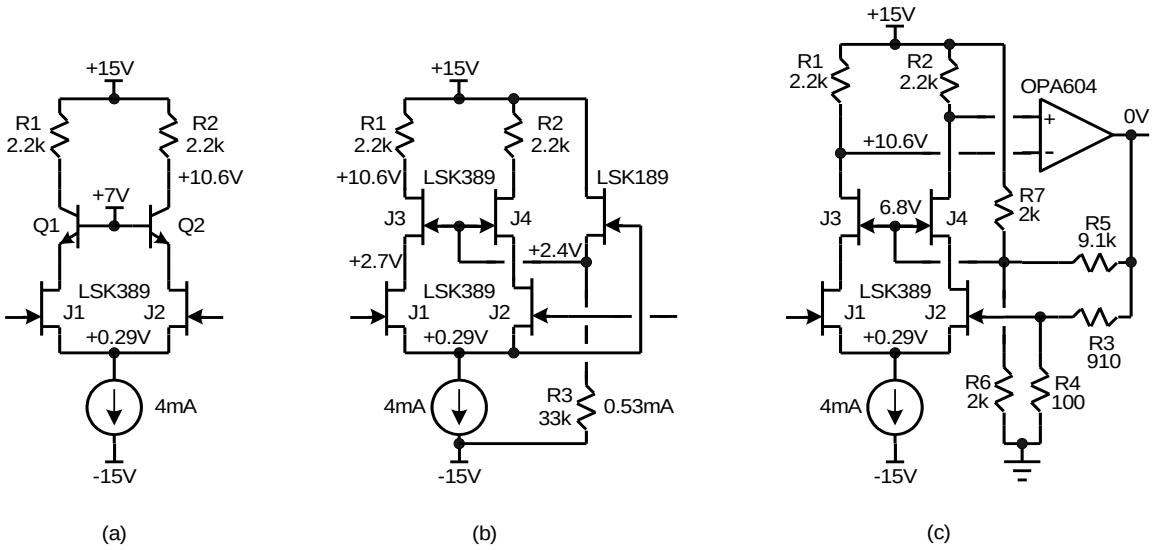


Figure 5: Cascoded differential amplifiers

Figure 5 (b) illustrates a bootstrapped cascode wherein the common mode signal present at the sources is fed to the gates of the JFET cascode transistors. This causes the drains of the JFETs to move with signal in the same way as the sources. This arrangement greatly reduces common mode distortion and also strongly suppresses the effect of drain-gate capacitance on the effective input capacitance of the stage. This can be important in some applications because of the moderate amount of drain-gate capacitance of the LSK389. An LSK189 JFET connected as a source follower is used in Figure 5 (b) to achieve the needed level shift of the voltage at the sources of J1 and J2. If greater V_{ds} for the differential pair is needed for more optimum operation, a Zener-based level shift arrangement, possibly using a P-channel LSK289, can be used. Bootstrapping is a form of positive feedback, so caution is advised at high frequencies. Such arrangements should always be simulated so that HF anomalies can be discovered and mitigated.

A third approach can be used in feedback amplifiers, as shown in Figure 5 (c). Here a replica of the feedback signal is used to drive the gates of the cascode transistors. I refer to this as a driven cascode [2]. The same cautions regarding bootstrapping mentioned above apply here as well.

Ultra-Low Noise Differential Amplifier Using Paralleled LSK389 JFETs

The ultra-low noise input amplifier is shown in Figure 6. It is a JFET-input, double folded cascode design without negative feedback [9]. Its gain is approximately 40 dB. Without negative feedback, there is no need for a feedback network with very low impedance (on the order of ohms) to keep the noise down. Such a feedback network can be difficult to drive. Moreover, without negative feedback, the input is naturally fully differential. The input JFET pair actually consists of four paralleled LSK389 JFET differential pairs, each pair with its own tail current source. This enables input-referred noise of 0.7 nV/√Hz to be achieved in a differential amplifier.

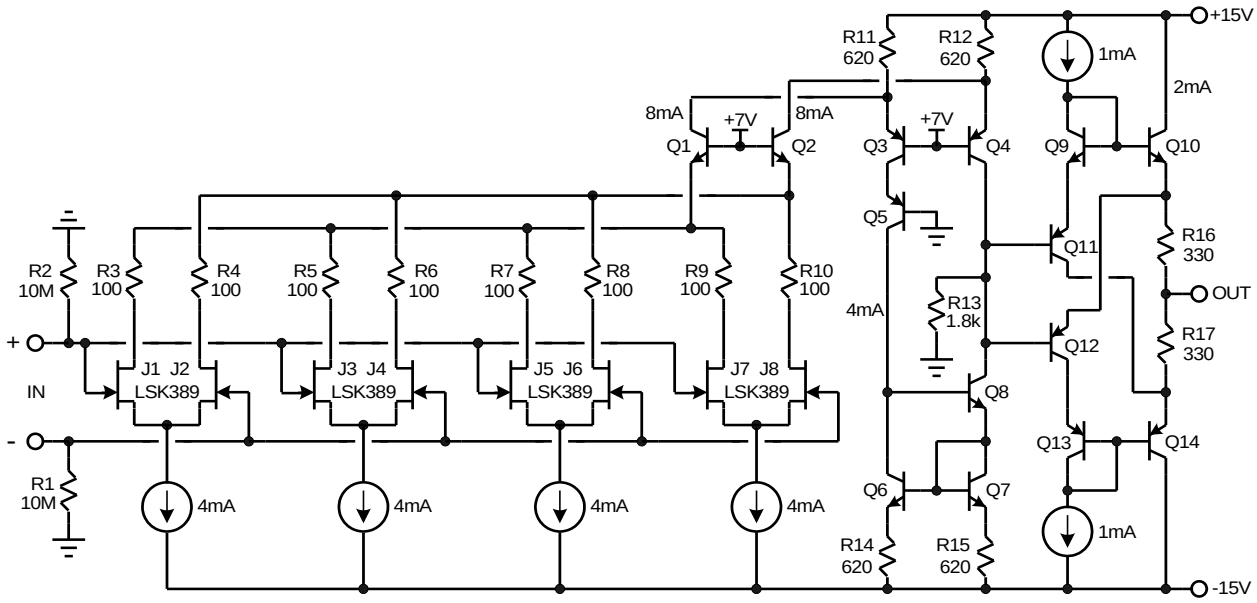


Figure 6: Ultra-Low noise differential amplifier

Paralleling of transistors is a well-known technique for reducing input voltage noise. Each time the number of transistors is doubled, a 3-dB improvement of S/N results. In the case here, 4 differential pairs are paralleled for a net improvement of 6 dB over a single differential pair. Simple paralleling of JFETs can lead to high-frequency instability and sub-optimal biasing due to differences in threshold voltage and I_{DSS} from pair to pair. If gate stopper resistors are used to mitigate the instability, noise is compromised. The key to paralleling JFET differential pairs is to literally parallel four pairs, each with its own tail current source. This decouples the sources among the pairs and allows each to find its own operating point. The decoupling of the sources also mitigates interaction among the pairs that can lead to instability. This, together with measures taken in the drain circuits, eliminates the need for gate stopper resistors.

This technique makes use of the fact that JFETs from the same process tend to have roughly the same transconductance if operated at the same current, even if the I_{DSS} and threshold voltages are not tightly matched. This means that each of the 4 pairs will contribute about the same amount of transconductance without close matching of the pairs.

The drains of the differential pairs are parallel-connected to the emitters of an NPN differential cascode stage. The low input impedance of the cascode helps reduce interactions among the parallel-connected drains that can lead to HF instability. Drain interactions are reduced by 100-Ω drain stopper resistors, which have no effect on noise.

A fifth degenerated differential pair using an LSK489 (not shown) can be used to inject a DC servo offset correction current at the emitters of Q1 and Q2 [9]. This approach provides a convenient and non-invasive way of injecting the correction current and adds negligible noise. Introducing the correction differentially ahead of the folded cascode results in less second harmonic distortion from JFET offset currents.

Gain is set to about 100 by the transconductance of the input pairs and shunt load resistor R13. Since the circuit operates without negative feedback, in some applications the gain may need to be trimmed. There may also be a modest temperature dependence of gain. The temperature dependence can be reduced if tail current sources with a positive temperature coefficient are employed. Doing so will tend to cancel the negative temperature coefficient of transconductance. Bandwidth of the amplifier is about 10 MHz. At an input level of 5 mV RMS, THD is only 0.005%, with no significant harmonics above the third. This level is about 20 dB higher than the nominal level of 500 µV produced by a moving coil cartridge.

Source Follower with JFET Current Source

A handy source follower buffer is shown in Figure 7. It consists of a source follower whose pull-down current of about 1.3 mA is generated by a JFET current source, where R3 sets the current. Notice that R3 has V_{gs} of J2 across it at J2's operating current. If J1 and J2 are matched and have the same V_{gs} at the same operating current, voltage-dropping resistor R2 will drop the V_{gs} of J1 if it is the same value as R3, and the overall buffer will have close to zero input-output DC offset. This is a perfect application for the LSK389.

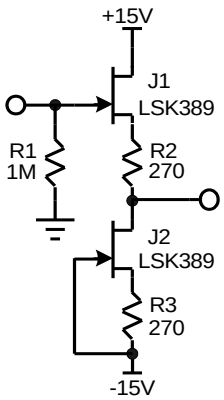


Figure 7: A source follower buffer with small DC offset

Substrate Bias Considerations

Figure 8 shows the connection arrangement inside the LSK389 dual monolithic JFET pair. Note that both transistors in the pair share a common substrate, and that substrate diodes exist between the gates and the substrate. The anodes of these substrate diodes are connected to the gates and the cathodes are connected to the substrate. These diodes are reverse biased under normal operating conditions. The substrate is brought out to pins 3 and 7 in the 8-pin SOIC package. The substrate is connected to the can in the metal TO-71 6L package.

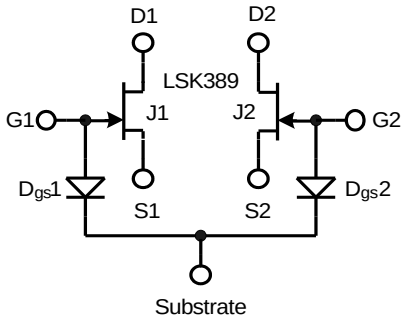


Figure 8: LSK389 including substrate diodes

The substrate diodes from the gates to the common substrate must sometimes be considered, but in most cases, the substrate is left floating. These diodes have a breakdown voltage in excess of 40 V. The leakage current of the substrate diodes, although quite small, can affect the net gate leakage current.

I_{DSS} Grades

The LSK389 is available in four I_{DSS} grades, A to D, with the following I_{DSS} ranges:

- LSK389A: 2.6 – 6.5 mA
- LSK389B: 6 – 12 mA
- LSK389C: 10 – 20 mA
- LSK389D: 17 – 30 mA

Conclusion

The LSK389 enables ultra-low noise amplifiers with very high input impedance and virtually no input bias current. Moreover, fully differential inputs with very high impedance can be implemented, which can be very important for low noise applications.

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LINEAR SYSTEMS

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Common Mode Rejection Ratio in **Dual Junction Field Effect Transistors**

By Kirkwood Rough and Timothy S. McCune

Differential amplifiers made with discrete transistors have significant noise and performance advantages. A single JFET amplifier will provide excellent impedance matching and low-noise amplification. Using a dual JFET wired as a differential amplifier will also largely reject common signals. This important characteristic – Common Mode Rejection – means that selecting the right dual JFET will be the most cost-effective way of improving signal-to-noise ratio in your design. You can't overlook how the part's internal design affects the rejection of unwanted inputs while amplifying the signal as accurately as possible.

All dual JFETs achieve Common Mode Rejection to some extent, but creating a part to optimize this requires specialized design techniques. Linear Systems Founder John H. Hall led this work in the early 1960s as a protégé to industry pioneer Jean Hoerni at Union Carbide's semiconductor division. The need for electrical characteristic matching by the two halves of the dual component over a wide range of temperatures was obvious, but deviations in epitaxial surfaces and other issues made this design work challenging. After heated arguments with more senior developers at Union Carbide, Hall eventually convinced Hoerni to let him try his approach.

Dual transistors – bipolars as well as JFETs – had to that point been created from two separate pieces of silicon. Each die would be tested for specific electrical characteristics and then matched by hand in a special package. At room temperature, duals made this way would match, but as temperatures changed, the characteristics of the separate halves deviated from each other.

To correct this problem, Hall envisioned the most intricate dual design yet conceived. Rather than each half of the dual being set side-by-side, he would weave the transistors together. This design enabled unprecedented matching over a wide range of temperatures, creating very high Common Mode Rejection Ratios.

First with bipolar transistors and later with JFETs, Hall improved the designs of these so-called monolithic tightly matched duals over the course of a 50-year career. Hall and his design team developed new and more capable cross-coupling methods to provide current distribution nearly identical in each half of the dual component. This achieved ultra-close matching over a wide range of temperatures, the key to having consistently high Common Mode Rejection.

Common Mode Rejection Ratio, expressed in dBV, is the common coupled voltage influence over frequency on a differential amplifier input stage. The input of a discrete differential amplifier, most often, is a dual gain element such as a dual Bipolar junction transistor, MOS or junction type Field Effect transistor, Thermionic Triode, Etc. Ideally the input gain element pair is perfectly matched in transconductance (Gm), offset (ΔVin), temperature coefficient (Δt), and noise (Vn). However any two gain elements separated by a finite space will inevitably have differences in these characteristics as a function of spatial differences in fabrication. John Hall's cross-coupled dual device structure was what evolved to mitigate this problem.

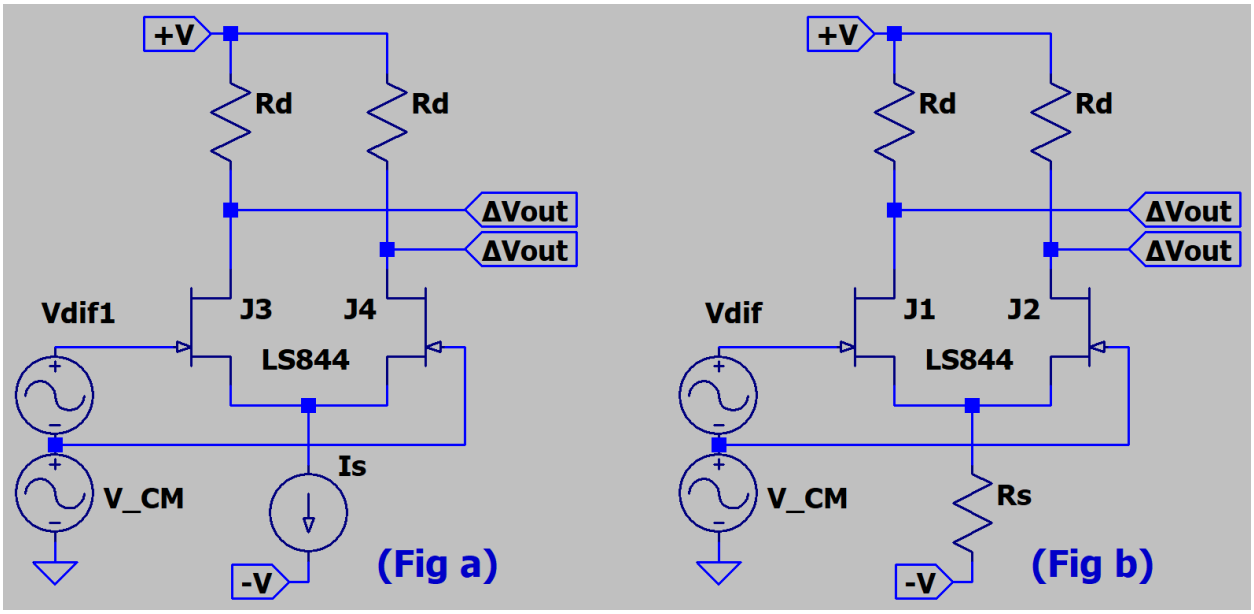
[1] The measure of a differential amp's performance in rejecting undesirable common-mode signals is the ratio of the differential voltage gain (Av(d)) to the common-mode gain (Acm). This ratio is the CMRR.

The measure of a differential amp's performance in rejecting undesirable common-mode signals is the ratio of the differential voltage gain (Av(d)) to the common-mode gain (Acm). This ratio is the CMRR.

Limiting this to Junction FET's, two equally fabricated parts on a silicon wafer adjacent to each other will have differences in doping distribution concentrations, crystal uniformity and thermal offset during processing. Whereas, if both parts occupied the same space, or nearly so, distribution of fabrication differences would approach the same values and therefore approach the ideal. To that end, these JFET device structures are merged, so that the dies are a uniformly interleaved area of both JFET's.

For instance, the LS840 series of Dual JFETs fabricated this way exhibit low common mode noise, and tight matching of VGS and Gm. When used as a differential amplifier, common mode input voltage influence to the differential input voltage is minimized to its lowest value when the sources are current source biased, (High CMMR).

Common source constant current biasing maintains an invariant total drain current regardless of input signal differential amplitude having a common mode voltage influence. (***fig a***) A resistive current bias will have a varied source current and present a ΔV gain where common mode V is involved. (***fig b***) An Audio amplifier potentially benefits from resistive bias by the slight gain variation influence of input signal amplitude promoting even order harmonics. However, Instrumentation amplifiers need high linearity and typically use a constant current source bias. This results in constant total drain current with no gain modulation. Common mode voltage influence on the signal path is significantly diminished when a current source resistance approaches infinity.



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The LSK389A, B, C and D grades of high performance monolithic dual JFETs feature extremely low noise, tight offset voltage and low drift over temperature specifications
LSK389 Series Datasheet and Spice Model
LSK389 Series Application Note

The LSK489 A and B grades are the industry's optimal combination of low input capacitance and extremely low-noise in a monolithic dual N-Channel JFET
LSK489 Datasheet and Spice Model
LSK489 Application Note

The LS844 Ultra-Low Noise, Low-Drift, Monolithic Dual N-Channel JFET Amplifier combines low noise, low input capacitance and our lowest price for a monolithic dual
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LS844 Series Application Note

The LS310 Series Tightly Matched, Monolithic Dual, NPN Transistor is a direct replacement for Analog Devices MAT series and National LM3494 series
LS310 Series Datasheet and Spice Model

The LS350 Series Tight Matching, Monolithic Dual, PNP Transistor is a direct replacement for Analog Devices MAT series parts. It is ideal for Tight Matching, Small Signal, Transistors Amplifier & Switching Applications
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Designing with the LS310 & LS350 Bipolar Transistor Series

General Monolithic Dual JFET Products

LS5905, 5906, 5907, 5908 & 5909 Series, Low-Leakage, Low-Drift, Monolithic Dual, N-Channel JFETs
LS5905 Series Datasheet and Spice Model

2N5564 Low Noise, Monolithic Dual, N-Channel Higher-Frequency JFET
2N5564 Datasheet and Spice Model

LS5911, 5912 & 5912C is a Wideband, High Gain, Monolithic Dual, N- Channel JFETs
LS5911 Series Datasheet and Spice Model

LS830, 831, 832 and 833 Ultra-Low Leakage, Low Drift, Monolithic Dual N-Channel JFETs
LS830 Series Datasheet and Spice Model

LS840, LS841 and LS842 Low Leakage, Low Drift, Monolithic Dual N-Channel JFETs
LS840 Series Datasheet and Spice Model

The SST/U401, 402, 403, 404, 405 and 406 Low-Noise, Low-Drift, Monolithic Dual N-Channel JFETs
SST/U401 Series Datasheet and Spice Model

LS3954, 3954A, 3955, 3956 and 3958 Low Noise, Low Drift, Monolithic Dual, N-Channel JFETs
LS3954 Series Datasheet and Spice Model

U421, 422, 423, 424, 425 and 426 Low-Noise, Low-Drift, Monolithic Dual N-Channel JFETs
U421 Series Datasheet and Spice Model

SST/U440 and U441 Wideband, High-Gain, Monolithic Dual N-Channel JFETs
SST/U440 Series Datasheet and Spice Model

LSJ689 high performance, P-Channel, monolithic dual JFET features extremely low noise, tight offset voltage and low drift over temperature
LSJ689 Datasheet and Spice Model
LSJ689 Application Note

General Bipolar Transistor Dual Products:

The IT120A Series Monolithic Dual, NPN Transistor is a direct replacement for the Intersil IT120 Series
IT120A Series Datasheet and Spice Model

The IT124 Monolithic Dual, NPN Transistor, Super Beta is a direct replacement for Intersil IT124
IT124 Series Datasheet and Spice Model

The IT130A Series Monolithic Dual, PNP Transistor is a direct replacement for Intersil IT130 Series
IT130A Series Datasheet and Spice Model

The LS318 Log Conformance, Monolithic Dual, NPN Transistor is a direct replacement for Micro Power Systems MP318 Series
LS318 Datasheet and Spice Model

The LS3250 Series Tightly Matched, Monolithic Dual, NPN Transistor is a Higher Current Version of the MP310, MP311, MP312, and MP313 Series
LS3250 Series Datasheet and Spice Model

The LS3550 Series Monolithic Dual and Single, PNP Transistor is a Higher Current Version of the MP350, MP 351, and MP352 Series
LS3550 Series Datasheet and Spice Model

The LS358 Log Conformance, Monolithic Dual, PNP Transistor is a direct replacement for Micro Power Systems MP358 Series
LS358 Datasheet and Spice Model

The LS301 Series High Voltage, Super Beta, Monolithic Dual, NPN Transistor is a direct replacement for Micro Power Systems MP301, MP302, MP303 Series
LS301 Series Datasheet and Spice Model

LINEAR SYSTEMS

Quality Through Innovation Since 1987

Interfacing Sensors & Transducers to Data Acquisition Systems in which Large Common Mode Signals are Present

By Brad Albing

Abstract:
A discussion of methods of amplifying and signal-conditioning for sensors with low level outputs in the presence of high ambient electrical noise sources. Advantages and disadvantages of some common amplifier circuits are considered.

Sensors or transducers used in data acquisition systems may have low-level outputs on the order of a few millivolts or milliamperes; or may take the form of a variable resistance on the order of kilo-ohms. Transducer examples include piezo, quartz, condenser, electret, photosensitive (optical) and MEMs devices – commonly used to detect vibration, acceleration, seismic activity, pressure, angle of inclination, light levels, and sound.

Signals from these transducers need amplification. But besides the signals that the transducer produces, there is usually undesirable electrical fields nearby that cause problems. Any additional electrical variations present but undesirable are collectively referred to as noise. Noise sources most commonly encountered are powerline “hum” and switching transients; and clock signals from nearby computers or microprocessors.

Transducers are often two-terminal devices. If the transducer is ground referenced (i.e., one terminal connected to circuit common or ground), it can be thought of as a single-ended devices whose signal can be sent to an amplifier with a single-ended input. In consideration of noise as described (above), note that there is actually signal + noise voltage sent to the amplifier. An example: A thermistor has one end connected to ground and the other end connected to a resistor that in turn connects to a low DC voltage (e.g., +5 V). The junction of the resistor and the thermistor is connected to an op-amp configured as an amplifier. Temperature variations produce a varying voltage at the output of the amplifier. But the relatively high resistance of the thermistor circuitry leaves it susceptible to noise.

Noisy signals need filtering that often takes the form of a low-pass filter (LPF). The LPF can remove some extraneous noise, such as powerline interference and clock signals. Note that these are electrically coupled noise sources, not magnetically coupled. Mitigation of magnetically coupled noise sources is beyond the scope of this Application Note.

Some two-terminal transducers are non-ground referenced and could therefore not be connected to a single-ended input amplifier. Instead, they would have both of their terminals connected to a differential input amplifier/LPF. A microphone with a balanced output connection or a strain gauge that is part of a full (four-element) bridge represents a typical example. With differential sensors, noise is still a problem. However, the noise is often coupled into the two sensor leads in amounts almost equal in magnitude and phase. Thus, the noise is present as a common mode voltage while the sensor signal of interest is present as a differential mode voltage. An ideal differential amplifier has infinite input impedance at each input, equal frequency response at each input, and equal gain but with inverted gain polarity between each input.

A simple differential amplifier using one op-amp is shown in Figure 1. At first glance, this seems like a good choice to amplify the output of a non-ground referenced transducer.

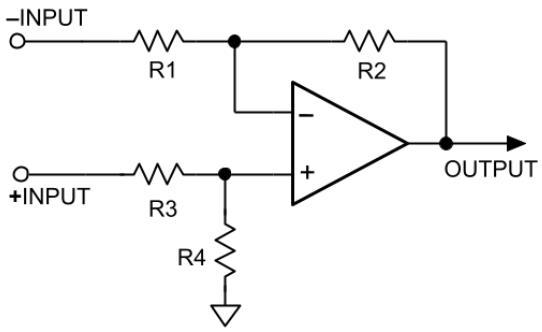

Figure 1: Differential Input Operational Amplifier

If R1 through R4 are the same value, the voltage gain for a signal from a true voltage source (zero internal impedance) applied at the **–**INPUT is –1 V/V. Similarly, the voltage gain for a signal applied to the **+**INPUT is +1 V/V. If the **+**INPUT is connected to ground and a battery whose output was exactly 1.0 V were connected from ground to the **-**INPUT (with its positive terminal to that input), the amplifiers output would be –1.0 V. Connected instead to the **+**INPUT with the **–**INPUT grounded, the output would be +1.0 V. A voltage source of any value (within the operating range of the amplifier) connected to both inputs (tied together) will produce nothing at the output. This is the heart of how a differential amplifier rejects common mode voltages.

While this amplifier appears to meet the requirements for the non-ground referenced transducer cited above, it has a significant problem. The input resistance looking into each of the two inputs is different. For the **+**INPUT, it's R3 + R4; for the **–**INPUT, it's just R1. That's because with an op-amp, the summing junction (the node where R1 and R2 connect to the op-amps negative input) is a virtual ground. Worse yet, when high frequencies are present, instead of input resistance, input impedance must be considered. This includes the resistors, any parasitic shunt capacitance associated with the resistors, input capacitance at the op-amps two inputs, and stray capacitance to ground. Parasitic inductance is present, but usually not a concern for most sensor applications.

These mismatched input impedances degrade the ability of the amplifier to reject common mode voltages present on non-ground referenced transducers. Note that the common mode voltages can easily be an order of magnitude or greater with respect to the differential mode voltages of interest. The figure of merit that describes ability to ignore or reject the common mode voltage is the common mode rejection ratio (CMRR).

Note that besides noise, transducers that are part of a four-element bridge circuit (e.g., a strain gauge) will likely have a DC voltage present (the excitation voltage) that elevates the transducer significantly above ground. Again, the differential amplifier must reject this common mode excitation voltage and just amplify the differential mode voltage from the strain gauge.

The most common work-around to deal with this lack of matching is to buffer each of the two inputs with op-amps. These two op-amps can be configured for unity gain or more, as long as the gains and offset voltages are closely matched. Such a configuration is an instrumentation amplifier (IA) and is shown in Figure 2.

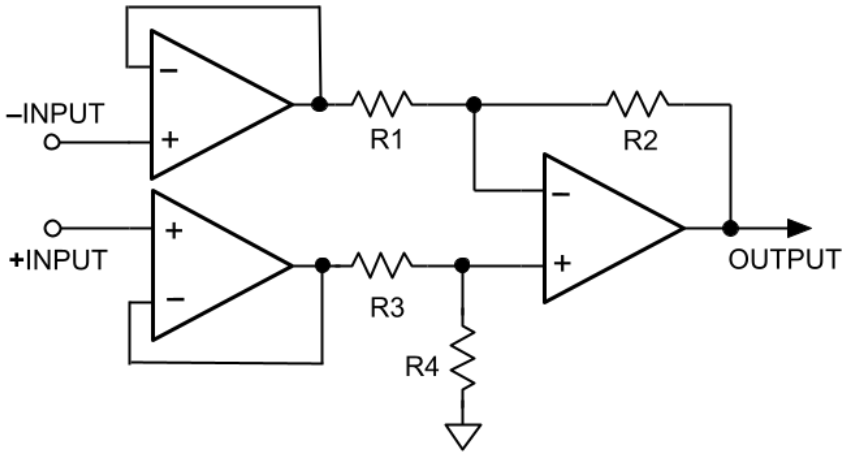

Figure 2: Simple Instrumentation Amplifier

The IA appears to solve the problems cited above. It does not completely. Although not shown in Figure 2, **–**INPUT and **+**INPUT must have resistors connected to ground to supply a path for the op-amps input bias current. The resistors' values can be large (perhaps in the many kΩ range) and must be closely matched. To the extent there is a mismatch in resistance, CMRR is degraded. As before, further degradation occurs due to the parasitic capacitance present both between the inputs and ground. Any capacitance mismatch results in a degradation of CMRR.

To alleviate these shortcomings, a better method relies on a matched pair of junction field effect transistors (JFETs). The LSK489 is an excellent choice: dual JFETs, weaved together in a proprietary way on a single, small die. This results in the C_{iss} (input capacitance) and related parasitic capacitances being low and being well matched. Typical C_{iss} is 4 pF. This helps improve CMRR. And the single die means dual FETs track better over the full temperature range.

Additional advantages provided by the LSK489 dual JFET: That C_{iss} spec is lower than some commonly used JFETs, MOSFETs, or bipolar transistors; the reduced C_{iss} reduces intermodulation distortion.

Besides these general benefits pertaining to IAs, the LSK489 is an excellent choice for audio circuits which may be powered from relatively low voltage (battery operated portable equipment) up to higher voltages such 48 V (phantom-powered microphone circuits). The matched low gate threshold voltage, matched high transconductance, low noise, and matched low capacitance make it the perfect choice for many audio applications.

Moving on to some real-world circuits, consider Figure 3. An LSK489 is configured as a differential input pair. Instead of simply using drain resistors, PNP transistors are used. Configured as an additional differential pair, they increase the transconductance of the differential input stage, increase CMRR, and provide some negative feedback. This negative feedback reduces the stage's distortion.

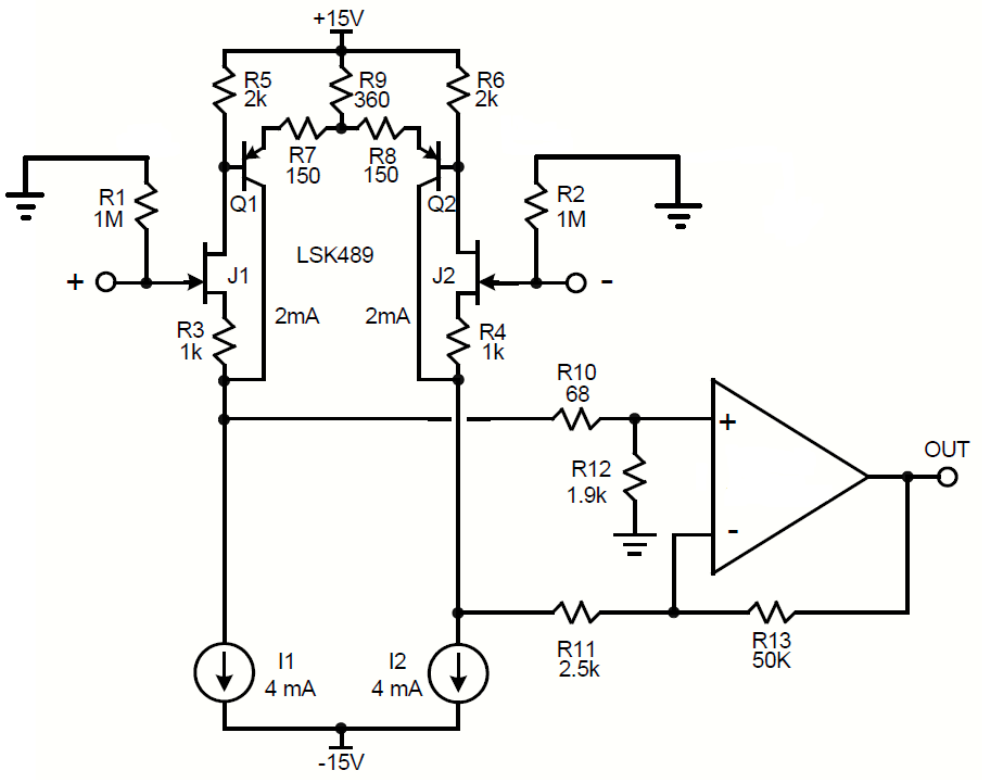

Figure 3: Differential Input Composite Amplifier

This combination of discrete FETs for the input stage plus a bipolar junction transistor (BJT) op-amp is referred to as a hybrid or composite amplifier. This configuration provides performance difficult to obtain in an all BJT or all FET IC op-amp. The FETs have virtually no input bias current and noise current, although they typically have higher noise voltage than BJTs. It is difficult to fabricate good JFETs in the fab process used for BJTs, so the sensible approach uses discrete FETs in front of a good quality, low noise op-amp. For a more detailed look at composite amplifiers along with more details on JFET operation, refer to the LSK489 Application Note. Additional information on FET operation and noise sources can be found in the LSK389 Application Note.

In application in which a higher bandwidth is needed, a cascode circuit can be used. The cascode configuration greatly reduces Miller effect multiplication of capacitance (gate-to-drain) which helps increase bandwidth. The cascode configuration is implemented by using a second pair of FETs as part of the input FETs drain load resistors. The upper two FETs act as source followers and allow the output of the op-amp to drive the drain voltage of the two input FETs. This effectively lowers the input capacitance for these lower two FETs. Additionally, the upper two FETs' drain voltages vary with the differential input voltage which controls the op-amp's inputs.

The cascode configuration also reduces the source-to-drain voltage of the input FETs. This generally reduces noise and power dissipation in the input FETs and is also useful if the supply rail voltage exceeds the breakdown voltage of the FETs. Figure 4 shows a typical application.

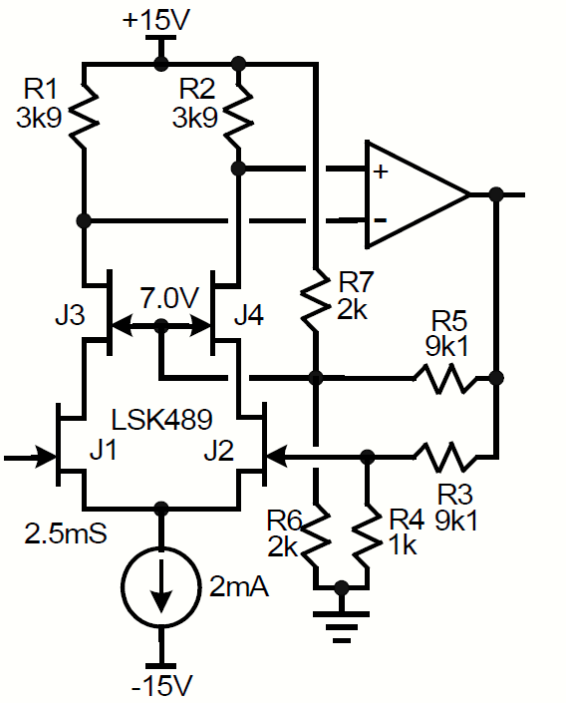

Figure 4: Driven Cascoded FET Pair

Conclusion:

Degradation of sensor signals can occur due to common mode noise sources and poor CMRR of the signal conditioning circuitry. Careful design techniques and well-thought-out amplifier circuitry is mandatory in order to extract signals in electrically noisy environments.

LINEAR SYSTEMS

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Consider the JFET When You Have a Priority Performance Objective

Introduction

Though not as well known as the bipolar transistor or op amp, this long-established transistor still excels in where you need to optimize circuit behavior, such as for lowest noise.

Many engineers are somewhat familiar with discrete bipolar transistors, such as the venerable 2N2222. They are also comfortable with the MOSFET (metal-oxide semiconductor field-effect transistor) as a discrete device for amplifying analog signals and switching power signals, as well as its role as the key digital structural element in large-scale ICs.

But alongside these devices is the JFET (junction field-effect transistor), which was developed soon after the bipolar transistor. To many designers, the JFET is the nearly ideal three-terminal solid-state device, and its operation and parameters are analogous to the vacuum-tube triode. The difference is that the JFET is, of course, a low-voltage, much-more efficient device, although it can't deliver the power that a vacuum tube can. For applications which require extremely low noise, the JFET is often offers superior performance compared to any other discrete device, as well as op amps.

JFET Structure and Operation

Figure 1. Illustrates the cross section of an n-channel JFET.

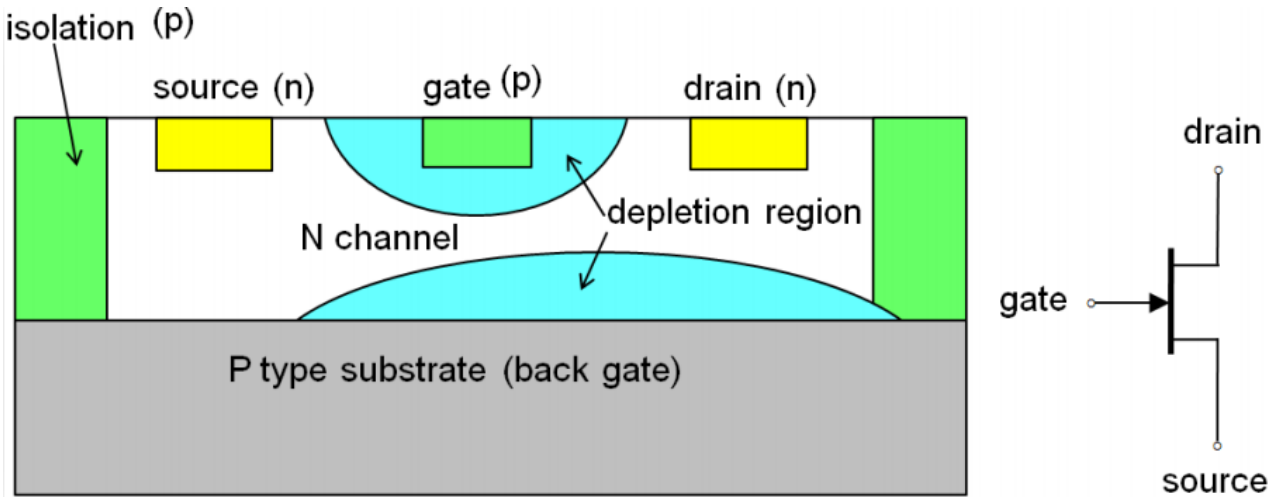

Figure 1. N-channel JFET Cross Section

In this device, there is a conducting, majority-carrier n channel between the source (where majority carriers enter the n-type material) and the drain (where majority carriers leave the material). By applying a negative voltage to the p+ gate, the depletion area widens with reverse bias. It then begins to restrict the flow of electrons between the source and the drain; it’s as if a garden hose is being squeezed. When the gate voltage becomes sufficiently negative, the channel pinches off (symbolized by VP), and the current flow decreases to zero.

Note: Some current flows even with zero gate-source voltage VGS at larger values of drain-source voltage VDS. The basic input/output relationship for VGS = 0V, gate and source are connected to each other, as illustrated in **Figure 2**.

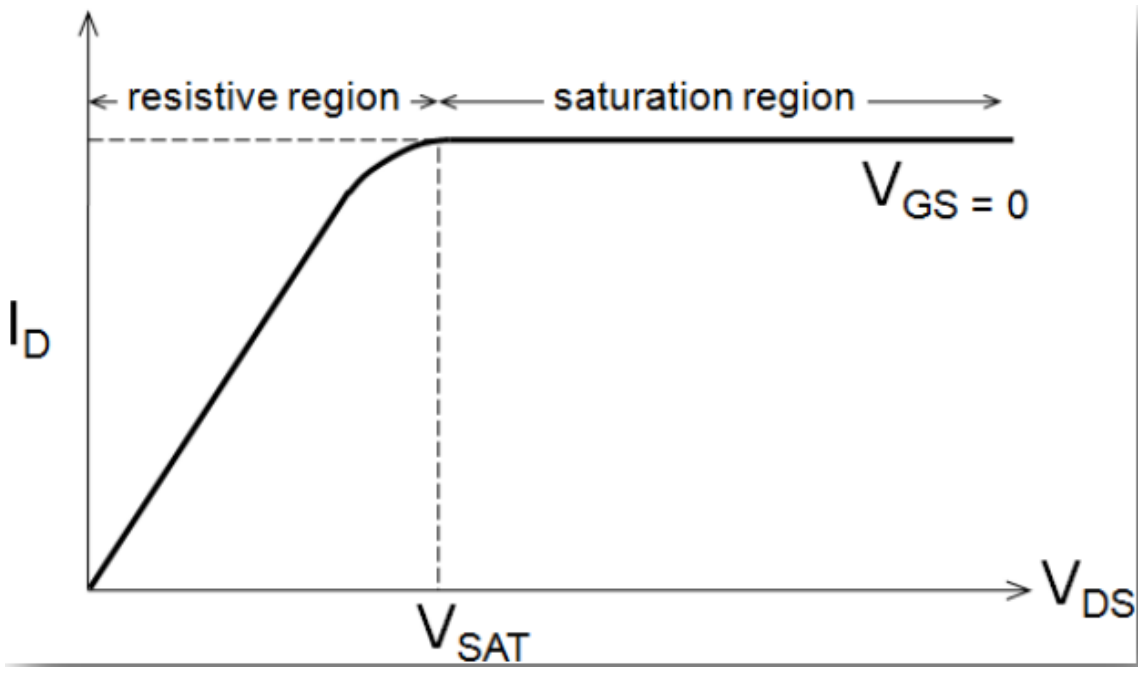

Figure 2 V VGS = 0V Basic Input/Output Relationship

There are two main operating regions:

1. Resistive region (left)
2. Saturation region (right)

In the resistive region on the left, the JFET is operating below its saturation voltage, and an increase in drain-source voltage VDS produces an increase in drain current ID which is very nearly linear. At VDS values above VSAT, there is no increase in ID.

The current flow through the JFET channel is determined by both VDS and VGS, but when VDS is greater than the saturation voltage VSAT—where an increase in VDS does not result in a further increase in drain current ID—then the channel current is determined solely by VGS.

While **Figure 2**. illustrates a single curve, what designers really use is a graph with a family of curves, **Figure 3**.

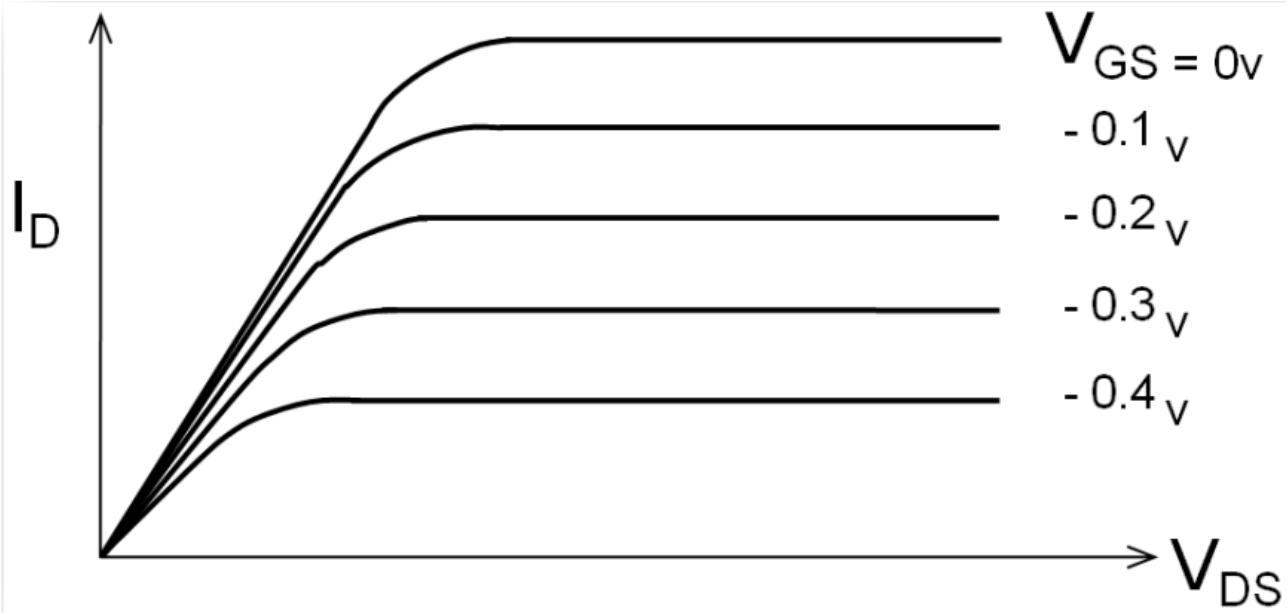

Figure 3 ID Versus VGS

This graph shows ID versus VGS for a set of values of VGS beginning at 0V, and then going increasingly negative in steps, usually with step size of 0.1V or 0.2V.

If you're familiar with the bipolar transistor, you know that its base is forward biased and conducts a base current. In contrast, the p-n junction of the JFET is reverse-biased and the gate current is zero. The result is that the bipolar transistor is a low-impedance device, while the JFET is inherently a high-impedance device.

JFETs and Noise

One area where JFETs can provide clear designer benefit is in audio-band noise, for both conventional audio as well as instrumentation amplifiers for low-frequency, highly sensitive sensors and transducers. The noise model of a JFET, Figure 4. shows the equivalent voltage and current noise sources. The current-noise effect depends on the source impedance RS, while the voltage noise (referred to input) is independent of that impedance.

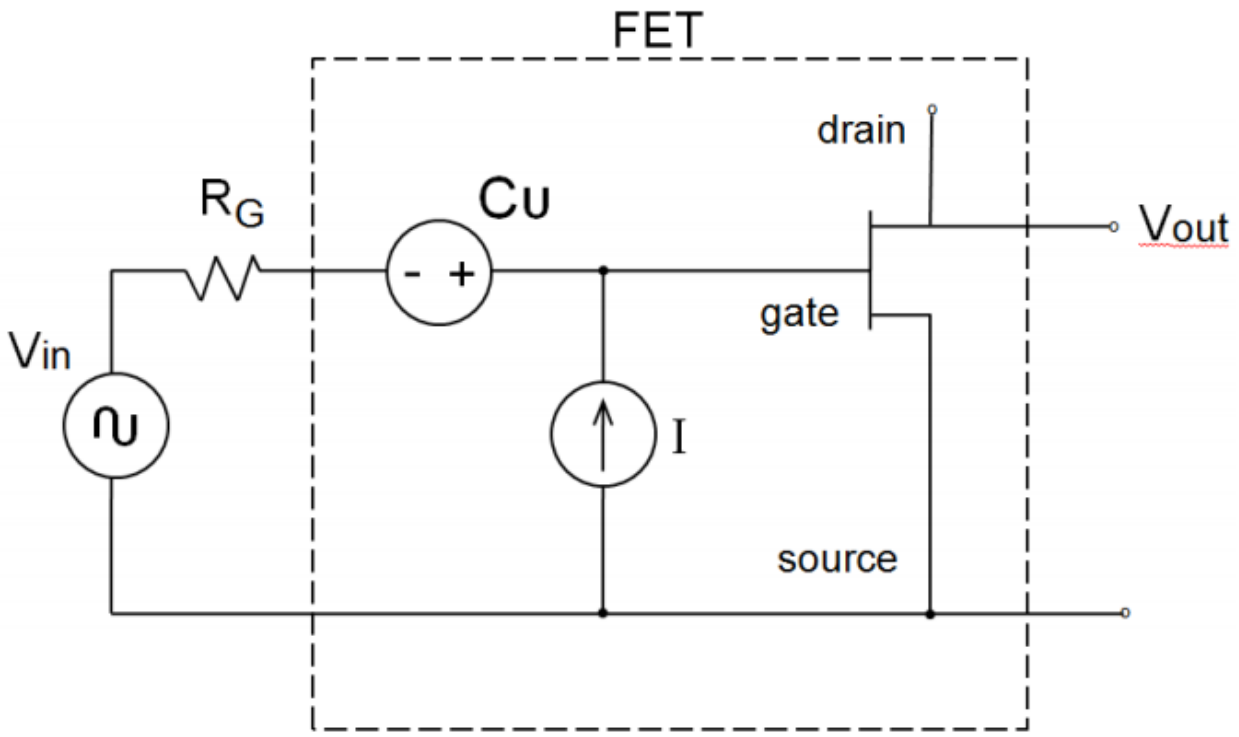

Figure 4 Equivalent Voltage and Current Noise Sources

The JFET has three overlapping noise types; their relative proportions change with frequency:

- Excess or flicker noise, properly called 1/fn , but more often referred to as 1/f noise, is the result of thermally generated reverse current in the gate channel junction; it is usually negligible in low-noise JFETs.
- Thermal noise, also called Johnson or Nyquist noise, is generated in the resistive channel of the JFET; the equivalent short-circuit noise voltage is characterized by the classic value √(4kTRNB) where K is Boltzmann's constant, T is temperature (Kelvin), RN is the equivalent resistance for noise, and B is bandwidth.
- Shot or generator recombination noise, which is related to the flow of current into the gate-source impedance.

What concerns most designers is the JFET noise figure (NF). NF is defined with respect to a reference standard, the generator resistance RG:

NF (in dB) = 10 log10 [1 + ((en2 + in2RG2)/4kTRGB)] where RG is a source resistor added to the circuit.

To determine the lowest noise figure for critical circuits, take the derivative of the NF equation and set it to zero. The result is that for minimum noise, source resistor RG should be set to be equal to en/in. While en will be at a minimum for JFETs when the device is operated at VGS = 0, both en and in vary only slightly as ID changes. In contrast, en and in vary directly with the collector current in bipolar transistors.

In general, JFETs can yield noise figures below 1 dB even in circuits with higher source impedances, reaching up to RG = 1 GΩ. Bipolar transistors will have NFs which are substantially higher, in the range of 5 dB or more.

Other JFET Considerations

Input capacitance of JFETs is relatively high, which will affect frequency response. This capacitance has two components: Ciss, the basic input capacitance, and Crss, the reverse transfer capacitance. While Crss is much lower than Ciss, it is magnified by the Miller effect and thus has a larger impact on overall input capacitance as seen by the source. To reduce this effective input capacitance, designers sometimes use the cascade configuration, which has been used since the days of vacuum tubes.

Temperature coefficient and temperature-induced drift are another related pair of concerns in low-noise, precision designs. It is possible to design the circuit to operate at the single point of zero tempco, which can be calculated by analysis based on the values of VGS and VP versus temperature. However, this approach is both technically difficult and often impractical, since the circuit's operating temperature is often not constant or controllable.

A better approach is based on using a different circuit topology. In place of the basic single-ended amplifier, designers can use a differential design, also called a balanced design. In this approach, two amplifiers are symmetrically configured as "half-circuits" and work both with and against each other. The consequence of this design is that any signals which are common to both half circuits are largely cancelled, characterized by common-mode rejection ratio (CMRR) or common-mode gain (CMG), both in dB; the higher the CMRR or lower the CMG, the better.
This approach works to counter tempco-related drift because changes in JFET parameters such as ID, VGS, and conductance are seen by the configuration as being common-mode signals and thus cancelled. But to make it work to the maximum extent, the two JFETs themselves must have characteristics which are as nearly identical as possible.

There are two ways to achieve this. The first approach is to take a large number of JFETs, test them, and then pair them up as closely as possible. While this is possible in theory and can work in low-volume or custom projects, it is often impractical in practice, especially in a manufacturing or field-repair environment.

A better approach is to use dual monolithic JFETs, where the die contains two devices. Such dual devices inherently usually have nearly identical performance parameters, including their various drift coefficients. Examples of such dual devices include the LSK389 ultra-low noise, monolithic, n-channel JFET pair and LSK489 low-noise, low-capacitance, n-channel JFET pair, both available from Linear Integrated Systems (Fremont, CA).

The LSK389 has lower noise than the LSK489, and while the LSK489's noise is almost as low, it also has much lower typical gate-to-drain capacitance of just 4 pF, compared with 25 pF for the LSK389. Although the noise difference between the two JFETs is not significant for most designs, the lower gate-to-drain capacitance is very important, as the higher capacitance can cause intermodulation distortion (IMD) in some designs.

This lower capacitance results in a much-wider-bandwidth front end for the audio op amp, while also reducing the IMD that the op amp will see.

Conclusion

There are many good, high-performance bipolar transistors, and even op amps, available on the market, no doubts about that. But for applications where the designer is really striving to achieve the highest level of performance in one or two parameters, the JFET can provide the flexibility in specifications, configuration, topology, and associated components needed to achieve these goals.

LINEAR SYSTEMS

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Linear Systems' LSK489 Application Note

By Bob Cordell

P-Channel Dual JFETs Make High-Performance Complementary Input Stages Possible

Introduction

For circuits designed to work with high impedance sources, ranging from electrometers to microphone preamplifiers, the use of a low-noise, high-impedance device between the input and the op amp is needed in order to optimize performance.

At first glance, one of Linear Systems' most popular parts, the LSK389 ultra-low-noise dual JFET would appear to be a good choice for such an application. The part's high input impedance (1 TΩ) and low noise (1 nV/√Hz at 1kHz and 2mA drain current) enables power transfer while adding almost no noise to the signal. But further examination of the LSK389's specification shows an input capacitance of over 20pF. This will cause intermodulation distortion as the circuit's input signal increases in frequency if the source impedance is high. This is because the JFET junction capacitances are nonlinear. This will be especially the case where common source amplifier arrangements allow the Miller effect to multiply the effective value of the gate-drain capacitance. Further, the LSK389's input impedance will fall to a lower value as the frequency increases relative to a part with lower input capacitance.

A better design choice is Linear Systems' new offering, the LSK489. Though the LSK489 has slightly higher noise (1.5 nV/√Hz vs. 1.0 nV/√Hz) its much lower input capacitance of only 4pF means that it will maintain its high input impedance as the frequency of the input signal rises. More importantly, using the lower-capacitance LSK489 will create a circuit that is much less susceptible to intermodulation distortion than one using the LSK389.

The LSK489's lower gate-to-drain capacitance enables more effective, elegant audio circuit designs. The relatively high capacitance of the LSK389 often requires designers to use a cascode circuit to provide the ability to handle higher bandwidths without intermodulation distortion. The cascode does this by eliminating the Miller effect that can multiply the effective gate-drain capacitance and its associated nonlinear effects. However, the cascode adds complexity and noise contributed by the cascode transistors.

The LSK489 is an N-channel dual low-noise, low-capacitance, tightly matched monolithic field effect transistor. It features:

- 3ms transconductance at 2mA drain current
- 1000 GΩ input impedance
- 60V breakdown voltage
- gate-drain capacitance of only 1.5pF
- 4pF input capacitance
- 1.5 nV/√Hz noise at 1kHz
- best low-noise/low-capacitance combination in the industry
- lowest input capacitance per unit gate length in the industry
- lowest noise for a given gate length in the industry
- tight V_{gs} matching at operating bias

The LSK489 is particularly well suited to low-noise, high-gain audio and instrumentation circuits operating from battery voltages up to 60 volts. 48V phantom-powered circuits, like those used in microphone preamplifiers, are especially benefited by the features of the LSK489. Low operating V_{gs}, high *gm*, tight matching, low noise and low capacitance make it well-suited to numerous audio and instrumentation applications.

Sensors, which play such an important role in today's world, benefit greatly from the performance delivered by the LSK489. Such sensor technologies include piezo, quartz, condenser, electret, and MEMs devices. These devices benefit from the LSK489's combination of low input capacitance and low noise. Electrometer applications also benefit from these characteristics.

JFET Operation

The simplified equation below describes the DC operation of a JFET. The term β is the transconductance coefficient of the JFET.

$$I_d = \beta(V_{gs} - V_T)^2$$

At $V_{gs} = 0$, we have I_{dss}:

$$I_{dss} = \beta(V_T)^2$$

β can be seen from I_{dss} and V_T to be:

$$\beta = I_{dss} /(V_T)^2$$

The operating transconductance *gm* is easily seen to be:

$$gm = 2 * \sqrt{\beta * I_d}$$

This last relationship is important, because transconductance of the JFET is what is most often of importance to circuit operation. For a given transconductance parameter β, *gm* is largely independent of I_{dss} and V_T, and goes up as the square root of drain current. This is in contrast to a bipolar transistor where *gm* is proportional to collector current. The value of Beta for the LSK489 is about 1.2e-3.

JFET Amplifier Noise

JFET noise results primarily from *thermal channel noise*. That noise is modeled as the Johnson noise of an equivalent input resistor r_n whose resistance is equal to approximately 0.67/*gm*. If we model the effect of *gm* as *rs'* (analogous to *re'* for a BJT), we have $r_n = 0.67rs'$. Johnson noise is proportional to the square root of resistance, and is about 4 nV/√Hz at a resistance of 1k. A JFET with gm = 3mS will have *rs'* = 333Ω and r_n = 200Ω. Theoretical noise will thus be about √(200/1000) * 4 nV/√Hz = 1.8 nV/√Hz.

The noise relation for a JFET is remarkably similar to the shot noise source for a BJT, which is the voltage noise of a resistor whose value is *re'*/2. The voltage noise of a BJT goes down as the square root of increased I_c because *gm* is proportional to I_c and *re'* goes down linearly as well. However, the *gm* of a JFET increases only as the square root of I_d. As a result, JFET input voltage noise goes down as the ¼ power of I_d.

The LSK489 Noise Advantage

In order to understand the LSK489's noise advantage it is helpful to briefly review the 4 major sources of noise in JFETs.

- Thermal Channel Noise
- Gate Current Shot Noise
- 1/f Noise
- Generation-Recombination Noise

The first two sources of noise are largely fundamental to the device, while the second two sources are largely the result of device imperfections. Examples of such imperfections include lattice damage and charge traps. A major reduction in G-R noise is key to the LSK489's superior noise performance.

Thermal channel noise

Thermal channel noise, as discussed above, is akin to the Johnson noise of the resistance of the channel. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, can vary with the individual device geometry, and is often a bit smaller than 0.67. However, it is unusual for the constant to be less than 0.5.

Gate shot noise current

JFET input current noise results from the shot noise associated with the gate input junction leakage current. This noise is normally very small, on the order of fA per √Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Shot noise increases as the square root of DC current. A useful relationship is that $I_{shot} = 0.57pA/\sqrt{Hz}/\sqrt{\mu A}$ [1]. Alternately, $I_{shot} = 0.57fA/\sqrt{Hz}/\sqrt{pA}$.

Consider a circuit with a 100MΩ source impedance and a JFET at 25°C with input noise current of 4 fA/√Hz. The resulting voltage noise will be 400 nV/√Hz. Leakage current doubles every 10°C, so at 65°C this noise contributor will be about 1600 nV/√Hz. For comparison, the Johnson noise of a resistive 100MΩ source is about 1300 nV/√Hz.

1/f Noise

At very low frequencies the input noise power of a JFET rises as the inverse of frequency. That is why this noise is referred to as 1/f noise. When expressed as noise voltage, this means that the noise rises at a rate of 3dB/octave as frequency decreases. In a good JFET, the 1/f spot noise at 10Hz may be twice the spot noise at 1kHz (up 6dB) when expressed as nV/√Hz.

The noise might typically be up by 3dB at 40Hz. 1/f noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice.[2] The improved processing of the LSK489 contributes to reduced 1/f noise.

By comparison, a good JFET op amp with input noise of 10 nV/√Hz at 1kHz may have its noise up by 3dB at 100Hz and the spot noise at 10Hz might be up by 10dB. At 1Hz that op amp may have spot noise on the order of 65 nV/√Hz.

Generation-Recombination Noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as G-R noise. This *excess noise* is governed by fluctuation in the number of carriers in the channel and the lifetime of the carriers. G-R noise manifests itself as drain current noise. When referred back to the input by the transconductance of the JFET, it is expressed as a voltage noise.

Like 1/f noise, G-R noise results from process imperfections that have created crystal lattice damage or charge trap sites. In contrast, however, G-R noise is not limited to low frequencies. In fact, it is flat up to fairly high frequencies, usually well above the audio band. The G-R noise power spectral density function is described in [2] as:

$$S_{G\text{-}R(f)}/N^2 = [(\overline{\Delta N})^2/N^2] * [4\tau/(1 + (2\pi f\tau)^2]$$

where $(\overline{\Delta N})^2$ is the variance of the number of carriers N, and τ is the carrier lifetime.

Above a certain frequency, the G-R noise power decreases as the square of frequency. When expressed as noise voltage, this means that it decreases at 6 dB/octave. The point where the G-R noise is down 3dB can be referred to as the G-R noise corner frequency. That frequency is governed by the carrier lifetime, and in fact is equal to the frequency corresponding to a time constant that is the same as the carrier lifetime.[2] We have,

$$f_{G\text{-}R} = 1/2\pi\tau$$

where τ is the carrier lifetime.

The 6 dB/octave high-frequency roll-off of G-R noise is only an approximation because there are normally numerous sites contributing to G-R noise and the associated carrier lifetimes may be different. As a result, the G-R noise corner frequency is poorly defined and the roll-off exhibits a more shallow slope than 6 dB/octave over a wider range of frequencies. The inflection in the JFET's noise vs. frequency curve may thus be somewhat indistinct. The important take-away here is that excess G-R noise can often exceed the thermal channel noise contribution and thus dominate voltage noise performance of a JFET.

JFET voltage noise spectrum and contributors

The idealized noise spectral density graph in Figure 1 illustrates how the three voltage noise contributors act to create the overall noise versus frequency curve for a JFET. In the somewhat exaggerated case illustrated, G-R noise dominates thermal channel noise.

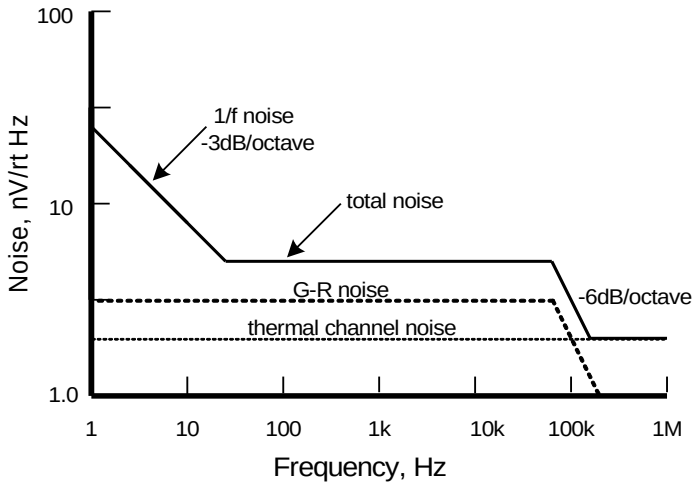

Figure 1: JFET Voltage Noise

LSK489 Noise improvement

The LSK489 noise advantage derives from process improvements that reduce device imperfections. Those imperfections create G-R noise and 1/f noise. Such process imperfections include crystal lattice damage and charge trap sites. Put simply, most JFETs are not as quiet as they can be. The process improvements made in the LSK489 have reduced both 1/f noise and G-R noise.

With the exception of its superior noise performance, the LSK489 is nearly identical to the LS844. Its device geometry and electrical performance are essentially the same; the only difference is the more advanced processing that reduces device imperfections.

The Common Substrate

The LSK489 is a monolithic dual JFET in which the substrate is shared between the two integrated JFET devices. The two gates are isolated from the common substrate through reverse-biased substrate diodes as shown in Figure 2. The anodes of these diodes are connected to the gates while the cathodes are connected to the common substrate. The substrate is not normally accessible, and it harmlessly floats as a result.

In some applications it is important to take these isolation diodes and the common substrate into consideration. The 6-pin versions of the LSK489 simply float the substrate, while the 8-pin SOIC package brings out the substrate for possible connection by the user. In some applications the floating substrate can be a very weak source of crosstalk between the gates. In other applications, the DC voltage to which the substrate floats may be of interest. The gate-substrate capacitance, which is a function of gate-substrate reverse bias, may influence performance in some applications. In some applications it may be useful to connect the substrate to a fixed DC voltage. Another possibility is to bootstrap the substrate with signal to yet further reduce the capacitive effects of the substrate diodes.

Limits on the operating bias voltages of the two sections of the dual JFET must be considered. This is usually not an issue when the dual JFET is employed as a differential pair, but may be an issue in some other circuit arrangements.

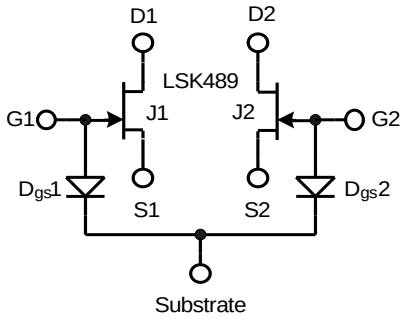

Figure 2: LSK489 Common Substrate

JFET Buffers

Figure 3 shows the LSK489 connected as a simple unity-gain source follower buffer. In (a) an output voltage offset equal to V_{gs} will result. If a dual JFET like the LSK489 is used, the circuit in (b) can be used. J2 acts as the pull-down current source. Because of the tight matching between J1 and J2, the same V_{gs} will appear across R2 and R3, resulting in an output voltage with nearly zero offset. A circuit like this built with a randomly selected LSK489 exhibited offset of only 5mV. R3 can be conveniently trimmed to adjust for zero offset. In (c) the gate bias resistor R1 has been bootstrapped to provide higher input resistance. R4 and R5 help stabilize the output voltage to near 0V. Here resistor R2 creates the same voltage offset in the gate of J2 as exists in the gate circuit of J1.

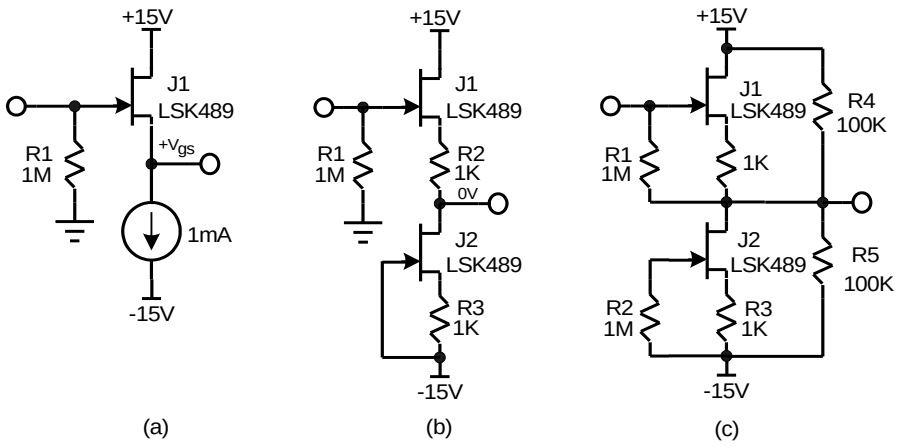

Figure 3: LSK489 Source Followers

Figure 4(a) illustrates a differential buffer with low output impedance and low distortion. The key to this design is that each JFET is connected in a complementary feedback pair (CFP) configuration with a PNP transistor, greatly augmenting its effective transconductance and providing distortion-reducing local negative feedback. Notice that the PNP transistors are actually connected as a differential pair, providing additional common-mode rejection. For a given choice of R3 and R4, the value of the current sources can be chosen to make the common-mode DC offset at the output fairly small. If the current sources are controlled by common-mode feedback from the outputs, common-mode offset can be made very small.

Figure 4(b) shows how the differential JFET buffer can be used to build an audio power amplifier with very high impedance differential inputs by buffering the relatively low input impedance presented by the power amplifier connected as a differential amplifier.

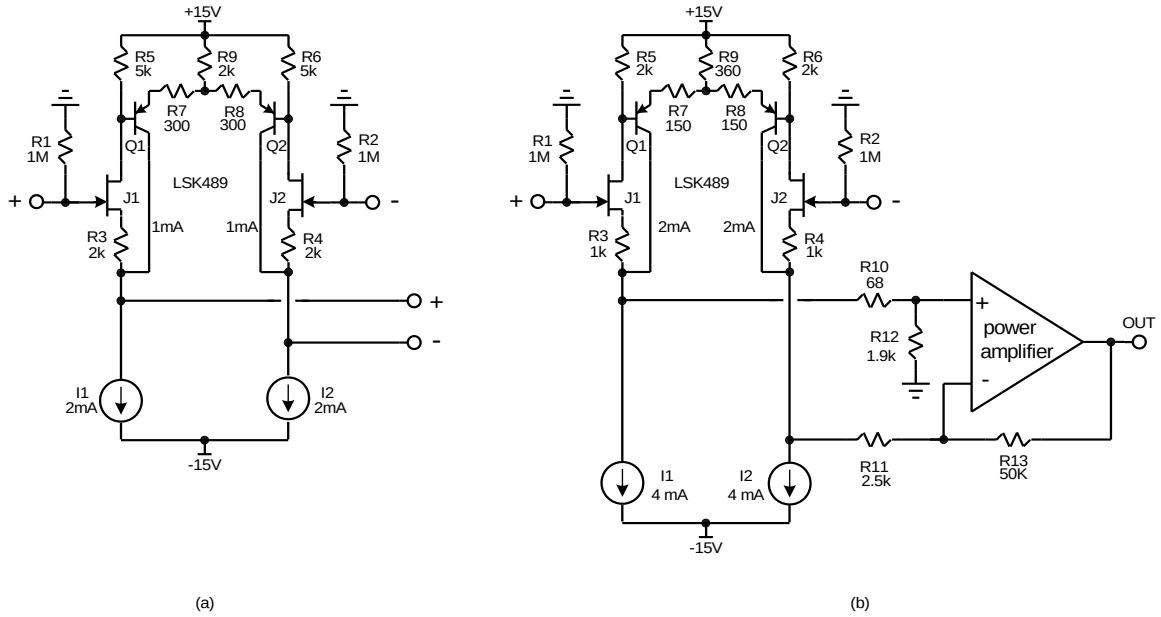

Figure 4: Differential CFP FET Buffer

JFET Hybrid Op Amps

It is often desirable to combine the low noise and simplicity of a good BJT op amp with the high input impedance of a JFET input. IC JFET op amps offer many advantages over BJT op amps, including the absence of input bias current and input noise current. However, they inevitably have greater input voltage noise, often no better than about 8 nV/√Hz. Low-noise BJT op amps easily achieve input voltage noise levels of 1.5 nV/√Hz. It is more difficult to implement good JFETs in a bipolar IC process. For this reason it is sometimes advantageous to employ a discrete JFET input stage in front of a high-performance bipolar op amp.

Figure 5 shows several ways in which a high-impedance JFET input can be added to a BJT op amp so as to reap the advantages of both technologies. In (a) a pair of source followers is simply put in front of the op amp, eliminating the BJT input bias current and input noise current. This arrangement has the disadvantage that the input noise of the op amp adds to that of the JFETs.

In (b) a JFET differential pair with a gain of 10X is placed in front of the op amp. The gain of the JFET stage swamps out the noise contribution of the op amp and increases total open-loop gain by 20dB. If a unity-gain compensated op amp is used, the arrangement must be used with closed loop gain greater than 10 for stability. In this case, a 20dB gain stage can be made that has the same high open-loop gain as the op amp were it used by itself in a unity-gain configuration. In some cases the extra pole created at the input of the op amp may require more conservative frequency compensation.

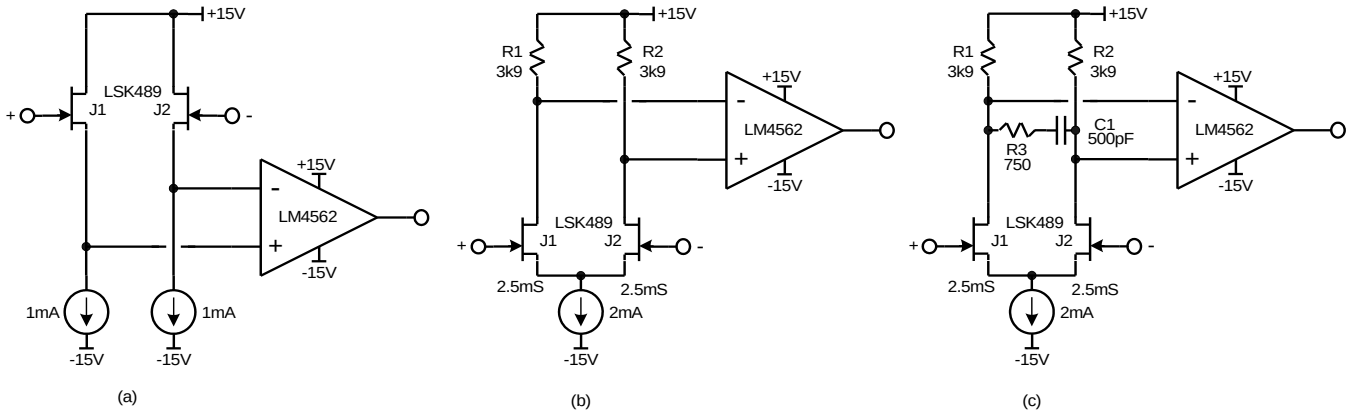

Figure 5: JFET Op Amps

In (c), a compensation arrangement is shown that allows the circuit of (b) to be configured for closed loop gain as low as unity. This is accomplished by R3 and C1, which add a pole-zero pair that decreases open-loop gain by 20dB at high frequencies well before the unity loop gain frequency is reached. The overall effect is like that of so-called two-pole compensation (TPC) sometimes used in feedback amplifiers to achieve higher loop gain at lower frequencies.

There is, however, a very important caveat with this arrangement when used at low closed-loop gain: the circuit is susceptible to latch-up. If the op amp output drives the gate of J2 to the point where it runs out of drain voltage headroom, the circuit may latch to the positive rail. Such behavior is much more likely when the feedback network provides little attenuation as in circuits with unity or low closed-loop gain.

Cascoded JFETs

Single-ended and differential JFET amplifier stages are often cascoded in order to add voltage headroom, reduce Miller effect or to increase output impedance of the stage. The cascode device can be either a BJT or another JFET. If the cascode device is a JFET, all of the signal current from the amplifying JFET passes through the cascode device(s) and no noise is added to the signal. If the cascode device is a BJT, some noise will be added as a result of base current noise flowing from the base to the cascode reference voltage. This adds noise to the signal. However, this noise must be put into perspective in comparison with the noise of the amplifying JFET. This can be evaluated by simulation. It is important that the BJT cascode transistor be a low-noise device with high beta.

Figure 6 shows some simple circuits where the amplifying JFET is cascoded. Sometimes it is necessary to cascode a JFET in order to achieve higher bandwidth by eliminating the Miller effect multiplication of the gate-drain capacitance, even in cases where C_{rss} is already low as with the LSK489. Cascoding may also be necessary when higher-voltage rails are used or when it is desirable to keep the drain-source voltage of the amplifying JFETs small to minimize dissipation or noise.

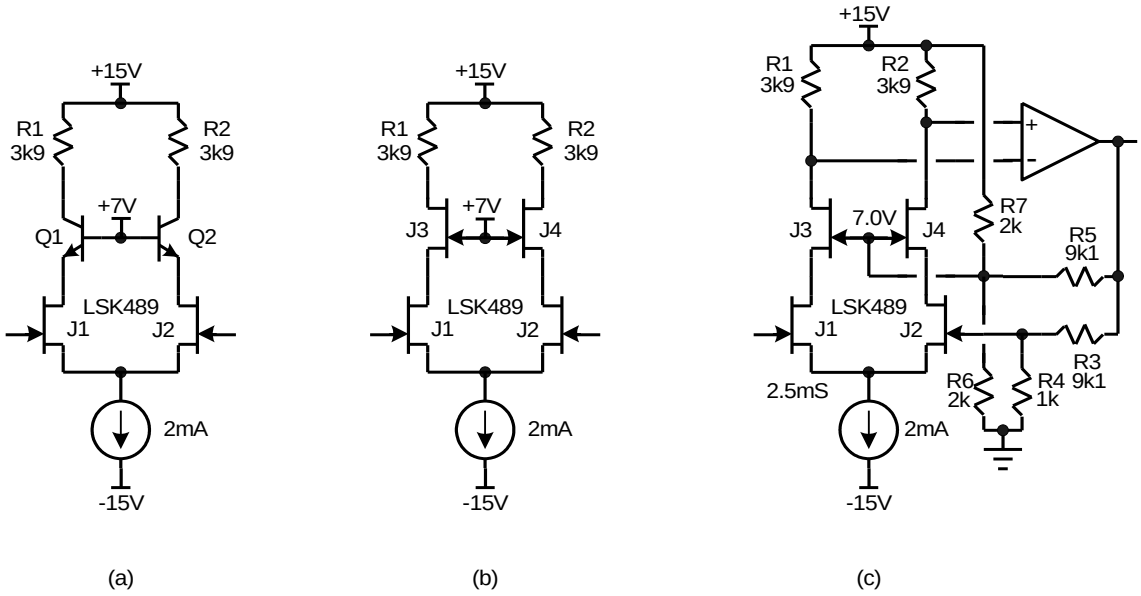

Figure 6: JFET Cascodes

Figure 6(a) shows a conventional arrangement where bipolar transistors are used for the cascade function. Some shot noise from the base current is added to the signal. In (b), JFETs are used for the cascodes, largely eliminating any noise penalty from the use of a cascode.

The circuit in (c) bootstraps the drains of J1 and J2 so as to nearly eliminate the effective input capacitance from C_{rss}. This is done by driving the gates of cascodes J3 and J4 with a replica of the feedback signal that is fed to the gate of J2. This is referred to as a *driven cascode*. Although the cascode circuits illustrated here are all differential cascodes, all of the principles and techniques apply to single-ended cascode circuits as well.

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Phono Preamp

The LSK489 is especially attractive for use in high-performance moving magnet (MM) phono preamplifiers. It can achieve very low noise while presenting very high input impedance to the MM cartridge. The absence of input bias current in the JFET design eliminates input noise current from which BJT designs suffer. Resistance to EMI and a soft overload characteristic make the JFET choice even more attractive.

The MM cartridge source impedance rises at higher frequencies due to the resonance formed by the cartridge inductance (on the order of 300-600 mH) and the load capacitance. This resonance usually lies around 18-22kHz and can have substantial Q. At the resonance frequency, the impedance can rise to almost the nominal load resistance of 47k. This raises the possibility of cartridge interaction with the nonlinear input capacitance of the amplifier. The low input capacitance of the LSK489 JFET pair reduces cartridge interaction and high-frequency intermodulation distortion. Moving magnet cartridges are usually designed to work with a specific loading capacitance on the order of 200pF, so an input stage with capacitance on the order of 20pF, like that of an LSK389, may create a significant disturbance, especially given that the JFET input capacitance can be nonlinear.

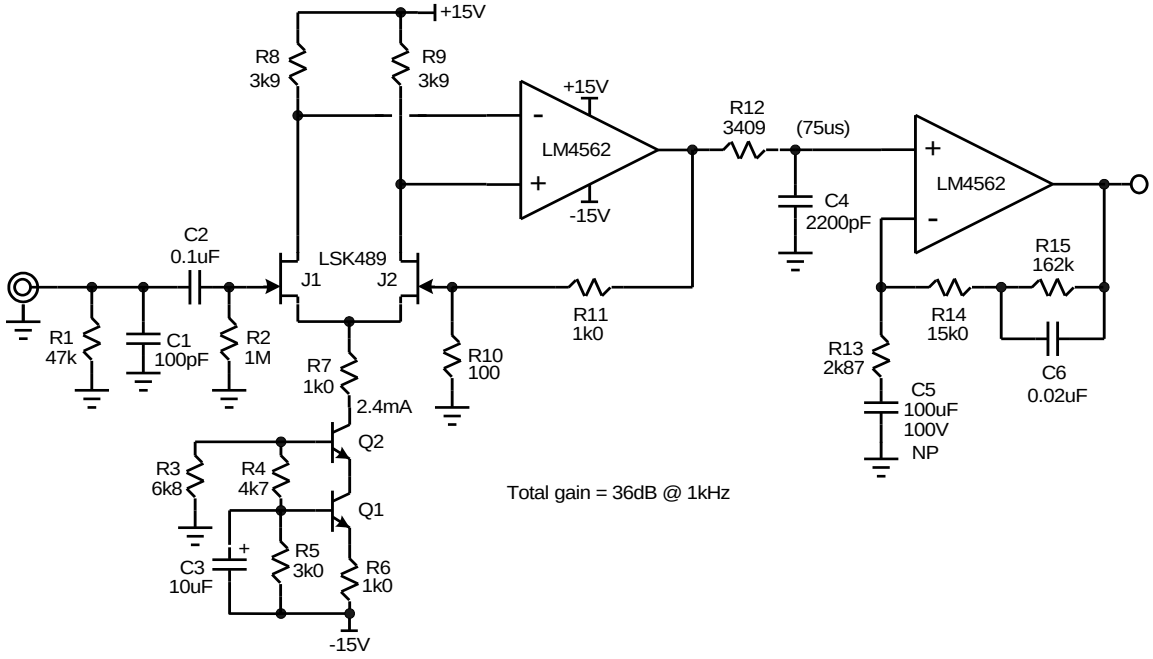

Figure 7: Phono Preamp

Figure 7 illustrates a phono preamp design that incorporates the LSK489 to achieve low noise and high input impedance. The circuit consists of a hybrid JFET-bipolar op amp that uses the LSK489 as its low-noise input stage. The low-distortion, low-noise LM4562 completes the hybrid operational amplifier, which is configured for a flat gain of 21dB. The 75us high-frequency corner of the RIAA equalization characteristic is implemented by R12 and C4. The remainder of the RIAA equalization implements time constants at 3180 and 318µs. It is implemented with the second half of the LM4562 op amp and the surrounding feedback network. Total gain of the preamp is 36dB at 1kHz. The LSK489 JFET input stage provides exceptional immunity to EMI.

The author's VinylTrak phono preamp [3] uses a similar arrangement, but the front-end stage is a discrete 20-dB amplifier without negative feedback. That design provides a true high-impedance differential input and very soft overload characteristics. The small signal levels from a moving magnet phono cartridge allow distortion in the no-feedback arrangement to be very low.

Dynamic Microphone Preamp

The requirements for a dynamic microphone preamp are not unlike those of a phono preamp, since the voltage levels and source impedance are similar. Low input voltage and current noise is important. The microphone preamp does not require equalization, but it must accept a balanced input and have a very large controllable gain range. The LSK489's combination of low noise and low input capacitance make it an ideal device for this application. Its strong resistance to EMI effects and its soft overload characteristics further enhance sound quality.

The LSK489 front-end can be implemented as a differential amplifier without negative feedback. This provides a true high-impedance differential input with exceptionally soft overload characteristics. The input stage consists of a degenerated differential a pair of JFETs, each with a current source connected to the source. The gain of this stage is set by a variable resistance connected from source to source. Drain load resistors create a differential output that is fed to an op amp configured as a differential amplifier. In such a design, the relatively low transconductance of the JFETs limits the amount of gain that can be obtained.

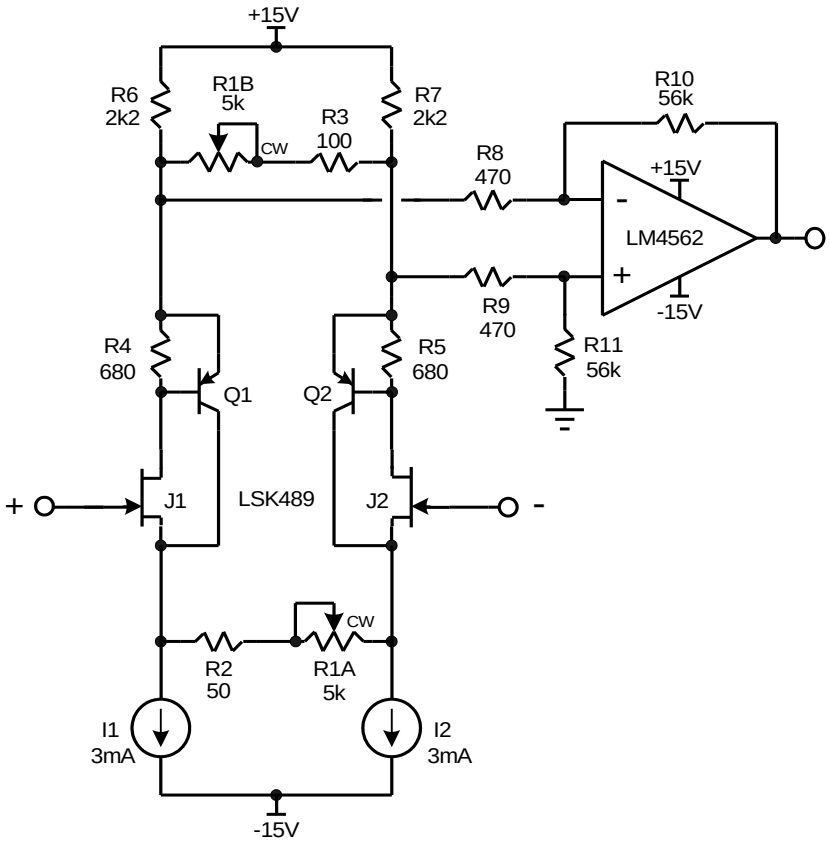

Figure 8: Dynamic Mic Preamp

An improved design is shown in Figure 8. Each JFET is configured as a complementary feedback pair (CFP) by adding a PNP transistor in the drain circuit. This arrangement increases the effective transconductance of the JFET by a factor of about 50 and provides local distortion-reducing feedback. The JFETs are biased at 1mA and the BJTs are biased at 2mA. Gain control over a wide range is difficult to achieve with a single variable resistance in the source circuit, so a second pot ganged with the first is added in a differential shunt arrangement in the drain circuit. A gain adjustment range of 6-60dB is achieved with a single knob, and is usably distributed with respect to pot rotation even when using linear pots. The use of log-taper pots can provide an even more uniform distribution of attenuation vs. rotation.

Input noise is only 5 nV/√Hz at the highest gain setting and harmonic distortion is no more than 0.012% at an output level of 5V peak. At a nominal line level of 1V rms, THD is 0.003% at a 60dB gain setting and falls below 0.001% at gain settings less than +50dB. Even though the circuit appears differential and symmetrical, distortion is dominated by the much more benign second harmonic. This is due to the asymmetry created in the drain circuit by the differential op amp configuration. It results in different signal amplitude at the drains of J1 and J2. Distortion above the 3rd harmonic is virtually absent.

Condenser Microphone Preamp

The LSK489's combination of low noise and low input capacitance make it an ideal device for the input stage of condenser and electret microphones.

A condenser microphone typically consists of a condenser microphone capsule and a built-in amplifier. The output of the condenser microphone is then fed to the input of a conventional dynamic microphone preamp located in the mixing console. The condenser microphone capsule comprises a diaphragm capacitor that is charged to 40-60V. It produces a voltage when the acoustic vibrations of the diaphram change the capacitance while charge is conserved. The capacitance may be as small as 5pF but is often in the neighborhood of 50pF. The output impedance of the capsule is thus extremely high, and the microphone preamp functions mainly as a buffer, since the output voltage of the capsule is fairly high in comparison to the output voltage of a dynamic microphone.

The extremely high capacitive source impedance of the capsule means that the amplifier must present an extremely high load resistance in order to preserve low frequency response. This resistance may be on the order of 1-10 GΩ. For the same reason, the preamplifier input capacitance must be very low, especially if it is nonlinear like that of a semiconductor junction. The low input capacitance of the LSK489 is an advantage here. In fact, in condenser microphone preamplifiers the drain of the JFET is usually bootstrapped with signal to further reduce the effect of C_{rss}. While most condenser microphone preamps use a single-ended JFET input stage, the differential amplifier arrangements made possible by the dual monolithic LSK489 can provide lower distortion in the presence of the fairly high input voltages that can be present with a condenser microphone capsule under high SPL conditions.

The small gate input current of a JFET can come into play in circuits like a condenser microphone preamplifier. The input is AC-coupled and the gate is biased with a resistor as large as 10GΩ so as to provide extremely high input impedance. The JFET's gate input current flows into the resistor, creating a positive voltage offset. The maximum operating value of gate current for the LSK489 is 25pA at 25°C (2pA typ.). This gate input current will create an offset of +250mV. Moreover, the gate leakage current will double every 10°C. Consider a condenser microphone lying in the hot sun reaching a temperature of 45°C. Maximum gate current could reach 100pA, with a resulting input offset voltage of +1V. Such an offset can be disruptive to some circuits. Offset voltage created by gate current flowing in the very large gate return resistor can be controlled by a DC servo connected to the return end of that resistor.

The voltage gain of the preamp may often be on the order of 20dB or less. In fact, for more sensitive capsules and high sound levels, attenuation of the signal may be necessary. A useful approach to such attenuation is to employ an input pad that creates a capacitance voltage divider with an attenuation of perhaps 20dB. A 5pF capsule with a 47pF shunt capacitance will enjoy such a level of attenuation. The low noise of the LSK489 means that the input attenuator can be engaged over a wider operating dynamic range. Finally, the condenser microphone electronics must be powered by so-called "phantom" powering. Only a few milliamperes are available, so low-power electronics are a must.

Piezo Accelerometer Charge Amplifier

Figure 9 shows a Piezo accelerometer charge amplifier. In this design, the gain is set by a shunt feedback arrangement that uses capacitors instead of resistors. The gain is equal to the ratio of the transducer capacitance to the feedback capacitance C1. This amplifier incorporates an extremely high gate return resistance of 10GΩ.

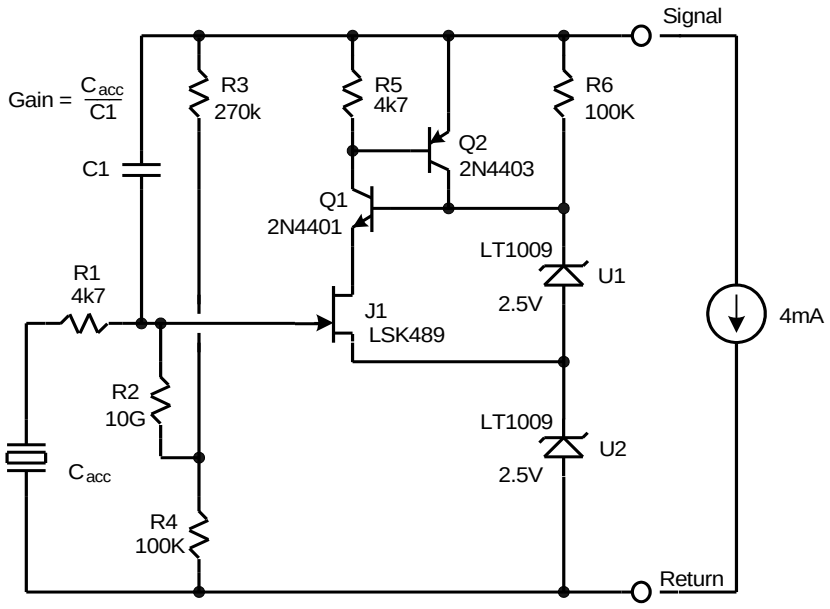

Figure 9: Piezo Accelerometer Charge Amplifier

Discrete JFET amplifier

Figure 10 shoes a discrete JFET amplifier that employs a folded cascode and a diamond buffer output stage. This is much like the low-noise discrete input stage of the author's VinylTrak phono preamplifier [3]. As shown the amplifier is operated open-loop at a gain of about 10, as determined by shunt resistor R14. The amplifier in this configuration offers a true balanced high-impedance input, exceptional resistance to EMI and a very soft overload characteristic.

The amplifier can also be used as an operational amplifier with fairly high open-loop gain if R14 is removed and suitable feedback compensation is added. In any configuration, the use of the folded cascode architecture offers wide bandwidth.

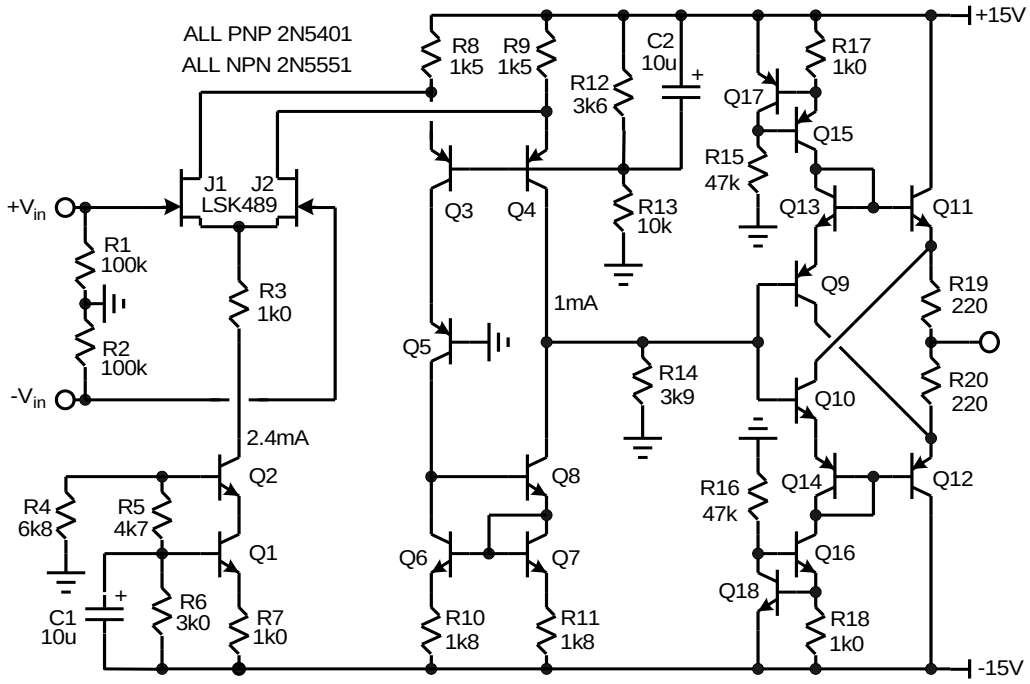

Figure 10: JFET Discrete Amplifier

Power amplifier with JFET input

The input stage for an audio power amplifier is often a long-tailed differential pair (LTP) implemented with bipolar transistors. Dual JFETs like the LSK489 provide a better alternative. Many believe that the sound is better, possibly due to its much softer overload characteristic. Others believe that its superior resistance to EMI is important. The absence of input bias current for the JFET often has advantages in DC offset control and selection of input stage operating impedances.

While the noise characteristics of a power amplifier are often not as critical as those of a preamp, it is still important to achieve low noise because there is no volume control in the power amplifier to reduce noise from the input stage under normal listening conditions. This is particularly so when the amplifiers are used with high-efficiency loudspeakers. For this reason the use of a low-noise JFET like the LSK489 is desirable.

Figure 11 shows a simple100 watt audio power amplifier with a JFET input stage incorporating an LSK489 differential pair. Input noise is only 6 nV/√Hz. The 60V breakdown of the LSK489 allows the use of a JFET input without a cascode for amplifiers with nominal rail voltages of up to 50V, assuming that the rail voltages do not exceed 60V under worst case light-loading and high mains voltage conditions.

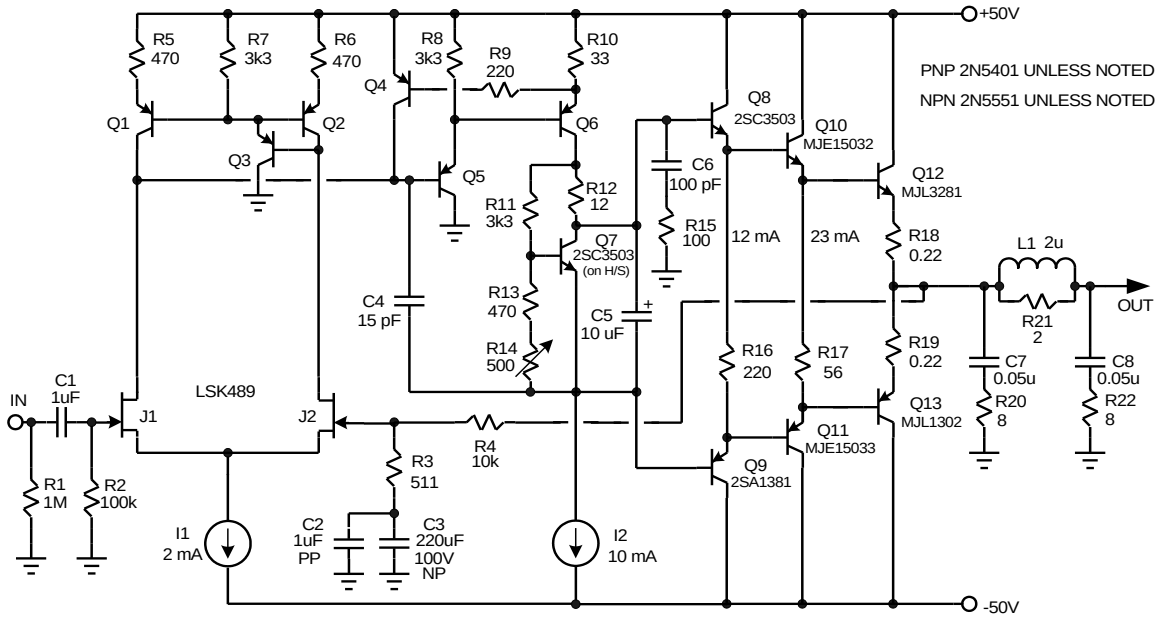

Figure 11: Power Amplifier

Assuming that the rail voltages do not fall to under 45V under full power into an 8Ω load, the amplifier is capable of output power in excess of 100 watts into 8 ohms (corresponding to a peak output voltage of 40V). For simplicity, details of the current sources and output protection circuits are not shown. The design of audio power amplifiers like this can be found in the book *Designing Audio Power Amplifiers*, written by the author. Useful information can also be found on the author's web page at www.cordellaudio.com [4].

Conclusion

With its low noise, low input capacitance and tight matching, the LSK489 is ideal for numerous audio and instrumentation applications. Its low capacitance also make it a good candidate for many high-frequency circuits.

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APPLICATION NOTE

By: Bob Cordell

N-Channel Dual JFETs Make High-Performance Complementary Input Stages Possible

Introduction

For circuits designed to work with high impedance sources, ranging from electrometers to microphone preamplifiers, the use of a low-noise, high-impedance device between the input and the op amp is needed in order to optimize performance.

At first glance, one of Linear Systems' most popular parts, the LSK389 ultra-low-noise dual JFET would appear to be a good choice for such an application. The part's high input impedance (1 TΩ) and low noise (1 nV/√Hz at 1kHz and 2mA drain current) enables power transfer while adding almost no noise to the signal. But further examination of the LSK389's specification shows an input capacitance of over 20pF. This will cause intermodulation distortion as the circuit's input signal increases in frequency if the source impedance is high. This is because the JFET junction capacitances are nonlinear. This will be especially the case where common source amplifier arrangements allow the Miller effect to multiply the effective value of the gate-drain capacitance. Further, the LSK389's input impedance will fall to a lower value as the frequency increases relative to a part with lower input capacitance.

A better design choice is Linear Systems' LS844. Though the LS844 has slightly higher noise (2.5 nV/√Hz vs. 1.0 nV/√Hz) its much lower input capacitance of only 4pF means that it will maintain its high input impedance as the frequency of the input signal rises. More importantly, using the lower-capacitance LS844 will create a circuit that is much less susceptible to intermodulation distortion than one using the LSK389.

The LS844's lower gate-to-drain capacitance enables more effective, elegant audio circuit designs. The relatively high capacitance of the LSK389 often requires designers to use a cascode circuit to provide the ability

to handle higher bandwidths without intermodulation distortion. The cascode does this by eliminating the Miller effect that can multiply the effective gate-drain capacitance and its associated nonlinear effects. However, the cascode adds complexity and noise contributed by the cascode transistors.

The LS844 is an N-channel dual low-noise, low-capacitance, tightly matched monolithic field effect transistor. It features:

- 3ms transconductance at 2mA drain current
- 1000 GΩ input impedance
- 60V breakdown voltage
- gate-drain capacitance of only 1.5pF
- 4pF input capacitance
- 2.5 nV/√Hz noise at 1kHz

- best low-noise/low-capacitance combination in the industry
- lowest input capacitance per unit gate length in the industry
- lowest noise for a given gate length in the industry
- tight V_{gs} matching at operating bias

The LS844 is particularly well suited to low-noise, high-gain audio and instrumentation circuits operating from battery voltages up to 60 volts. 48V phantom-powered circuits, like those used in microphone preamplifiers, are especially benefited by the features of the LS844. Low operating V_{gs}, high *gm*, tight matching, low noise and low capacitance make it well-suited to numerous audio and instrumentation applications.

Sensors, which play such an important role in today's world, benefit greatly from the performance delivered by the LS844. Such sensor technologies include piezo, quartz, condenser, electret, and MEMs devices. These devices benefit from the LS844's combination of low input capacitance and low noise. Electrometer applications also benefit from these characteristics.

JFET operation

The simplified equation below describes the DC operation of a JFET. The term β is the transconductance coefficient of the JFET.

$I_d = \beta(V_{gs} - V_T)^2$

At $V_{gs} = 0$, we have I_{dss}:

$I_{dss} = \beta(V_T)^2$

β can be seen from I_{dss} and V_T to be:

$\beta = I_{dss} /(V_T)^2$

The operating transconductance *gm* is easily seen to be:

$$gm = 2 * \sqrt{\beta} * I_d$$

This last relationship is important, because transconductance of the JFET is what is most often of importance to circuit operation. For a given transconductance parameter β, *gm* is largely independent of I_{dss} and V_T, and goes up as the square root of drain current. This is in contrast to a bipolar transistor where *gm* is proportional to collector current. The value of Beta for the LS844 is about 1.2e-3.

JFET amplifier noise

JFET noise results primarily from *thermal channel noise*. That noise is modeled as the Johnson noise of an equivalent input resistor r_n whose resistance is equal to approximately 0.67/*gm*. If we model the effect of *gm* as *rs'* (analogous to *re'* for a BJT), we have $r_n = 0.67rs'$. Johnson noise is proportional to the square root of resistance, and is about 4 nV/√Hz at a resistance of 1k. A JFET with gm = 3mS will have *rs'* = 333Ω and r_n = 200Ω. Theoretical noise will thus be about √ (200/1000) * 4 nV/√Hz = 1.8 nV/√Hz.

The noise relation for a JFET is remarkably similar to the shot noise source for a BJT, which is the voltage noise of a resistor whose value is *re'*/2. The voltage noise of a BJT goes down as the square root of increased I_c because *gm* is proportional to I_c and *re'* goes down linearly as well. However, the *gm* of a JFET increases only as the square root of I_d. As a result, JFET input voltage noise goes down as the ¼ power of I_d.

The LS844 noise advantage

In order to understand the LS844's noise advantage it is helpful to briefly review the 4 major sources of noise in JFETs.

- Thermal channel noise
- Gate current shot noise
- 1/f noise
- Generation-recombination noise

The first two sources of noise are largely fundamental to the device, while the second two sources are largely the result of device imperfections. Examples of such imperfections include lattice damage and charge traps. A major reduction in G-R noise is key to the LS844's superior noise performance.

Thermal channel noise

Thermal channel noise, as discussed above, is akin to the Johnson noise of the resistance of the channel. However, it is important to recognize that the channel is not acting like a resistor in the saturation region where JFETs are usually operated. The channel is operating as a doped semiconductor whose conduction region is pinched off by surrounding depletion regions to the point where the current is self-limiting. Conduction is by majority carriers. The constant 0.67 in the equation where $r_n = 0.67/gm$ is largely empirical, can vary with the individual device geometry, and is often a bit smaller than 0.67. However, it is unusual for the constant to be less than 0.5.

Gate shot noise current

JFET input current noise results from the shot noise associated with the gate input junction leakage current. This noise is normally very small, on the order of fA per √Hz. It can usually be neglected. However, in extremely high-impedance circuits and/or at very high temperatures, this noise must be taken into account. Shot noise increases as the square root of DC current. A useful relationship is that I_{shot} = 0.57pA/√Hz/√μA [1]. Alternately, I_{shot} = 0.57fA/√Hz/√pA.

Consider a circuit with a 100MΩ source impedance and a JFET at 25°C with input noise current of 4 fA/√Hz. The resulting voltage noise will be 400 nV/√Hz. Leakage current doubles every 10°C, so at 65°C this noise contributor will be about 1600 nV/√Hz. For comparison, the Johnson noise of a resistive 100MΩ source is about 1300 nV/√Hz.

1/f noise

At very low frequencies the input noise power of a JFET rises as the inverse of frequency. That is why this noise is referred to as 1/f noise. When expressed as noise voltage, this means that the noise rises at a rate of 3dB/octave as frequency decreases. In a good JFET, the 1/f spot noise at 10Hz may be twice the spot noise at 1kHz (up 6dB) when expressed as nV/√Hz.

The noise might typically be up by 3dB at 40Hz. 1/f noise is associated with imperfections in the fabrication process, such as imperfections in the crystal lattice.[2] The improved processing of the LS844 contributes to reduced 1/f noise.

By comparison, a good JFET op amp with input noise of 10 nV/√Hz at 1kHz may have its noise up by 3dB at 100Hz and the spot noise at 10Hz might be up by 10dB. At 1Hz that op amp may have spot noise on the order of 65 nV/√Hz.

Generation-recombination noise

A less-known source of voltage noise results from carrier generation-recombination in the channel of the JFET. This is referred to as G-R noise. This *excess noise* is governed by fluctuation in the number of carriers in the channel and the lifetime of the carriers. G-R noise manifests itself as drain current noise. When referred back to the input by the transconductance of the JFET, it is expressed as a voltage noise.

Like 1/f noise, G-R noise results from process imperfections that have created crystal lattice damage or charge trap sites. In contrast, however, G-R noise is not limited to low frequencies. In fact, it is flat up to fairly high frequencies, usually well above the audio band. The G-R noise power spectral density function is described in [2] as:

$$\overline{S_{G\text{-}R(f)}}/N^2 = [(\Delta N)^2/N^2] * [4\tau/(1 + (2\pi f\tau)^2]$$

where $\overline{(\Delta N)^2}$ is the variance of the number of carriers N, and τ is the carrier lifetime.

Above a certain frequency, the G-R noise power decreases as the square of frequency. When expressed as noise voltage, this means that it decreases at 6 dB/octave. The point where the G-R noise is down 3dB can be referred to as the G-R noise corner frequency. That frequency is governed by the carrier lifetime, and in fact is equal to the frequency corresponding to a time constant that is the same as the carrier lifetime.[2] We have,

$$f_{G\text{-}R} = 1/2\pi\tau$$

where τ is the carrier lifetime. Leeman Alan

The 6 dB/octave high-frequency roll-off of G-R noise is only an approximation because there are normally numerous sites contributing to G-R noise and the associated carrier lifetimes may be different. As a result, the G-R noise corner frequency is poorly defined and the roll-off exhibits a more shallow slope than 6 dB/octave over a wider range of frequencies. The inflection in the JFET's noise vs. frequency curve may thus be somewhat indistinct. The important take-away here is that excess G-R noise can often exceed the thermal channel noise contribution and thus dominate voltage noise performance of a JFET.

JFET voltage noise spectrum and contributors

The idealized noise spectral density graph in Figure 1 illustrates how the three voltage noise contributors act to create the overall noise versus frequency curve for a JFET. In the somewhat exaggerated case illustrated, G-R noise dominates thermal channel noise.

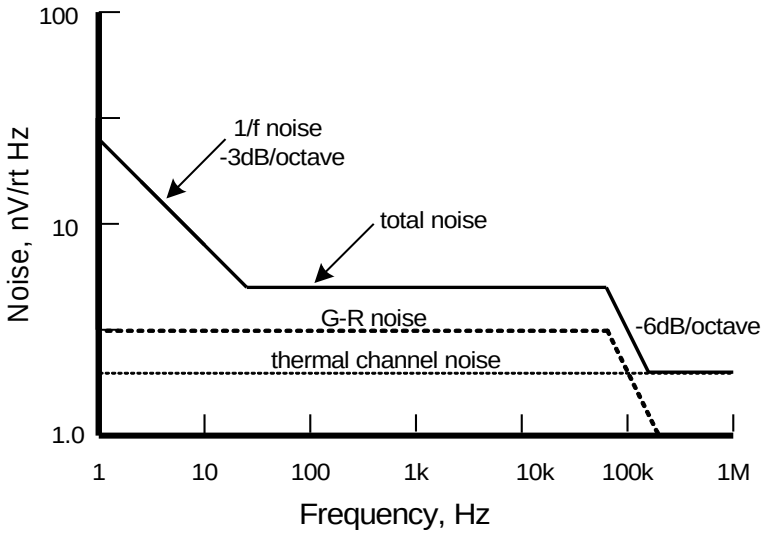

Figure 1: JFET Voltage Noise

LS844 Noise improvement

The LS844 noise advantage derives from process improvements that reduce device imperfections. Those imperfections create G-R noise and 1/f noise. Such process imperfections include crystal lattice damage and charge trap sites. Put simply, most JFETs are not as quiet as they can be. The process improvements made in the LS844 have reduced both 1/f noise and G-R noise.

The common substrate

The LS844 is a monolithic dual JFET in which the substrate is shared between the two integrated JFET devices. The two gates are isolated from the common substrate through reverse-biased substrate diodes as shown in Figure 2. The anodes of these diodes are connected to the gates while the cathodes are connected to the common substrate. The substrate is not normally accessible, and it harmlessly floats as a result.

In some applications it is important to take these isolation diodes and the common substrate into consideration. The 6-pin versions of the LS844 simply
float the substrate, while the 8-pin SOIC package brings
out the substrate for possible connection by the user. In some applications the floating substrate can be a very weak source of crosstalk between the gates. In other applications, the DC voltage to which the substrate floats may be of interest. The gate-substrate capacitance, which is a function of gate-substrate reverse bias, may influence performance in some applications. In some applications it may be useful to connect the substrate to a fixed DC voltage. Another possibility is to bootstrap the substrate with signal to yet further reduce the capacitive effects of the substrate diodes.

Limits on the operating bias voltages of the two sections of the dual JFET must be considered. This is usually not an issue when the dual JFET is employed as a differential pair, but may be an issue in some other circuit arrangements.

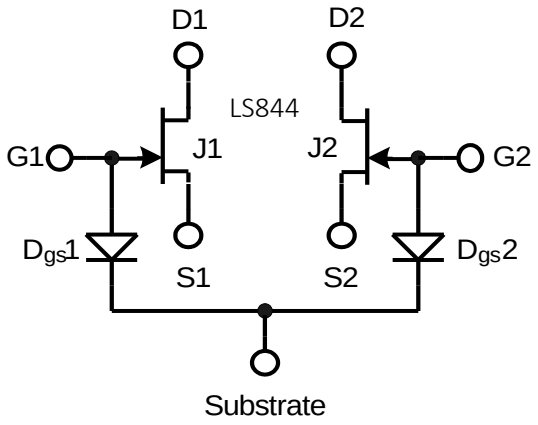

Figure 2: LS844 Common Substrate

JFET Buffers

Figure 3 shows the LS844 connected as a simple unity-gain source follower buffer. In (a) an output voltage offset equal to V_{gs} will result. If a dual JFET like the LS844 is used, the circuit in (b) can be used. J2 acts as the pull-down current source. Because of the tight matching between J1 and J2, the same V_{gs} will appear across R2 and R3, resulting in an output voltage with nearly zero offset. A circuit like this built with a randomly selected LS844 exhibited offset of only 5mV. R3 can be conveniently trimmed to adjust for zero offset. In (c) the gate bias resistor R1 has been bootstrapped to provide higher input resistance. R4 and R5 help stabilize the output voltage to near 0V. Here resistor R2 creates the same voltage offset in the gate of J2 as exists in the gate circuit of J1.

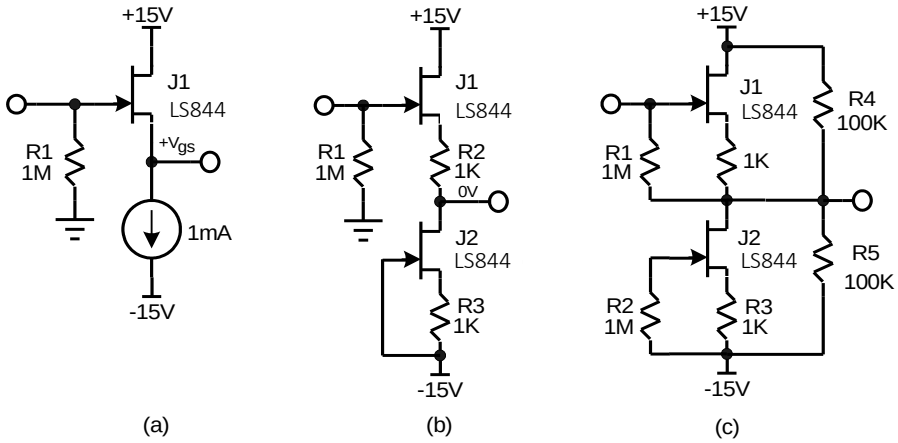

Figure 3: LS844 Source Followers

Figure 4(a) illustrates a differential buffer with low output impedance and low distortion. The key to this design is that each JFET is connected in a complementary feedback pair (CFP) configuration with a PNP transistor, greatly augmenting its effective transconductance and providing distortion-reducing local negative feedback. Notice that the PNP transistors are actually connected as a differential pair, providing additional common-mode rejection. For a given choice of R3 and R4, the value of the current sources can be chosen to make the common-mode DC offset at the output fairly small. If the current sources are controlled by common-mode feedback from the outputs, common-mode offset can be made very small.

Figure 4(b) shows how the differential JFET buffer can be used to build an audio power amplifier with very high impedance differential inputs by buffering the relatively low input impedance presented by the power amplifier connected as a differential amplifier.

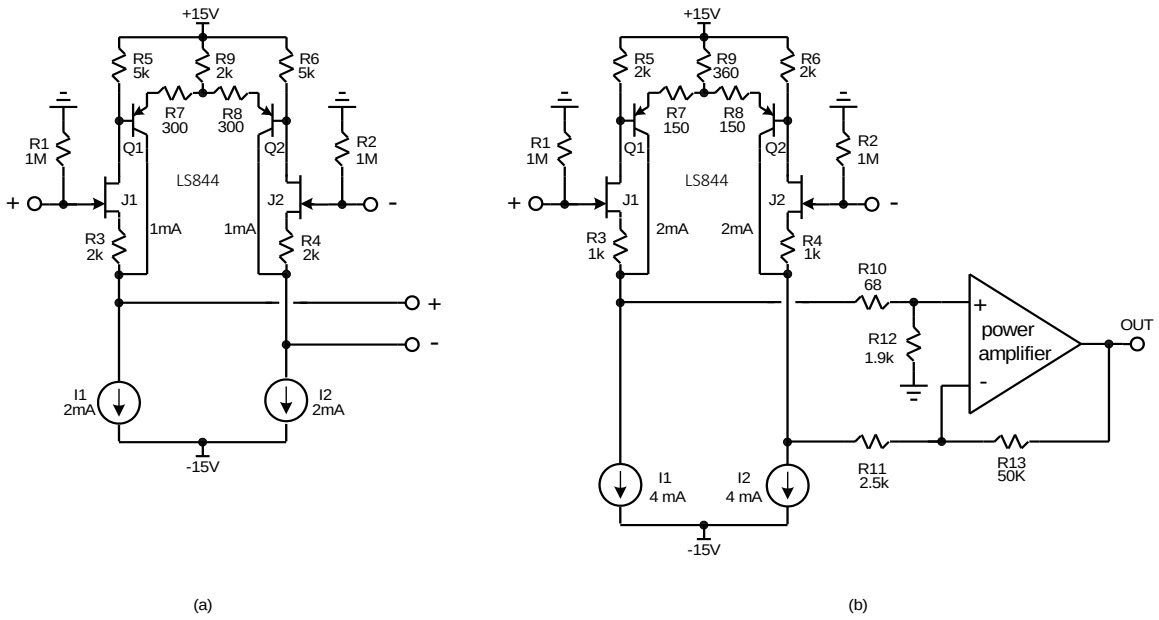

Figure 4: Differential CFP FET Buffer

JFET hybrid op amps

It is often desirable to combine the low noise and simplicity of a good BJT op amp with the high input impedance of a JFET input. IC JFET op amps offer many advantages over BJT op amps, including the absence of input bias current and input noise current. However, they inevitably have greater input voltage noise, often no better than about 8 nV/√Hz. Low-noise BJT op amps easily achieve input voltage noise levels of 2.5 nV/√Hz. It is more difficult to implement good JFETs in a bipolar IC process. For this reason it is sometimes advantageous to employ a discrete JFET input stage in front of a high-performance bipolar op amp.

Figure 5 shows several ways in which a high-impedance JFET input can be added to a BJT op amp so as to reap the advantages of both technologies. In (a) a pair of source followers is simply put in front of the op amp, eliminating the BJT input bias current and input noise current. This arrangement has the disadvantage that the input noise of the op amp adds to that of the JFETs.

In (b) a JFET differential pair with a gain of 10X is placed in front of the op amp. The gain of the JFET stage swamps out the noise contribution of the op amp and increases total open-loop gain by 20dB. If a unity-gain compensated op amp is used, the arrangement must be used with closed loop gain greater than 10 for stability. In this case, a 20dB gain stage can be made that has the same high open-loop gain as the op amp were it used by itself in a unity-gain configuration. In some cases the extra pole created at the input of the op amp may require more conservative frequency compensation.

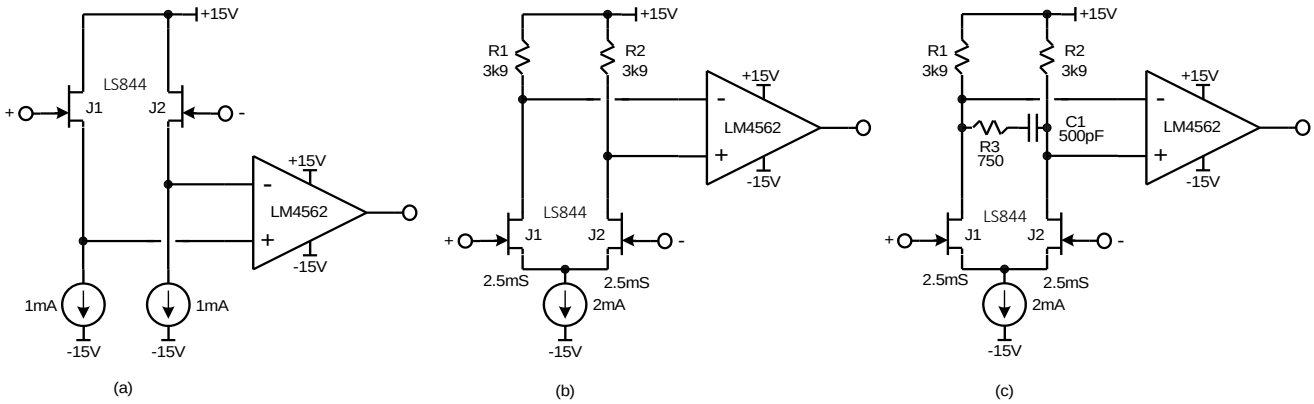

Figure 5: JFET Op Amps

In (c), a compensation arrangement is shown that allows the circuit of (b) to be configured for closed loop gain as low as unity. This is accomplished by R3 and C1, which add a pole-zero pair that decreases open-loop gain by 20dB at high frequencies well before the unity loop gain frequency is reached. The overall effect is like that of so-called two-pole compensation (TPC) sometimes used in feedback amplifiers to achieve higher loop gain at lower frequencies.

There is, however, a very important caveat with this arrangement when used at low closed-loop gain: the circuit is susceptible to latch-up. If the op amp output drives the gate of J2 to the point where it runs out of drain voltage headroom, the circuit may latch to the positive rail. Such behavior is much more likely when the feedback network provides little attenuation as in circuits with unity or low closed-loop gain.

Cascoded JFETs

Single-ended and differential JFET amplifier stages are often cascoded in order to add voltage headroom, reduce Miller effect or to increase output impedance of the stage. The cascode device can be either a BJT or another JFET. If the cascode device is a JFET, all of the signal current from the amplifying JFET passes through the cascode device(s) and no noise is added to the signal. If the cascode device is a BJT, some noise will be added as a result of base current noise flowing from the base to the cascode reference voltage. This adds noise to the signal. However, this noise must be put into perspective in comparison with the noise of the amplifying JFET. This can be evaluated by simulation. It is important that the BJT cascode transistor be a low-noise device with high beta.

Figure 6 shows some simple circuits where the amplifying JFET is cascoded. Sometimes it is necessary to cascode a JFET in order to achieve higher bandwidth by eliminating the Miller effect multiplication of the gate-drain capacitance, even in cases where C_{rss} is already low as with the LS844. Cascoding may also be necessary when higher-voltage rails are used or when it is desirable to keep the drain-source voltage of the amplifying JFETs small to minimize dissipation or noise.

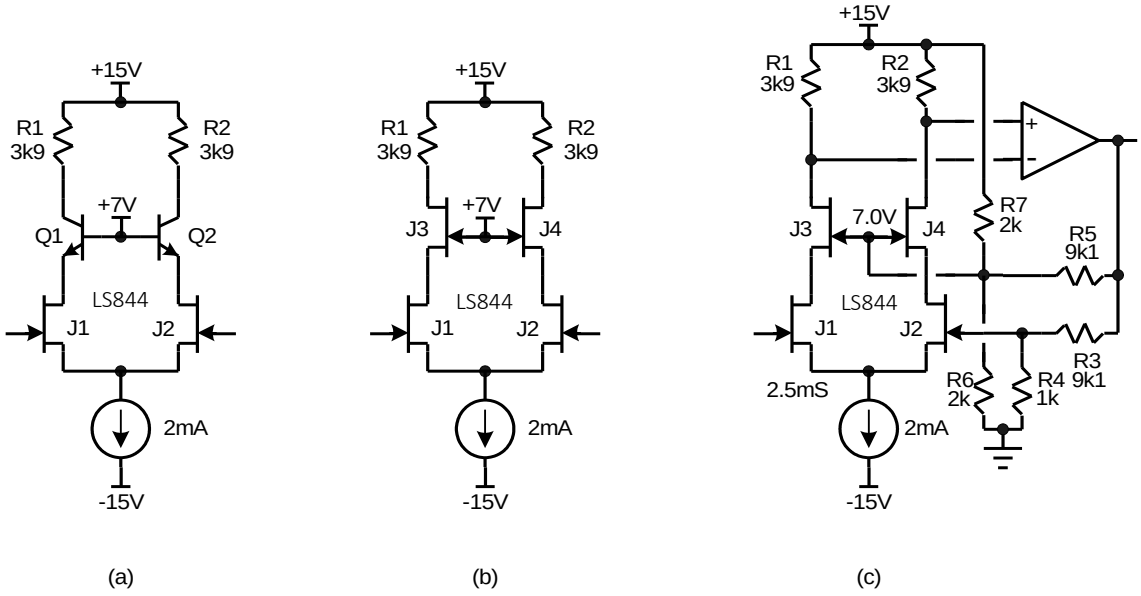

Figure 6: JFET Cascodes

Figure 6(a) shows a conventional arrangement where bipolar transistors are used for the cascade function. Some shot noise from the base current is added to the signal. In (b), JFETs are used for the cascodes, largely eliminating any noise penalty from the use of a cascode.

The circuit in (c) bootstraps the drains of J1 and J2 so as to nearly eliminate the effective input capacitance from C_{rss}. This is done by driving the gates of cascodes J3 and J4 with a replica of the feedback signal that is fed to the gate of J2. This is referred to as a *driven cascode*. Although the cascode circuits illustrated here are all differential cascodes, all of the principles and techniques apply to single-ended cascode circuits as well.

Phono preamp

The LS844 is especially attractive for use in high-performance moving magnet (MM) phono preamplifiers. It can achieve very low noise while presenting very high input impedance to the MM cartridge. The absence of input bias current in the JFET design eliminates input noise current from which BJT designs suffer. Resistance to EMI and a soft overload characteristic make the JFET choice even more attractive.

The MM cartridge source impedance rises at higher frequencies due to the resonance formed by the cartridge inductance (on the order of 300-600 mH) and the load capacitance. This resonance usually lies around 18-22kHz and can have substantial Q. At the resonance frequency, the impedance can rise to almost the nominal load resistance of 47k.

This raises the possibility of cartridge interaction with the nonlinear input capacitance of the amplifier. The low input capacitance of the LS844 JFET pair reduces cartridge interaction and high-frequency intermodulation distortion. Moving magnet cartridges are usually designed to work with a specific loading capacitance on the order of 200pF, so an input stage with capacitance on the order of 20pF, like that of an LSK389, may create a significant disturbance, especially given that the JFET input capacitance can be nonlinear.

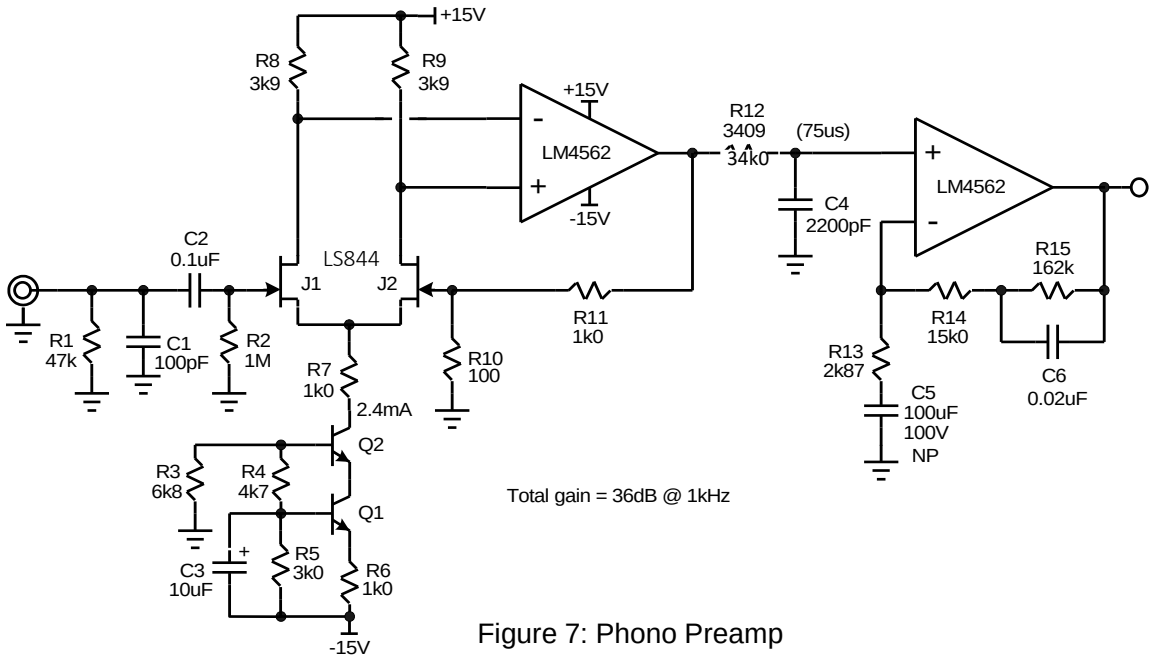

Figure 7: Phono Preamp

Figure 7 illustrates a phono preamp design that incorporates the LS844 to achieve low noise and high input impedance. The circuit consists of a hybrid JFET-bipolar op amp that uses the LS844 as its low-noise input stage. The low-distortion, low-noise LM4562 completes the hybrid operational amplifier, which is configured for a flat gain of 21dB. The 75us high-frequency corner of the RIAA equalization characteristic is implemented by R12 and C4. The remainder of the RIAA equalization implements time constants at 3180 and 318µs. It is implemented with the second half of the LM4562 op amp and the surrounding feedback network. Total gain of the preamp is 36dB at 1kHz. The LS844 JFET input stage provides exceptional immunity to EMI.

The author's VinylTrak phono preamp [3] uses a similar arrangement, but the front-end stage is a discrete 20-dB amplifier without negative feedback. That design provides a true high-impedance differential input and very soft overload characteristics. The small signal levels from a moving magnet phono cartridge allow distortion in the no-feedback arrangement to be very low.

Dynamic microphone preamp

The requirements for a dynamic microphone preamp are not unlike those of a phono preamp, since the voltage levels and source impedance are similar. Low input voltage and current noise is important. The microphone preamp does not require equalization, but it must accept a balanced input and have a very large controllable gain range. The LS844's combination of low noise and low input capacitance make it an ideal device for this application. Its strong resistance to EMI effects and its soft overload characteristics further enhance sound quality.

The LS844 front-end can be implemented as a differential amplifier without negative feedback. This provides a true high-impedance differential input with exceptionally soft overload characteristics. The input stage consists of a degenerated differential a pair of JFETs, each with a current source connected to the source. The gain of this stage is set by a variable resistance connected from source to source. Drain load resistors create a differential output that is fed to an op amp configured as a differential amplifier. In such a design, the relatively low transconductance of the JFETs limits the amount of gain that can be obtained.

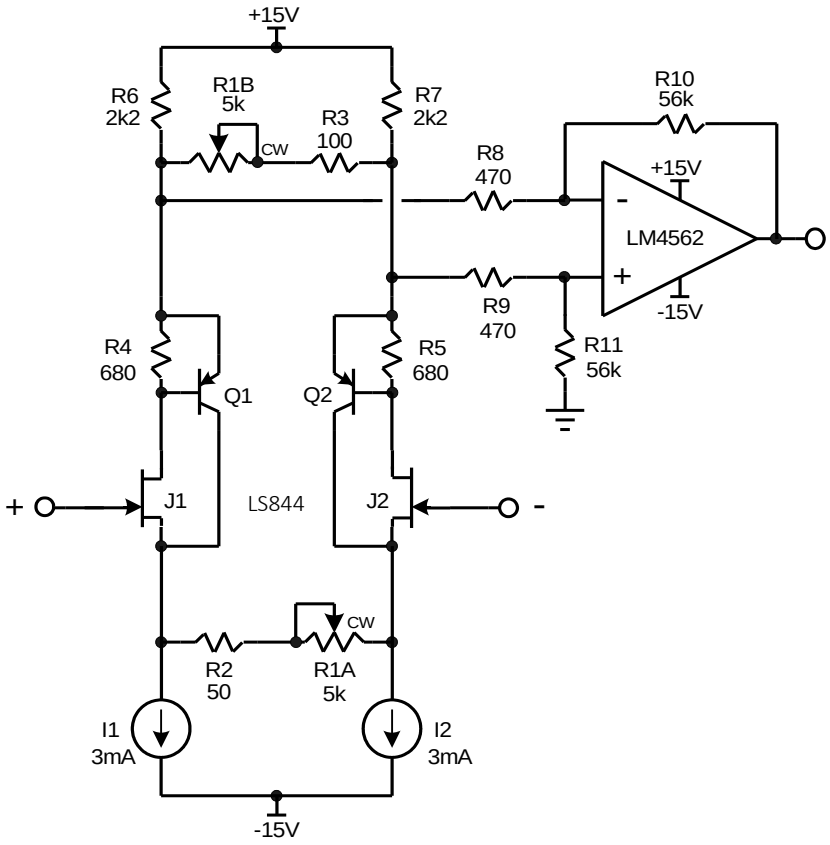

Figure 8: Dynamic Mic Preamp

An improved design is shown in Figure 8. Each JFET is configured as a complementary feedback pair (CFP) by adding a PNP transistor in the drain circuit. This arrangement increases the effective transconductance of the JFET by a factor of about 50 and provides local distortion-reducing feedback.

The JFETs are biased at 1mA and the BJTs are biased at 2mA. Gain control over a wide range is difficult to achieve with a single variable resistance in the source circuit, so a second pot ganged with the first is added in a differential shunt arrangement in the drain circuit. A gain adjustment range of 6-60dB is achieved with a single knob, and is usably distributed with respect to pot rotation even when using linear pots. The use of log-taper pots can provide an even more uniform distribution of attenuation vs. rotation.

Input noise is only 5 nV/√Hz at the highest gain setting and harmonic distortion is no more than 0.012% at an output level of 5V peak. At a nominal line level of 1V rms, THD is 0.003% at a 60dB gain setting and falls below 0.001% at gain settings less than +50dB. Even though the circuit appears differential and symmetrical, distortion is dominated by the much more benign second harmonic. This is due to the asymmetry created in the drain circuit by the differential op amp configuration. It results in different signal amplitude at the drains of J1 and J2. Distortion above the 3rd harmonic is virtually absent.

Condenser microphone preamp

The LS844's combination of low noise and low input capacitance make it an ideal device for the input stage of condenser and electret microphones.

A condenser microphone typically consists of a condenser microphone capsule and a built-in amplifier. The output of the condenser microphone is then fed to the input of a conventional dynamic microphone preamp located in the mixing console. The condenser microphone capsule comprises a diaphragm capacitor that is charged to 40-60V. It produces a voltage when the acoustic vibrations of the diaphragm change the capacitance while charge is conserved. The capacitance may be as small as 5pF but is often in the neighborhood of 50pF. The output impedance of the capsule is thus extremely high, and the microphone preamp functions mainly as a buffer, since the output voltage of the capsule is fairly high in comparison to the output voltage of a dynamic microphone.

The extremely high capacitive source impedance of the capsule means that the amplifier must present an extremely high load resistance in order to preserve low frequency response. This resistance may be on the order of 1-10 GΩ. For the same reason, the preamplifier input capacitance must be very low, especially if it is nonlinear like that of a semiconductor junction. The low input capacitance of the LS844 is an advantage here. In fact, in condenser microphone preamplifiers the drain of the JFET is usually bootstrapped with signal to further reduce the effect of C_{rss}. While most condenser microphone preamps use a single-ended JFET input stage, the differential amplifier arrangements made possible by the dual monolithic LS844 can provide lower distortion in the presence of the fairly high input voltages that can be present with a condenser microphone capsule under high SPL conditions.

The small gate input current of a JFET can come into play in circuits like a condenser microphone preamplifier. The input is AC-coupled and the gate is biased with a resistor as large as 10GΩ so as to provide extremely high input impedance. The JFET's gate input current flows into the resistor, creating a positive voltage offset. The maximum operating value of gate current for the LS844 is 25pA at 25°C (2pA typ.).

This gate input current will create an offset of +250mV. Moreover, the gate leakage current will double every 10°C. Consider a condenser microphone lying in the hot sun reaching a temperature of 45°C. Maximum gate current could reach 100pA, with a resulting input offset voltage of +1V. Such an offset can be disruptive to some circuits. Offset voltage created by gate current flowing in the very large gate return resistor can be controlled by a DC servo connected to the return end of that resistor.

The voltage gain of the preamp may often be on the order of 20dB or less. In fact, for more sensitive capsules and high sound levels, attenuation of the signal may be necessary. A useful approach to such attenuation is to employ an input pad that creates a capacitance voltage divider with an attenuation of perhaps 20dB. A 5pF capsule with a 47pF shunt capacitance will enjoy such a level of attenuation. The low noise of the LS844 means that the input attenuator can be engaged over a wider operating dynamic range. Finally, the condenser microphone electronics must be powered by so-called “phantom” powering. Only a few milliamperes are available, so low-power electronics are a must.

Piezo accelerometer charge amplifier

Figure 9 shows a Piezo accelerometer charge amplifier. In this design, the gain is set by a shunt feedback arrangement that uses capacitors instead of resistors. The gain is equal to the ratio of the transducer capacitance to the feedback capacitance C1. This amplifier incorporates an extremely high gate return resistance of 10GΩ.

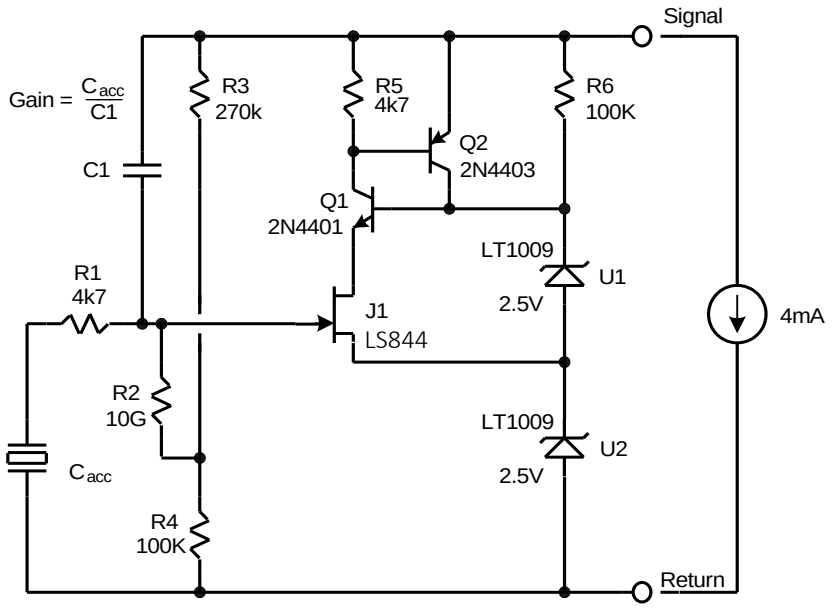

Figure 9: Piezo Accelerometer Charge Amplifier

Discrete JFET amplifier

Figure 10 shoes a discrete JFET amplifier that employs a folded cascode and a diamond buffer output stage. This is much like the low-noise discrete input stage of the author's VinylTrak phono preamplifier [3]. As shown the amplifier is operated open-loop at a gain of about 10, as determined by shunt resistor R14. The amplifier in this configuration offers a true balanced high-impedance

input, exceptional resistance to EMI and a very soft overload characteristic.

The amplifier can also be used as an operational amplifier with fairly high open-loop gain if R14 is removed and suitable feedback compensation is added. In any configuration, the use of the folded cascode architecture offers wide bandwidth.

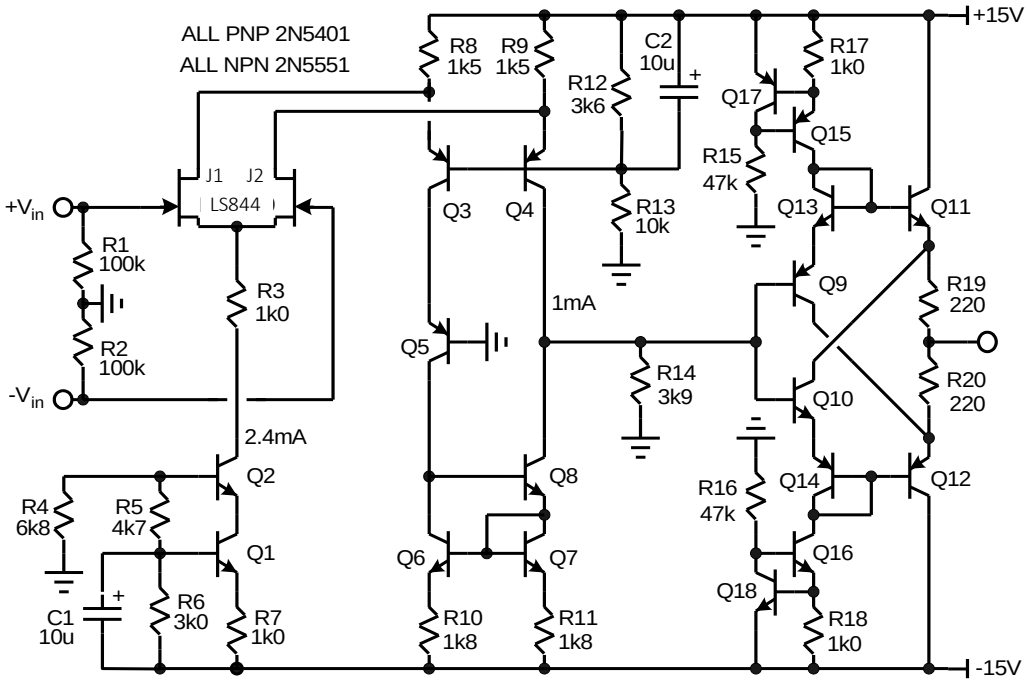

Figure 10: JFET Discrete Amplifier

Power amplifier with JFET input

The input stage for an audio power amplifier is often a long-tailed differential pair (LTP) implemented with bipolar transistors. Dual JFETs like the LS844 provide a better alternative. Many believe that the sound is better, possibly due to its much softer overload characteristic. Others believe that its superior resistance to EMI is important. The absence of input bias current for the JFET often has advantages in DC offset control and selection of input stage operating impedances.

While the noise characteristics of a power amplifier are often not as critical as those of a preamp, it is still important to achieve low noise because there is no volume control in the power amplifier to reduce noise from the input stage under normal listening conditions. This is particularly so when the amplifiers are used with high-efficiency loudspeakers. For this reason the use of a low-noise JFET like the LS844 is desirable.

Figure 11 shows a simple100 watt audio power amplifier with a JFET input stage incorporating an LS844 differential pair. Input noise is only 6 nV/√Hz. The 60V breakdown of the LS844 allows the use of a JFET input without a cascode for amplifiers with nominal rail voltages of up to 50V, assuming that the rail voltages do not exceed 60V under worst case light-loading and high mains voltage conditions.

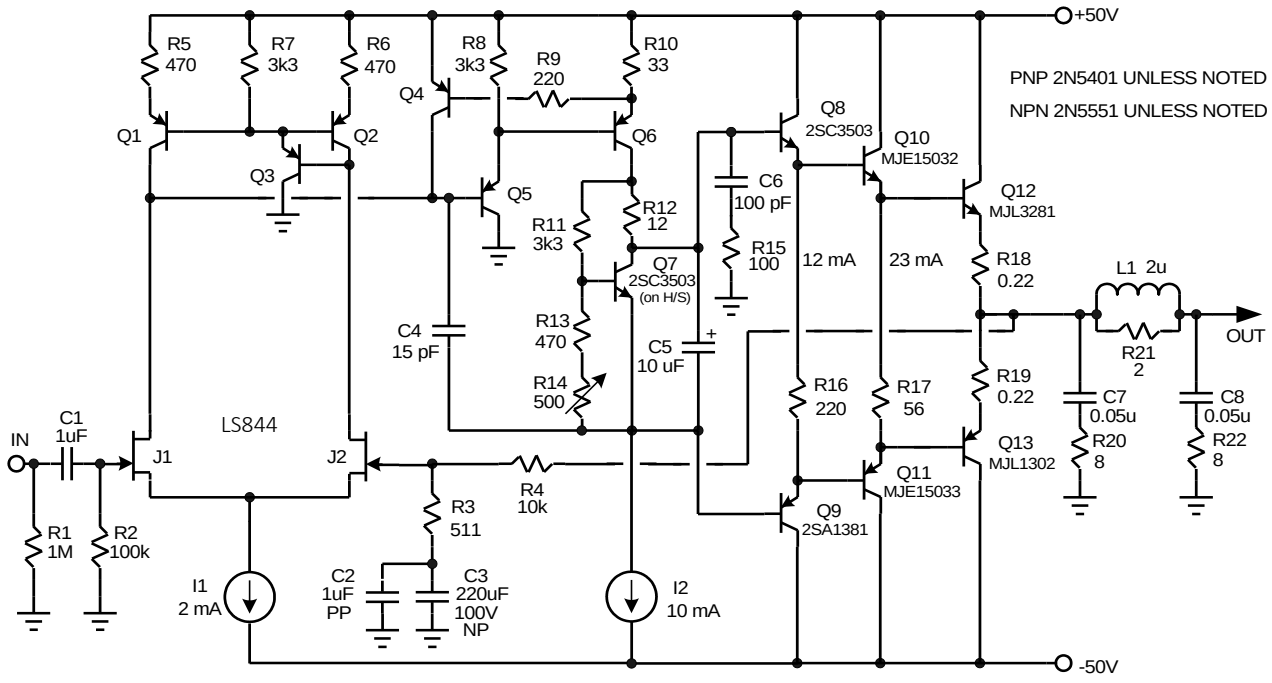

Figure 11: Power Amplifier

Assuming that the rail voltages do not fall to under 45V under full power into an 8Ω load, the amplifier is capable of output power in excess of 100 watts into 8 ohms (corresponding to a peak output voltage of 40V). For simplicity, details of the current sources and output protection circuits are not shown. The design of audio power amplifiers like this can be found in the book *Designing Audio Power Amplifiers*, written by the author. Useful information can also be found on the author's web page at www.cordellaudio.com [4].

Conclusion

With its low noise, low input capacitance and tight matching, the LS844 is ideal for numerous audio and instrumentation applications. Its low capacitance also make it a good candidate for many high-frequency circuits.

References

[1]. Designing Audio Power Amplifiers, Bob Cordell, McGraw-Hill, 2010.

[2]. Alicja Konczakowska and Bogdan M. Wilamowski, *Noise in Semiconductor Devices*, Chapter 11 in *Industrial Electronics Handbook*, vol. 1, *Fundamentals of Industrial Electronics*, 2nd edition, CRC Press 2011.

[3]. Bob Cordell, *VinylTrak – A full-featured MM/MC phono preamp*, Linear Audio, vol. 4, September 2012, www.linearaudio.net.

[4]. Web site www.cordellaudio.com.

LINEAR SYSTEMS

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COMPARISON OF IMPORTANT DESIGN SPECS FOR JFETS USED IN SMALL SIGNAL APPLICATIONS

Junction field effect transistors (JFETs) are used and are useful in many different circuit topologies. Because these devices function as voltage controlled current sources (VCCS) as opposed to current controlled current sources (CCCS), they offer designers certain flexibilities in designs not available when using bipolar transistors (which are CCCS devices). JFETs can also be used as voltage controlled variable resistors and voltage-controlled switches. JFETs have extremely high input impedances (on the order of giga-ohms) and extremely low input leakage currents (on the order of pico-amps). Selected parts are designed to have excellent performance in high and very high frequency (VHF) circuits.

Parameters to consider:

When designing with JFETs, the design engineer must consider the various device parameters. The most commonly used parameters are:

- V_{GSS} – breakdown voltage of the gate-to-source [diode] junction;
- I_{DSS} – drain to source saturation current at some specified drain to source voltage (V_{DS}) and gate voltage (V_{GS}); V_{GS} is usually set to 0.0 V – i.e., gate is connected to source;
- $V_{GS(OFF)}$ – gate-to-source voltage that causes virtually no current flows from drain to source; conduction channel is "pinched off" – sometimes referred to as pinch-off voltage;
- V_{GS} – gate to source operating voltage; the gate-to-source voltage needed to get some specified drain current to flow with some specified V_{DS};
- I_{GSS} – the current flow through the gate-to-source diode when it is reverse biased; measured at some specific reverse voltage and with a specified V_{DS};
- G_{fs} – transconductance – the ratio of the [output] drain current to the [input] gate voltage; stated as amps per volt, the reciprocal of ohms – measured in Siemens and measured at some specified V_{DS}, I_D, and frequency;
- e_n – voltage noise spectral density measured at some specific V_{DS}, I_D, frequency, and noise bandwidth; units of measurement are noise voltage-per-root hertz, typically written as (e.g.) nV/√Hz;
- C_{ISS} – common source input capacitance; useful in circuits operating at high audio frequencies and beyond;
- C_{RSS} – common source reverse transfer capacitance; again, useful in the higher frequency circuits;
- $R_{DS(on)}$ – on resistance, drain to source; measured at some specific V_{DS}, I_D, and frequency; generally, only specified for devices intended for use as voltage variable resistors or voltage-controlled switches.

For any design, whether audio frequency, radio frequency (RF), signal switching, signal attenuation, amplification, or signal shaping, the design engineer must trade off between parameters. There are no perfect devices; the engineer must decide on whether, for example, e_n or I_{DSS} or G_{fs} or V_{GS} is the driving force in a design. In addition to these considerations, when gain stages are configured as differential amplifier pairs, it is necessary to carefully match the two transistors used in each differential pair. Specifically, attention must be paid to the matching of characteristics such as differential $V_{GS(OFF)}$, V_{GS}, I_{DSS}, G_{fs}, C_{ISS}, and C_{RSS}. A further complication arises if the temperature coefficients (tempco) of the devices don't track. The degree of matching of all these parameters in dual devices predominantly affects common mode rejection ratio (CMRR) and offset voltage.

The best way to mitigate these mismatch problems is to use dual JFETs constructed on the same chip (i.e., monolithic JFET pairs). These inherently have very tight parameter matching and tracking. Examples of such parts are our LSK389, LSK489, and LSJ689. Besides the excellent matching, these parts are among the lowest noise parts available. A careful search for low noise JFETs *may* turn up lower noise devices, but none with a good mix of low noise, low I_{DSS}, well matched parameters, and monolithic construction.

Further consideration of low noise device applications:

Low noise amplifier circuits can be implemented by selecting JFETs with very low e_n. The combination of low noise and extremely high input impedance make them the perfect choice in pre-amp and frequency shaping circuitry for:

- high-end audio devices such as dynamic, ribbon (capacitive), or electret microphones;
- high-end audio devices such as moving coil/moving magnet phono cartridges;
- industrial transducers such as inductive pickups, accelerometers, or piezo vibration sensors;
- scientific sensor pre-amps such as those used with electrometers, photo-diodes, photo-multiplier tubes, or Geiger-Müller radiation detector tubes;
- bio-medical sensor pre-amps used in blood pressure, blood oxygen level, respiration rate, galvanic skin response, EKG, and ECG measurements.

A careful design can produce an e_n of 0.7nV/√Hz. More detailed applications information regarding designing for low noise can be found in three of our applications notes: LSK389 Application Note, LSK489 Application Note, and LSJ689 Application Note.

The extremely high input impedances and extremely low input leakage currents cited above are two of the more important parameters of JFETs when used in scientific sensor applications (again, electrometers, photo sensors, or Geiger-Müller tubes).

Further information on general JFET designs can be found in the LSK389 Application Note cited above along with an app-note originally published by Siliconix, AN102, JFET Biasing Techniques.

Low or ultra-low power applications:

Low power-draw topologies are easily implemented by selecting JFETs with an I_{DSS} of 2 to 6 mA and low $V_{GS(OFF)}$. These will prove useful in circuitry used in portable equipment that is powered from batteries. Another low power class of devices uses power scavenged from the surrounding environment. This includes (but is not limited to):

- equipment powered from light sources using solar/photo-voltaic cells;
- equipment powered from heat using thermocouples/thermopiles;
- equipment powered from mechanical motion/vibration using piezo-ceramic elements;
- equipment powered from mechanical motion such as ocean waves or wind using electromechanical generators;

- equipment powered from ambient RF or magnetically coupled energy.

Low power amplifier and oscillator examples:

Two examples of JFET amplifier circuitry are taken from the LSK489 Application Note previously cited and reproduced below in Figure 1. On the left, the matched pair (LSK489) is a low current draw (2 mA) differential source follower that buffers the input to an op-amp. By selecting a low power op-amp, overall power draw can be quite low. On the right, the differential pair is reconfigured as a drain follower which not only buffers but also adds significant voltage gain.

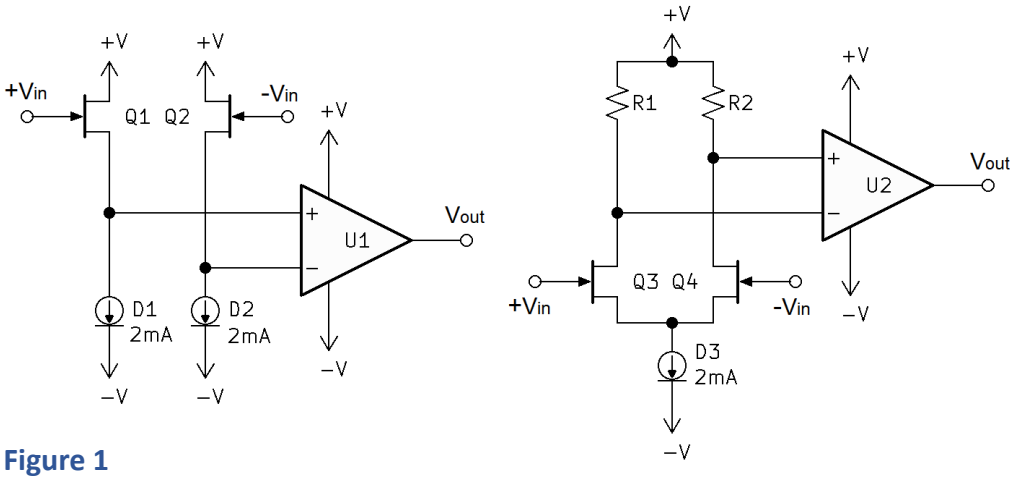

Figure 1

An example of a stand-alone JFET amplifier stage, again taken from the LSK489 Application Note, is shown in Figure 2. As configured, current draw is 4 mA.

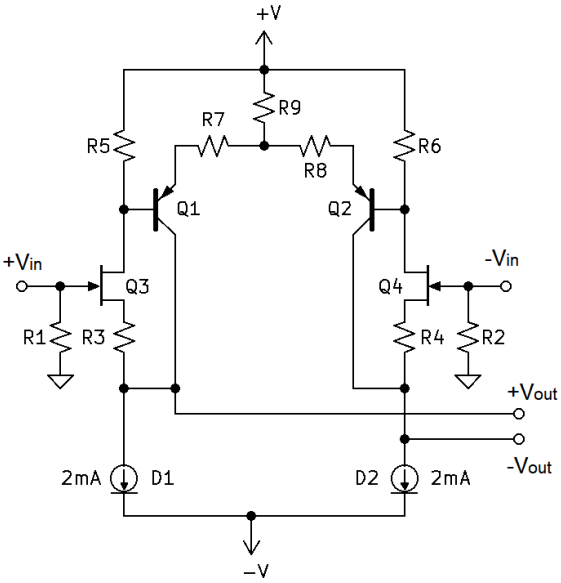

Figure 2

Two examples of ultra-low power oscillators are shown in Figures 3a and 3b, both built with one JFET (our LSK170A). Figure 3a is a Hartley oscillator. C2 and C3 are coupling and power supply bypass capacitors (respectively); as such, typical values can be 0.1 uF. A typical value for R1 is 1.0 Meg-Ω. C1 and L1 are selected to parallel resonate at the desired frequency of operation which can be from audio frequencies to VHF. A prototype circuit using a selected LSK170A, a J. W. Miller B5496C tapped coil, and a 10pF capacitor for C1 worked with a supply voltage of 105 mVDC and a current draw of 166 uA. Resonant frequency was 4 MHz.

Figure 3b is an Armstrong oscillator. C4, C5, and R2 are functionally equivalent to C3, C2, and R1 above. T1 is a Toko RAN 10A 6845 RF coupling transformer with a 1:40 voltage turns ratio (measured at 100kHz). A prototype circuit using a selected LSK170A oscillated at 860 kHz with a supply voltage of 20 mV and current draw of 86 uA.

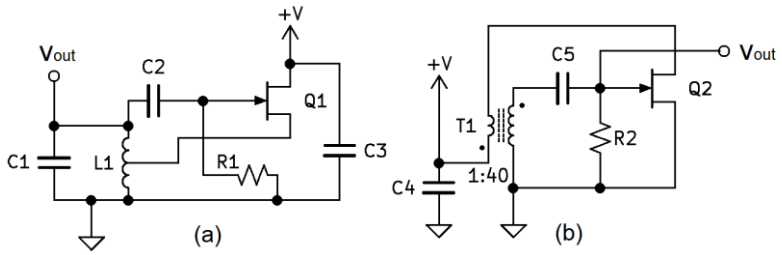

Figure 3

Voltage controlled attenuators or switches:

While all JFETs can be used as voltage controlled variable resistors, certain JFETs are manufactured and characterized for this specific application. They are typically used with no DC voltage applied from drain to source and instead have just an AC signal applied (capacitively coupled). Varying the voltage at the gate with respect to the source varies the drain to source resistance.

An example circuit using a P-channel JFET (Linear Systems LS26VPS) as part of a simple two-resistor voltage divider is shown in Figure 4. R1 is the upper resistor and Q1's drain to source resistance is the lower resistor. A signal applied at the Vin terminal will be attenuated and appear at the Vout terminal. An increasingly positive voltage applied to V_{CNTL} increases the drain to source resistance and reduces the attenuation factor. This circuit can be used as an adjustable attenuator or a voltage-controlled switch.

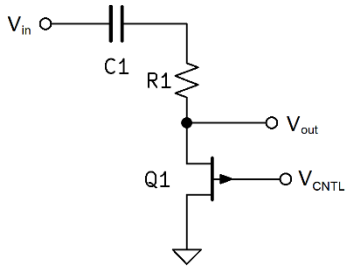

Figure 4

More detailed applications information can be found in our applications note A Guide to Using FETs for Voltage Controlled Circuits.

RF or VHF applications:

In most high frequency amplifier circuits, rather than using a broadband amplifier as is used in low frequency audio and servo circuits, tank (L-C) circuits are added to the input and output ports of the amplifier stage and are tuned to specific frequencies. Such a stage is referred to as a tuned gate/tuned drain amplifier. It has very high input impedance and can provide frequency-selective high gain. A simplified example is shown in Figure 5.

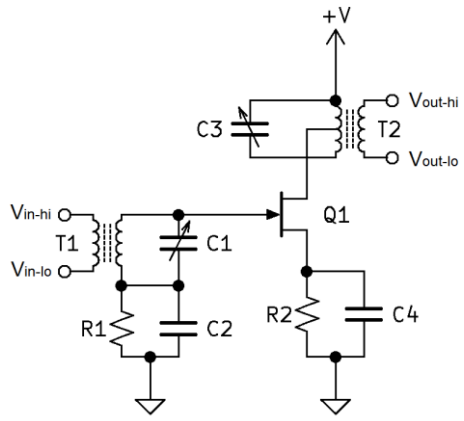

Figure 5

A variation on this circuit is the tuned source/tuned drain common gate amplifier shown in Figure 6. It has relatively low input impedance. In some applications, this circuit has higher stability (lower likelihood to exhibit parasitic oscillation).

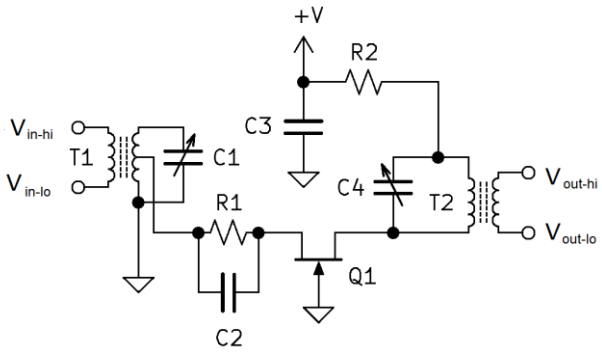

Figure 6

When oscillations *are* desired and frequency accuracy is important a crystal-controlled oscillator is needed. Figure 7 shows a Pierce oscillator.

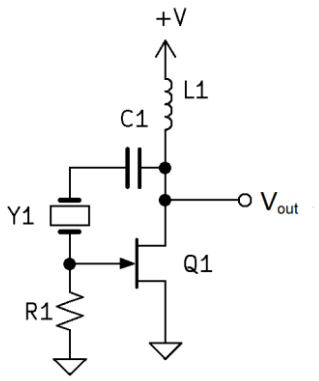

Figure 7

Switch-mode power supply application:

The circuit in Figure 8 shows a variation on an Armstrong oscillator seen in Figure 3b, above. With this circuit, when first powered, the load remains disconnected. Once the oscillations have risen to a sufficiently high level, i.e., when the rectified voltage at C2 rises above the gate threshold voltage of the P-channel enhancement mode MOSFET Q2, it turns on and provides current to the load.

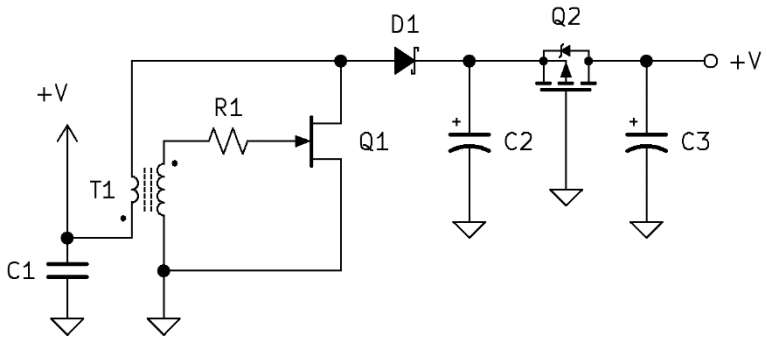

Figure 8

For a more detailed look at switch-mode power supplies that can operate on extremely low voltages, see the Analog Devices App Note by Jim Williams, J-FET-Based DC/DC Converter Starts and Runs from 300mV Supply.

Conclusion:

General purpose amplifier topologies – the pre-amp and level-shifting stages of power and servo-amplifiers – and high frequency (RF) amplifiers benefit from the use of JFETs. Further, in demanding low and ultra-low power applications, JFETs are unequaled in their superior performance.

LINEAR SYSTEMS

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A GUIDE TO USING FETs FOR SENSOR APPLICATIONS

By Ron Quan

Linear Systems provides a variety of FETs (Field Effect Transistors) suitable for use in low noise amplifier applications for photo diodes, accelerometers, transducers, and other types of sensors.

In particular, low noise JFETs exhibit low input gate currents that are desirable when working with high impedance devices at the input or with high value feedback resistors (e.g., ≥1MΩ). Operational amplifiers (op amps) with bipolar transistor input stages have much higher input noise currents than FETs.

In general, many op amps have a combination of higher noise and input capacitance when compared to some discrete FETs. For example, a typical FET input op amp may have input capacitances of about 20 pF, whereas many discrete FETs have input capacitances of less than 5 pF. Also, there are few low noise FET input op amps that have equivalent input noise voltages density of less than 4 nV/$\sqrt{Hz}$. However, there are a number of discrete FETs rated at ≤ 2 nV/$\sqrt{Hz}$ in terms of equivalent Input noise voltage density.

For those op amps that are rated as low noise, normally the input stages use bipolar transistors that generate much greater noise currents at the input terminals than FETs. These noise currents flowing into high impedances form added (random) noise voltages that are often much greater than the equivalent input noise.

One advantage of using discrete FETs is that an op amp that is not rated as low noise in terms of input current can be converted into an amplifier with low input current noise. For example, see the circuit shown in Figure 1.

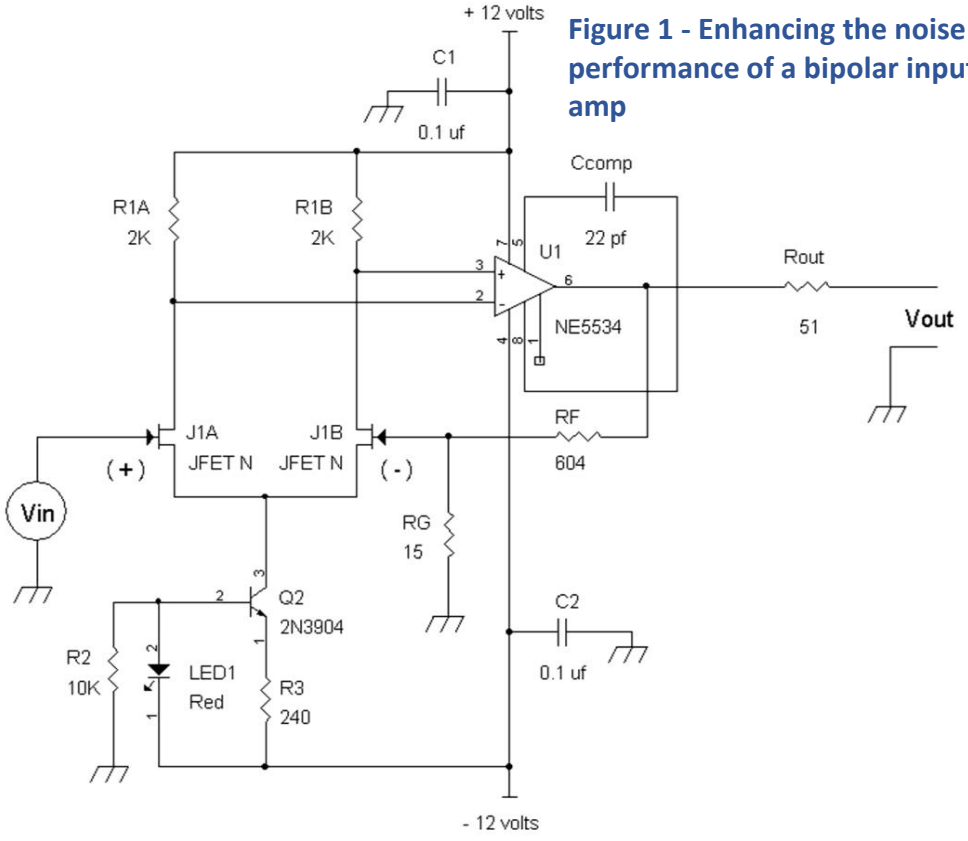


Figure 1 - Enhancing the noise performance of a bipolar input stage op amp

In Figure 1 on the previous page, current source Q2, JFETs J1A and J1B with load resistors R1A and R1B form a preamp to the input of U1 to provide better noise performance in terms of input bias current noise and equivalent input noise voltage.

The collector current of Q2 is approximately 1 volt across R3 or about 4 mA. The drain currents of J1A and J1B are equal when Vin = 0, or about 2 mA each. With the load resistors set at 2KΩ, there are about 4 volts DC across each of these resistors. The typical transconductance, g_m, for an LSK489 matched dual JFET is about 3 mS = 3 mmho at 2 mA drain current. Thus, the differential mode gain from the gates of J1A and J1B to the drains of J1A and J1B will be approximately 3 mS x 2KΩ = 6.

Note: 1 mho = 1 S = 1 amp/volt, and 1 mmho = 1 mS = 1 ma/volt.

Although an NE5534 op amp has about 4 nV per root Hertz in terms of equivalent noise voltage density, its input bias noise current in the order of 0.60 pA per root Hertz.

The DC gate current of a JFET will typically be less than 0.1 nA, and the input noise current will be:

$\sqrt{2qIg\ B}$ = noise current from the gate of the JFET

Ig = gate bias current
q = electron charge = 1.6 x 10^{-19} coulomb
B = bandwidth in Hertz. For a noise density calculation, the bandwidth is 1 Hz. Thus, B = 1.

For 0.1 nA = Ig.

$\sqrt{2qIg\ B}$ = 0.00566 pA/$\sqrt{Hz}$ = noise density current from the gate of the JFET.

In comparison to 0.60 pA/$\sqrt{Hz}$ for the input noise density current for the NE5534, the JFET has about 100 times lower input noise current at 0.00566 pA/$\sqrt{Hz}$. The LSK489 has 1.8 nV/$\sqrt{Hz}$ of noise voltage density per FET.

For J1A and J1B to be a dual matched JFET transistor such as the LSK489, the equivalent input noise voltage will be about 2.54 nV per root Hertz, or about 3.925 dB lower noise than the 4 nV/$\sqrt{Hz}$ rating of the NE5534.

Alternatively, even lower noise can be achieved by using an LSK389B for J1A and J1B, which will result in an equivalent input noise voltage of 1.27 nV/$\sqrt{Hz}$. The LSK389B has typically 0.9 nV/$\sqrt{Hz}$ per FET.

One should note that the added JFET front circuit (J1A and J1B) will increase the gain bandwidth product of the amplifier by the gain of the FET circuit. For example, at 2 mA per JFET, the tranconductance of the LSK489 is typically 3 mmho or 3 mS. With the 2KΩ load resistors, R1A and R1B, the differential mode gain is about 6.

Thus, the 10 MHz gain bandwidth product of the NE5534 is increased to 60 MHz (6 x 10 MHz = 60 MHz). Note the feedback resistors, RF and RG, are set for a gain ≥ 6 to ensure stability in the amplifier without oscillation. That is, (RF/RG) ≥ 5 since the gain is [1 + (RF/RG)].

The tranconductance of the LSK389B is about 3 times more than the LSK489. Thus, if the LSK389 is used in Figure 1, (RF/RG) ≥ 20 to ensure stability without oscillation.

Another way to reduce input bias current noise is shown in Figure 2 via source followers.

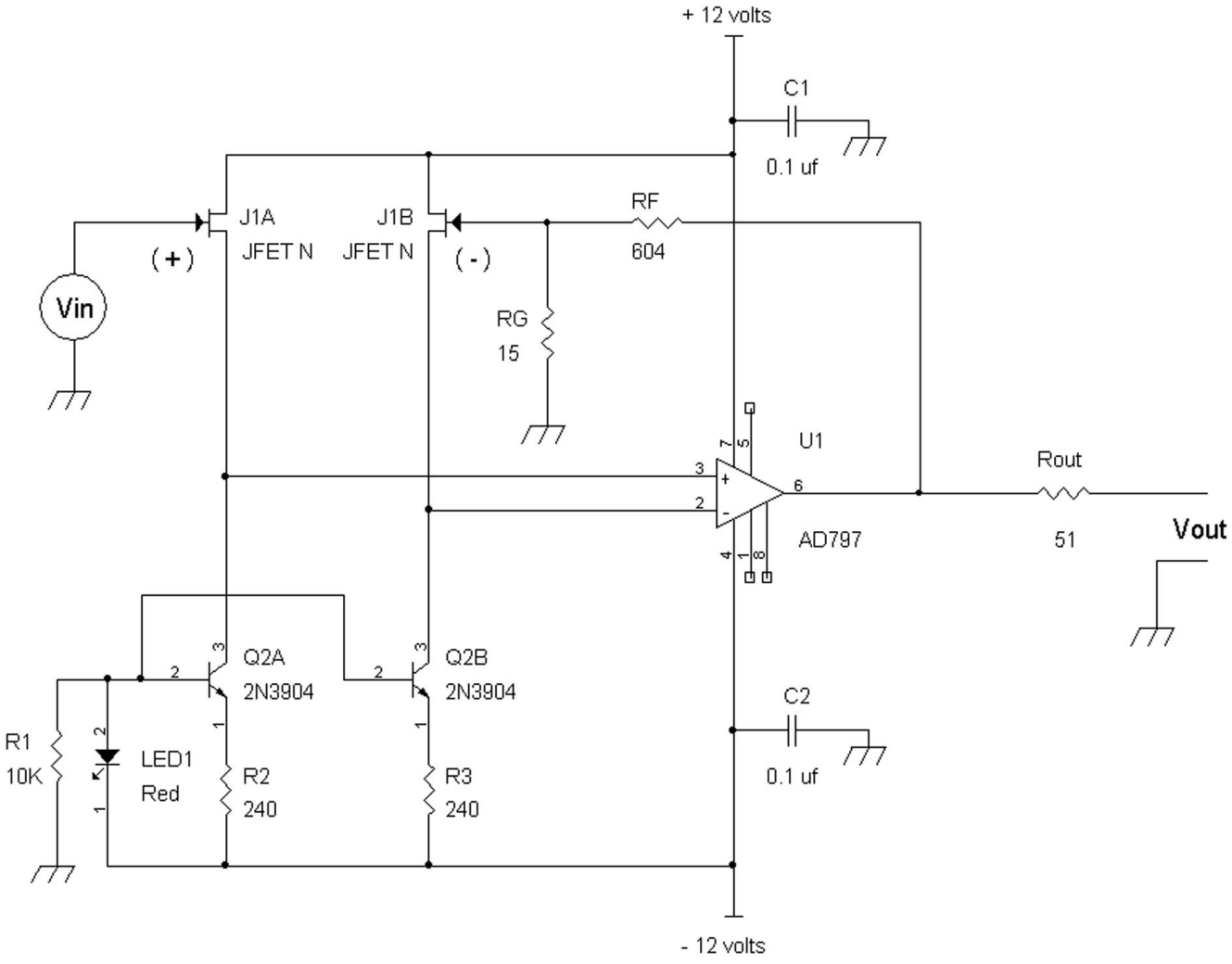


Figure 2 - An amplifier with a differential pair source follower to reduce input bias current noise

In Figure 2 above, FETs, J1A and J1B, are configured as source followers to the inputs of an op amp such as a low noise type, AD797 (or LT1028).

In terms of equivalent input voltage noise the AD797 and LT1028 are rated at about 0.9 nV/$\sqrt{Hz}$. However, their input noise currents are in the order of 1.0 pA/$\sqrt{Hz}$.

By using the source followers as shown, the input noise currents are reduced to about 0.00566 pA/$\sqrt{Hz}$.

For low input capacitance operation (< 3 pF), J1A and J1B can be a matched pair LSK489.

This will result in an equivalent input noise voltage of 2.7 nV/$\sqrt{Hz}$ with an LSK489. If slightly higher input capacitance is tolerated (< 5 pF), then an LSK389B is used for an equivalent input noise voltage of 1.55 nV/$\sqrt{Hz}$.

Q2A and Q2B should be a matched pair of NPN transistors to ensure equal source currents for J1A and J1B. However, often purchasing discrete transistors on tape provides very close DC matching in terms of base to emitter turn on voltage.

Specific Applications

Piezoelectric Element Preamps

One of the common types of sensors today is based on the piezoelectric effect. These types of sensors include accelerometers and hydrophone transducers.

The basic piezoelectric device is modeled at the bottom of the page.

Figure 3(a): Charge model of piezo device.

Figure 3(b): Equivalent voltage model.

In Figure 3(a), a piezoelectric device delivers charge instead of current. The charge, Qpiezo, flows into a capacitor, Cpiezo, to develop a voltage. Recall that:

Qpiezo = Cpiezo x Vpiezo, or expressed another way via algebra:

Vpiezo = Qpiezo/Cpiezo (where Vpiezo is the voltage across the capacitor Cpiezo)

As shown in Figure 3(a), there is also a resistor, Rpiezo, in parallel with the charge generator and capacitor. Rpiezo has a very high resistance, usually very close to an open circuit. For example, the measured DC resistance across a piezoelectric earphone/microphone is > 2000 MΩ.

However, it may be easier to look at a piezoelectric device as a voltage generator. By equivalently converting the charge source, Qpiezo, and capacitor, Cpiezo into a “Thevenin” voltage source and series impedance, we have the model as shown in Figure 3(b).

From Figure 3(b) we see that the piezoelectric device provides an AC coupled signal and it cannot provide a sustained DC voltage across Rpiezo.

Figure 3(a) - Charge model of piezo device

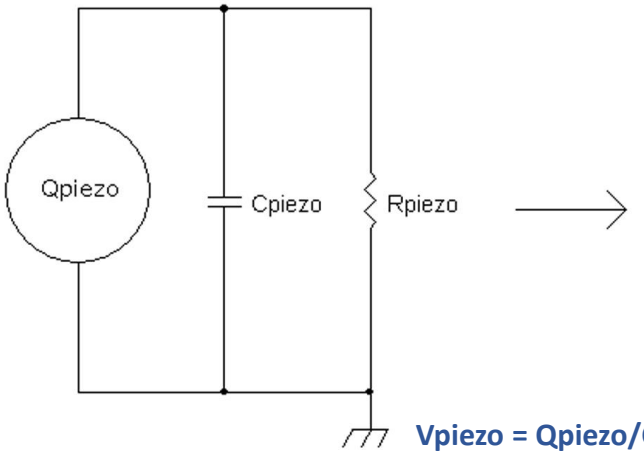
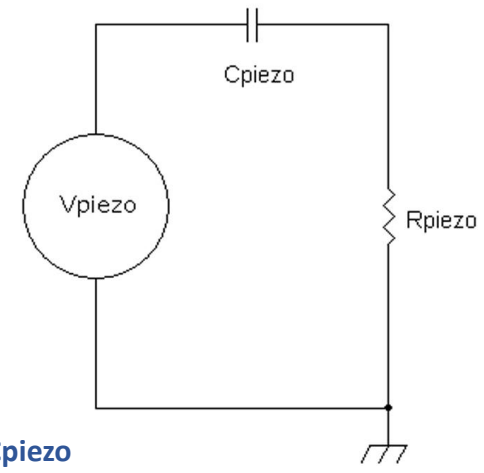


Figure 3(b) - Equivalent voltage model



Vpiezo = Qpiezo/Cpiezo

From Figure 3(b), we see that the low frequency cut-off response is dependent on the values of Cpiezo and Rpiezo. In practice for the most extended low frequency response, we need Cpiezo to load into a very high resistance value.

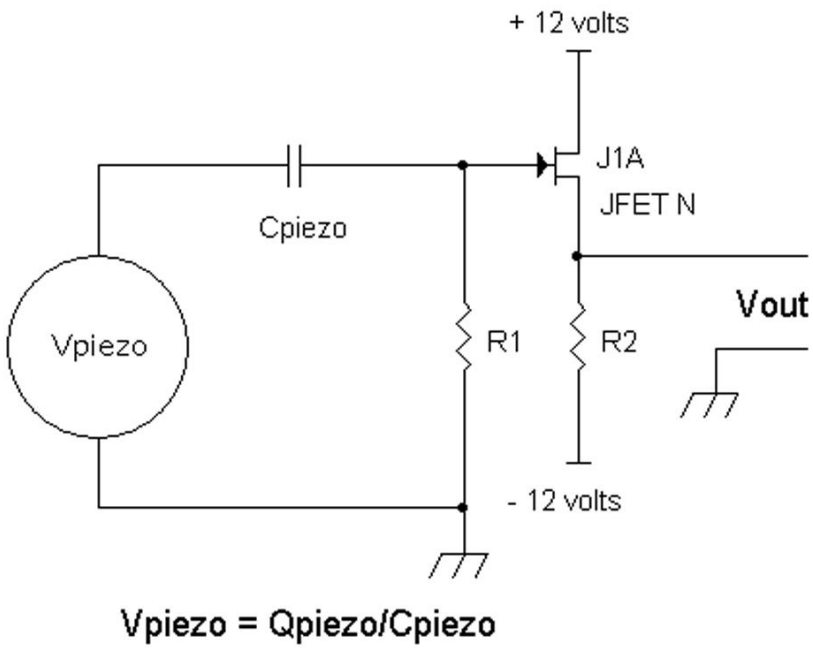
For simplicity, let's take a look at a simple FET buffer amplifier in Figure 4 at the bottom of the page.

Figure 4 A piezo device connected to a simple JFET source follower amplifier.

Generally, R1 can be in the range of 1MΩ to 10MΩ. However, it is not uncommon to have R1 in the order of 100MΩ to 1000MΩ. Source resistor R2 is set to bias the source to a DC bias current from about 100 µA to 5 mA or R2 can be in the range of 100KΩ to 2KΩ. J1A can be an LSK170 JFET. The drain of J1 is connected to a plus supply voltage and the source provides a signal voltage, Vout with a medium to low impedance output resistance that is able to drive another amplifier. Note that Vout may be connected in series to an AC coupling capacitor to remove the DC voltage at the source of J1A.

Another way to amplify the signal from a piezo device is shown in Figure 5 on the next page. For simplicity, we will ignore the effect of Rpiezo, which is close to infinite resistance.

Figure 4 - A piezo device connected to a simple JFET source follower amplifier



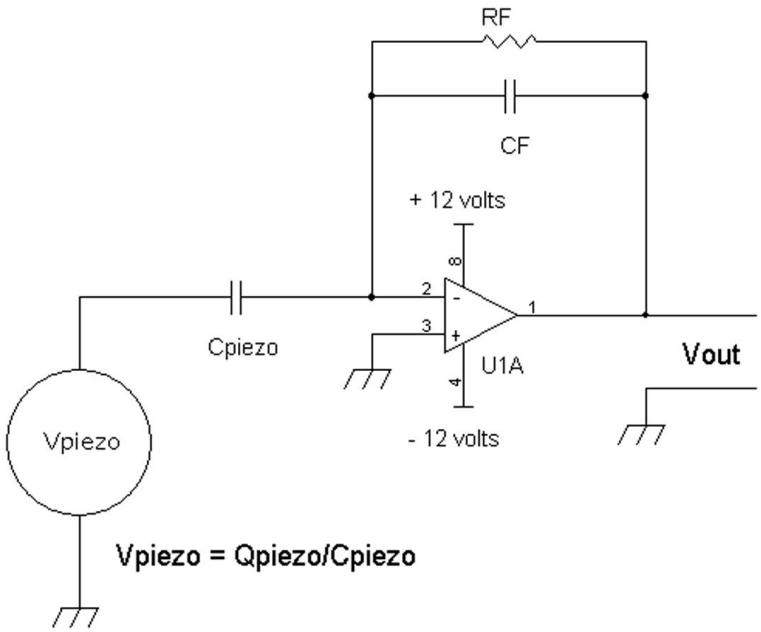


Figure 5 - Charge amplifier with integrating capacitor CF

If we ignore the feedback resistor, RF, for now, then we see that the gain is:

Vout/Vpiezo = - ZCF/ZCpiezo

Where ZCF and ZCpiezo are the impedances for CF and Cpiezo

Vout/Vpiezo = - ZCF/ZCpiezo = - [1/jωCF]/[1/jωCpiezo] = - Cpiezo/CF

Since Cpiezo is fixed and is internal to the piezo device, the gain is changed by setting the value of CF. For example, the smaller the value of CF, the larger the gain.

Ideally, CF should work as an integrating capacitor. However, to prevent Vout from latching to the supply rails, RF is connected in parallel to CF provide a DC path from the output of U1A to the (-) input of the op amp. Resistor RF also provides a discharge path for CF.

It may be “counter intuitive” but RF actually works as a high pass filter and sets the low cut-off frequency. To see how this happens, let’s suppose RF = 1MΩ and CF = 1000 pF. At 10 Hz, the magnitude of the ZCF ~ 16M. Since CF is in parallel with RF, we see that RF at 1MΩ dominates ZCF||RF at 10 Hz. At low frequencies, we can then “ignore” CF and now see that Figure 5 looks like a differentiator circuit (imagine removing CF from the schematic) with Cpiezo as the input capacitor and RF as the feedback resistor. Now note that a differentiator circuit has a high pass filtering effect.

When the AC gain is calculated for magnitude versus frequency, the – 3 dB cut-off frequency for the high pass filter effect is 1/2π(RF)(CF), and the gain is Vout/Vpiezo = Cpiezo/CF.

As an example, consider the model 765M25 dynamic pressure sensor from Columbia Research Laboratories. It has a transducer capacitance of Cpiezo = 6500 pF and a charge sensitivity of 1200 pC/psi where pC = pico coulombs, and psi = pounds per square inch. Suppose CF = 1000 pF and RF = 10MΩ. We have the following

Voltage Gain = Cpiezo/CF = 6500 pF/1000 pF = 6.5

Vpiezo = Qpiezo/Cpiezo = [1200 pC/psi]/6500 pF

Vout = Vpiezo x Voltage Gain = {[1200 pC/psi]/6500 pF} x 6.5 = 1.2 volts/psi

High pass filter cut-off frequency @ - 3 dB = 1/2π(10MΩ)(1000 pF) = 15.924 Hz

We will now look at am example of a low noise FET amplifier for a piezo device is shown in Figure 6.

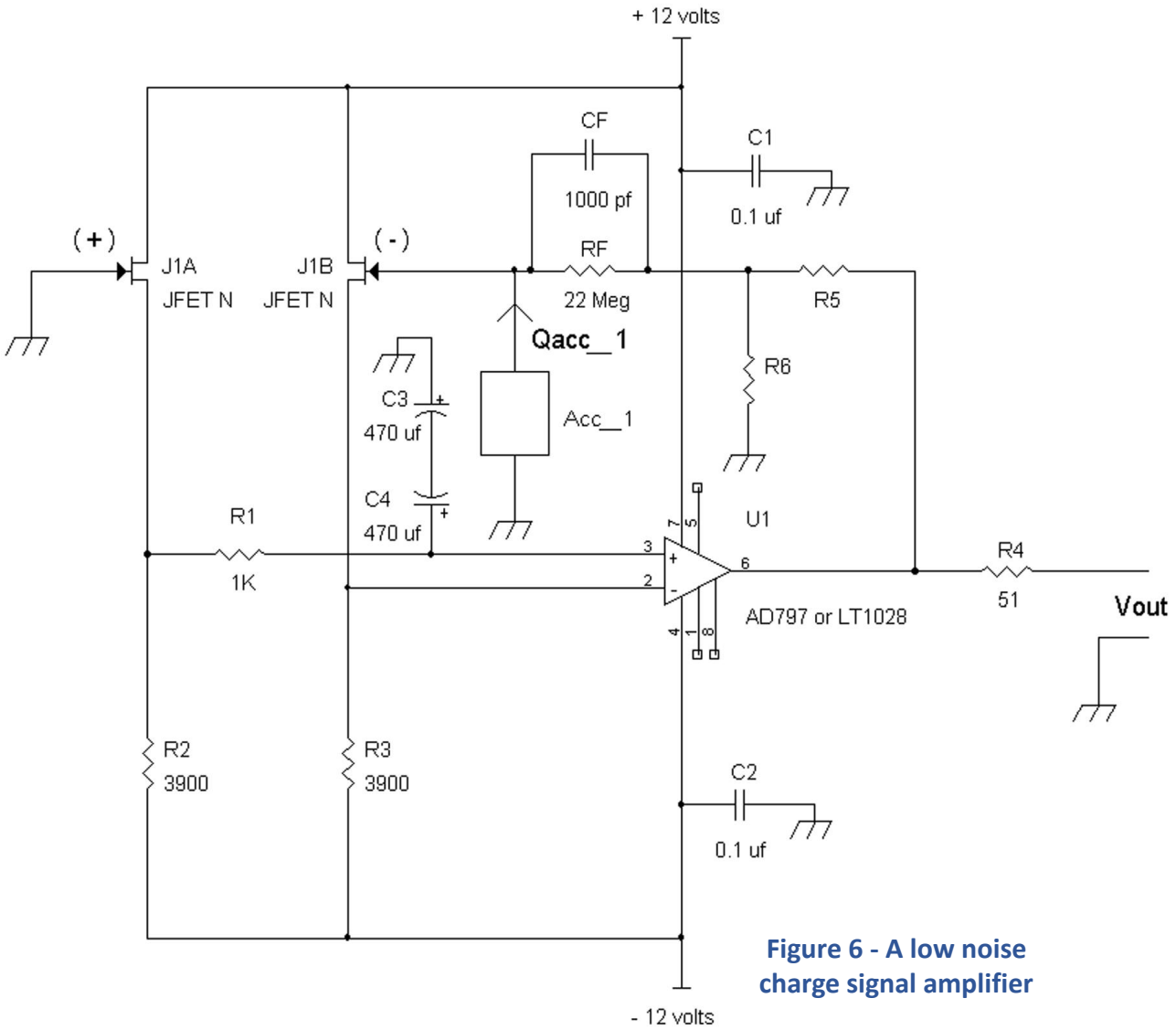


Figure 6 - A low noise charge signal amplifier

The charge amplifier above uses an piezo signal source such as a piezo accelerometer, Acc_1 that provides a charge signal Qacc_1 into the gate input terminal of FET J1. Although the schematic shows an accelerometer as the signal source, other types of charge output devices can be used such as a quartz accelerometer, piezoelectric pressure sensor, or piezoelectric hydrophone.

JFETs J1A and J1B such as the LSK389 or LSK489 are source followers. They are coupled to the (+) and (-) inputs of U1, a low noise bipolar input stage op amp. By taking advantage of the low gate current in J1B, noise is kept to a minimum. However, source follower J1B does provide some phase shift (in the negative feedback loop) at high frequencies that can cause the charge amplifier to oscillate if the output of U1 were to be connected to RF and CF directly via bypassing R5 and R6, which "wires" the amplifier in unity gain configuration.

To ensure sufficient phase margin that avoids oscillation, the amplifier's voltage gain factor is increased above unity gain via voltage divider R5 and R6. The voltage division by R5 and R6 adds more phase margin to the negative feedback amplifier to ensure stable and oscillation free operation. With the insertion of R5 and R6 in the feedback path, the voltage gain factor is [1 + (R5/R6)].

For example, if R5 = 510Ω and R6 = 100Ω, the amplifier system starts off with a voltage gain of [1 + (510/100)] = 6.1, which was found experimentally to provide sufficient phase margin to avoid oscillation in some op amps.

It is recommended that R5||R6 << RF, and for the values chosen 510Ω||100Ω is indeed << 10MΩ. Also it is preferred that RF is driven with a low impedance source < 100Ω, and the drive resistance (via the Thevenin resistance) is R5||R6 = 510Ω||100Ω = 83Ω < 100Ω.

The overall gain of the system given the piezo device that has a rated capacitance of Cpiezo is:

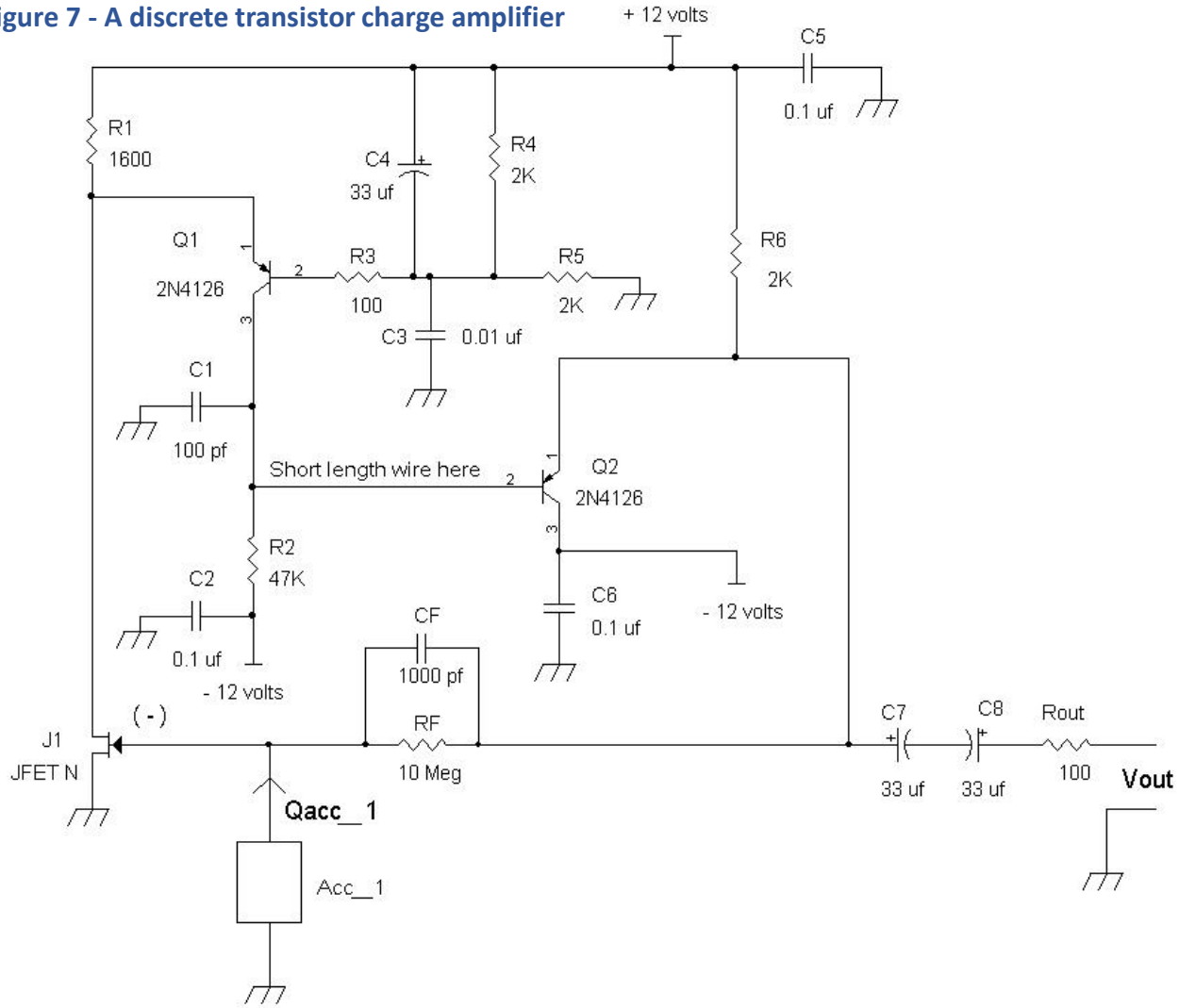
$$V_{out}/V_{piezo} = -[1 + (R5/R6)] \times C_{piezo}/CF$$

Where $V_{piezo} = Q_{piezo}/C_{piezo}$
Figure 6 shows nominally CF = 1000 pF and RF = 22MΩ, but other values may be used. Also keep in mind that the high pass filter cut-off frequency is $1/2\pi(RF)(CF)$

In Figure 6, JFETs, J1A and J1B, are configured as differential source followers. Although normally, the source of J1A would be tied directly to the (+) input of U1 (pin 3), lower noise can be achieved via low pass filter R1, C3, and C4 that removes random noise from the source of J1A. Achieving the lowest possible equivalent input noise is necessary when the high impedance signal source includes capacitance across it.

For a discrete charge amplifier implementation see Figure 7 below.

Figure 7 - A discrete transistor charge amplifier



In the charge amplifier in Figure 7 A on the previous page, a low noise JFET, J1 may be an LSK170. Although the capacitance of the LSK170 is higher than an LSK489, which can also be used, the accelerometer's capacitance (e.g., Cpiezo in Figure 3(a)) is much higher making the input capacitance of the JFET negligible.

The advantage of using a discrete design is that this amplifier has only one voltage gain stage that allows its output at the emitter of Q3 to be connected directly to RF and CF for an oscillation free operation. Because of the finite open loop gain of this amplifier, the voltage gain, Cpiezo/CF, should be generally kept to ≤ 10.

FET J1 and bipolar transistor Q1 form a folded cascade amplifier. With about 6 volts at the base of Q1, there is about 6.7 volts at Q1's emitter, which forms 5.3 volts across R1 = 1600Ω. This results in about 3.3 mA of current flowing into R1. The DC voltage at the gate of J1 will be approximately – 0.5 volt or so due to the negative feedback configuration via RF. Working backwards from the emitters of Q3 and Q2, the base of Q2 should have about [(– 0.5 volt – VEB_{Q2}) = -1.2 volts at the base of Q2 and the collector of Q1.

The voltage across R2 is then [-1.2 volts – (- 12 volts)] = 10.8 volts, which results in Q1's collector current of (10.8 volts/47KΩ) = IC_{Q1} = 0.230 mA. Since β >>1, the emitter current is essentially equal to the collector current, which is 0.230 mA.

The sum of Q1's emitter current and J1's drain current is the current flowing through R1, which is 3.3 mA.

Put in another way, the $I_{R1} = ID_{J1} + IE_{Q1}$

Also note that the current gain of Q1 (and Q2) is high with β >>1, which leads to $IE_{Q1} = IC_{Q1}$.

Therefore, $I_{R1} = ID_{J1} + IC_{Q1}$

By use of algebra,

$ID_{J1} = I_{R1} - IC_{Q1}$

I_{R1} = 3.3 mA and IC_{Q1} = 0.230 mA

Therefore, the drain current of J1,

ID_{J1} = 3.3 mA – 0.230 mA

ID_{J1} = 3.07 mA = drain current of J1.

Open loop gain of the charge amplifier is the transconductance of J1, g_{mJ1}, muliplied by R2 and K_1. The scaling factor K_1 represents the transfer of signal from the drain of J1 to Q1. There is a small amount of signal taken away from R1. Also we can approximate that the gain of emitter follower, Q2 = 1.

Open loop gain = g_{mJ1} x R2 x K_1

For an LSK170 biased at about 3 mA, g_{mJ1} = 15 mS = 15 mmho

R2 = 47KΩ

$K_1 = R1/[(R1) + (1/g_{mQ1})]$

Note that: $(1/g_{mQ1})$ = 0.026 volt/IC_{Q1} =0.026 volt/0.230 mA = 113Ω = $(1/g_{mQ1})$

K_1 = 1600Ω/[1600Ω + 113Ω] = 0.934

Open loop gain = g_{mJ1} x R2 x K_1 = 15 x 47 x 0.934 = 705 x 0.934 = 658.

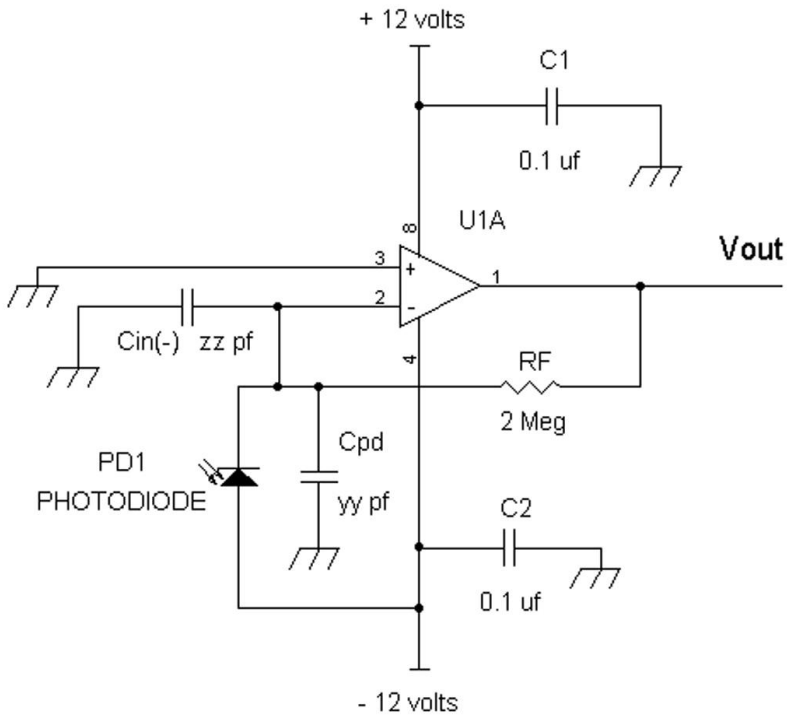
Note that Q2 form an emitter follower circuit and Q2 provides a low impedance output for Vout. Because there will be an offset voltage, DC blocking capacitors C7 and C8 are used.

Specific Applications
Photodiode Preamps

In some JFET op amps such as the AD743, the input capacitance is in the order of 18 to 20 pF. In comparison, with an LSK489 dual FET, the input capacitance is in the order of 3 pF, which will be suitable for low noise photodiode applications. In this section we will see why it is important to have low equivalent input noise and low input capacitance in a photodiode preamp. A simple photodiode is shown in Figure 8 below, which uses an op amp.

In the photodiode amplifier below, when light is shined onto the photodiode, current is generated by the photodiode, PD1. As configured with the cathode of PD1 connected to the (-) input terminal of U1, Vout generates a positive voltage proportional to the amount of light into the photodiode. Also shown in Figure 8 are the equivalent capacitances from the photodiode, Cpd, and (-) input terminal, Cin(-), which are connected in parallel. To minimize Cpd, the photodiode capacitance, the anode of PD1 is connected to the minus 12 volt power supply for maximum reverse bias to lower its junction capacitance. For example, if a BPV10 photodiode is used, Cpd is about 2.7 pF at 12 volts reverse bias. At a lower reverse bias voltage such as 1 volt, Cpd is about 7 pf.

Figure 8 - A simple photodiode transresistance amplifier



For low noise considerations, these two capacitances, Cpd and Cin(-), should be low as possible. The reason is that the equivalent input noise density voltage, Vnoise_input of the op amp will be amplified in the following manner at Vout, neglecting any noise current from the photodiode:

Vout_noise for a bandwidth of 1 Hz = (Vnoise_input) $\sqrt{1 + (\omega RFCt)^2}$ + $\sqrt{4kTRF}$ (1)

Where ω = $2\pi f$, RF = feedback resistor, k = 1.38 x10^{-23} Joules per degrees Kelvin, T = 298 degrees Kelvin

Ct = Cpd||Cin(-) = total capacitance at the (-) input terminal, and
Ct = Cpd + Cin(-)

$\sqrt{4kTRF}$ = thermal noise voltage of the feedback resistor RF for a bandwidth of 1 Hz.

As we can see from the equation above, the output noise, Vout_noise, goes higher if *Ct* is increased.

In designing a low noise transresistance preamps the goals are to:

1. Minimum equivalent input noise voltage. Equation (1) above shows that the output noise voltage is dependent on the equivalent input noise voltage, Vnoise_input.
2. Minimize noise current from the (-) input because the noise current at the input will form a noise voltage across the feedback resistor. Generally, a JFET is desirable for the (-) input because of its low gate noise current.
3. Minimize the capacitance from the (-) input to ground. The equation (1) shows that more noise is generated at the output when the capacitance, Ct = Cpd + Cin(-), at the (-) input terminal is increased.
4. Use as large value RF as possible. At first glance, it would appear increasing the resistance in RF would increase the output noise because of the resistor's thermal noise. This is true but the signal amplification from the photodiode is increased more so that results in a net increase in signal to noise ratio when RF is increased in value. For example, doubling the value in RF increases the resistor noise from RF by $\sqrt{2}$ = 1.41 while increasing the photodiode signal output voltage by 2. Thus, there is a net gain of $\sqrt{2}$ or + 3 dB, in terms of signal to noise ratio in this example.

In Figure 8, the typical input capacitance, Cin(-) at the (-) input of an FET op amp is about 18 pf. To lower the capacitance of the op amp, a low capacitance and low noise JFET is used as a buffer or source follower to the (-) input. See Figure 9.

A low noise JFET such as an LSK189 is configured as a source follower, with a source biasing resistor R3. In terms of input capacitance at the gate of J1 with an LSK189, it is about 3 pF from the gate to the drain, which is much less than the 18 pF of Cin(-). Capacitance between the gate and ground due to the gate to source capacitance approaches zero. This is because the source follower configuration provides substantially the same AC voltage at the gate and at the source, which substantially cancels out the capacitance between the gate and the source. The source follower also greatly reduces the capacitance seen at the gate to ground even when the source is driving signal into a capacitive load, Cin(-), the capacitance at the (-) input terminal of the op amp U1A.

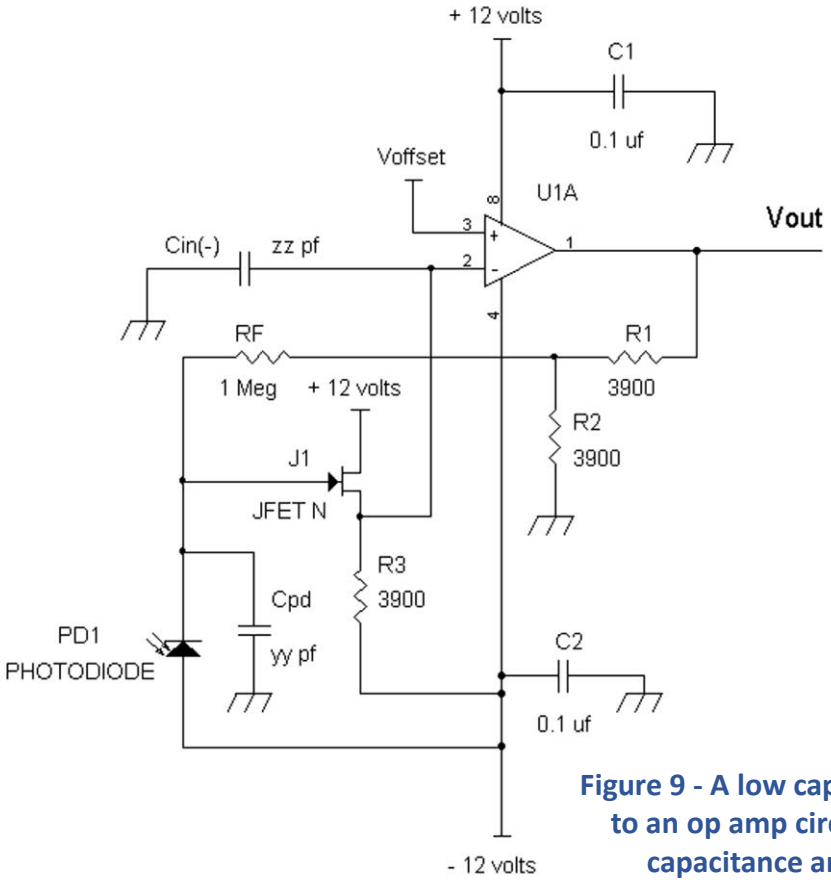


Figure 9 - A low capacitance JFET added to an op amp circuit to lower input capacitance and reduce noise

It should be noted that the source follower circuit may add some phase shift to the overall amplifier circuit. To ensure phase margin and no oscillations, a resistive divider R1 and R2 is used. With the values given at 3900Ω for R1 and R2, the equivalent feedback resistance is [1 + (R2/R1)] x RF = 2 x 1MΩ = 2MΩ, the same resistance value shown in Figure 8 for RF.

If the (+) input of the op amp in Figure 9 is grounded, such that Voffset = 0 volts, Vout will most likely have a DC offset. To "zero" Vout when there is no signal from the photodiode, a clean DC voltage, Voffset may be applied to the (+) input of U1.

Op amp U1A = AD797 has an equivalent input noise voltage of 0.9 nV/$\sqrt{Hz}$ and J1 =LSK189 with an equivalent input noise voltage of 1.8 nV/$\sqrt{Hz}$, the total equivalent input noise voltage is about 2.0 nV/$\sqrt{Hz}$. This is lower than a very low noise JFET op amp such as an AD743 that has 3.2 nV/$\sqrt{Hz}$. Note that bipolar input stage op amps AD797 with 0.9 nV/$\sqrt{Hz}$ has lower equivalent input noise voltage than 2.0 nV/$\sqrt{Hz}$, but the AD797's input noise current is too high and are not suitable for amplifier circuits with large value feedback resistors (RF) in the MΩ such as the circuit shown in Figure 8.

Note that J1 may be substituted with an LSK170 (0.9nV/$\sqrt{Hz}$) if a slight increase in capacitance from the gate to ground is acceptable. This FET has about half the equivalent input noise of the LSK189.

Specific Applications

Extending the Frequency Response of a Transresistance Amplifier

In transresistance amplifiers, a feedback resistor will have a capacitance, CF, across its leads. This capacitance will reduce the bandwidth of the output signal at high frequencies. See Figures 10(a) and 10(b) below.

Figure 10(a) shows a photodiode preamp with Ct = Cpd + Cin(-), and CF a capacitor across the feedback resistor RF. CF can be the internal parasitic capacitance from resistor RF, or it can be capacitor often connected across RF to add positive phase shift that offsets the negative shift from Ct. This added positive phase shift due to CF ensures stability in the photodiode preamp. However, one side effect from CF is reducing the bandwidth of the amplified photodiode signal at Vout.

The -3 dB bandwidth at Vout is $1/[2\pi(RF)(CF)] = f_{-3dB}$
For example, RF = 2MΩ and CF = 1pF, then $f_{-3dB} = 1/[2\pi(2M\Omega)(1pF)] = 79.6$ kHz
One way to reduce the effects this roll off in frequency response is to make RF a series connection of ten 200KΩ resistors. If CF is still 1pF, the new bandwidth will be: $f_{-3dB} = 1/[2\pi(200K\Omega)(1pF)] = 796$ kHz

However, there is another alternative and that is to equalize the frequency response as shown in Figure 10(b).

Figure 10(a) - Simple preamp.

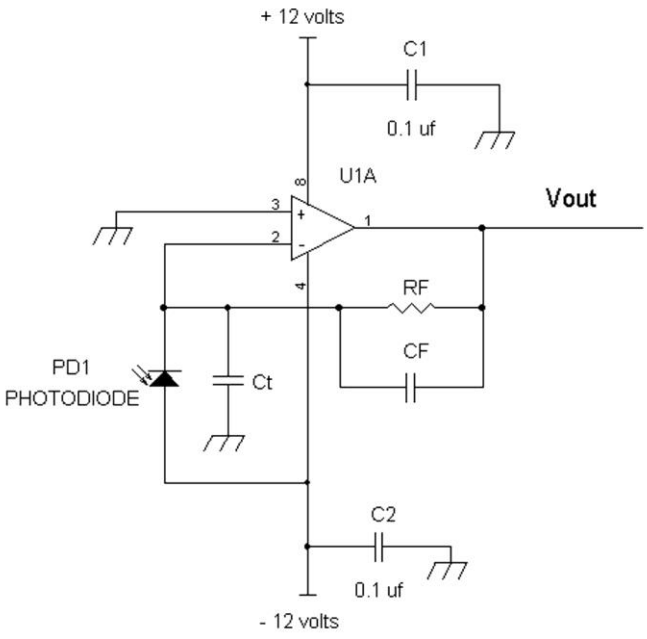
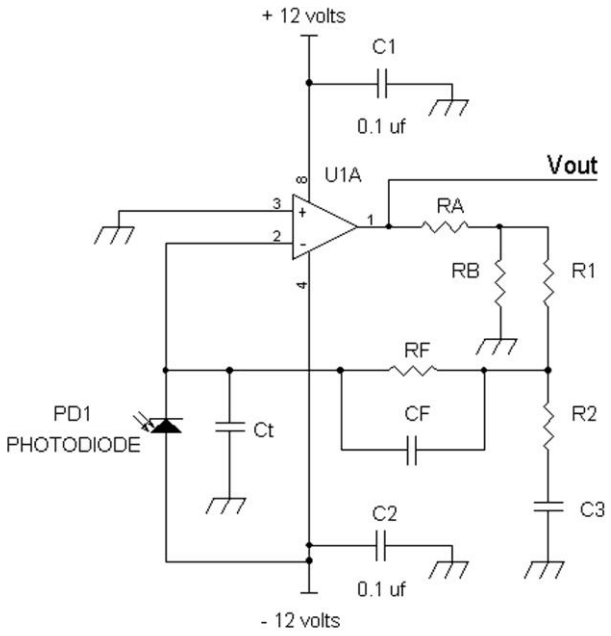


Figure 10(b) - Simple preamp with equalization.



For now, let's assume that that op amp U1A in Figure10(b) has sufficient phase margin to not oscillate when RA = 0Ω, and when RB = open circuit or removed.

If (R1 + R2)(C3) = (RF)(CF) there will be a "boost" that compensates for the roll-off. When the boost ends is determined by the (R2)(C2) time constant. The amount of bandwidth extension is [1+ (R1/R2)]. Generally there is a limit on bandwidth extension. If R2 → 0Ω, then C3 is grounded and forms a low pass filter and lagging phase shift network with R1, that will most likely cause oscillation.

Generally, it is recommended to start with R2 = 33% of R1, which gives a bandwidth extension of [1 + (R1/0.33R1)] = [1 + 3] = 4 = bandwidth extension.

For example, if RF= 2MΩ and CF = 1pF, we want R1 <<RF, so let's make R1 = 10KΩ and R2 = 3.3KΩ, then (R1 + R2)(C3) = (RF)(CF) or (10KΩ + 3.3KΩ)(C3) = (13.3KΩ)(C3) = (2MΩ)(1pF), or

C3 = (2MΩ)(1pF)/(13.3KΩ) = 150 pf = C3. With these values, the frequency response will increase from 79.6 kHz to about 318 kHz for Figure 10(b).

Note: Often the op amp U1A may require voltage divider resistors RA and RB to ensure sufficient phase margin so that the amplifier in Figure10(b) does not oscillate. Typically, start out with a voltage divider of 2 or more. That is, (RA/RB) ≥ 1. Also, it is recommended that RA||RB ≤ 500Ω and that RA||RB << R1.

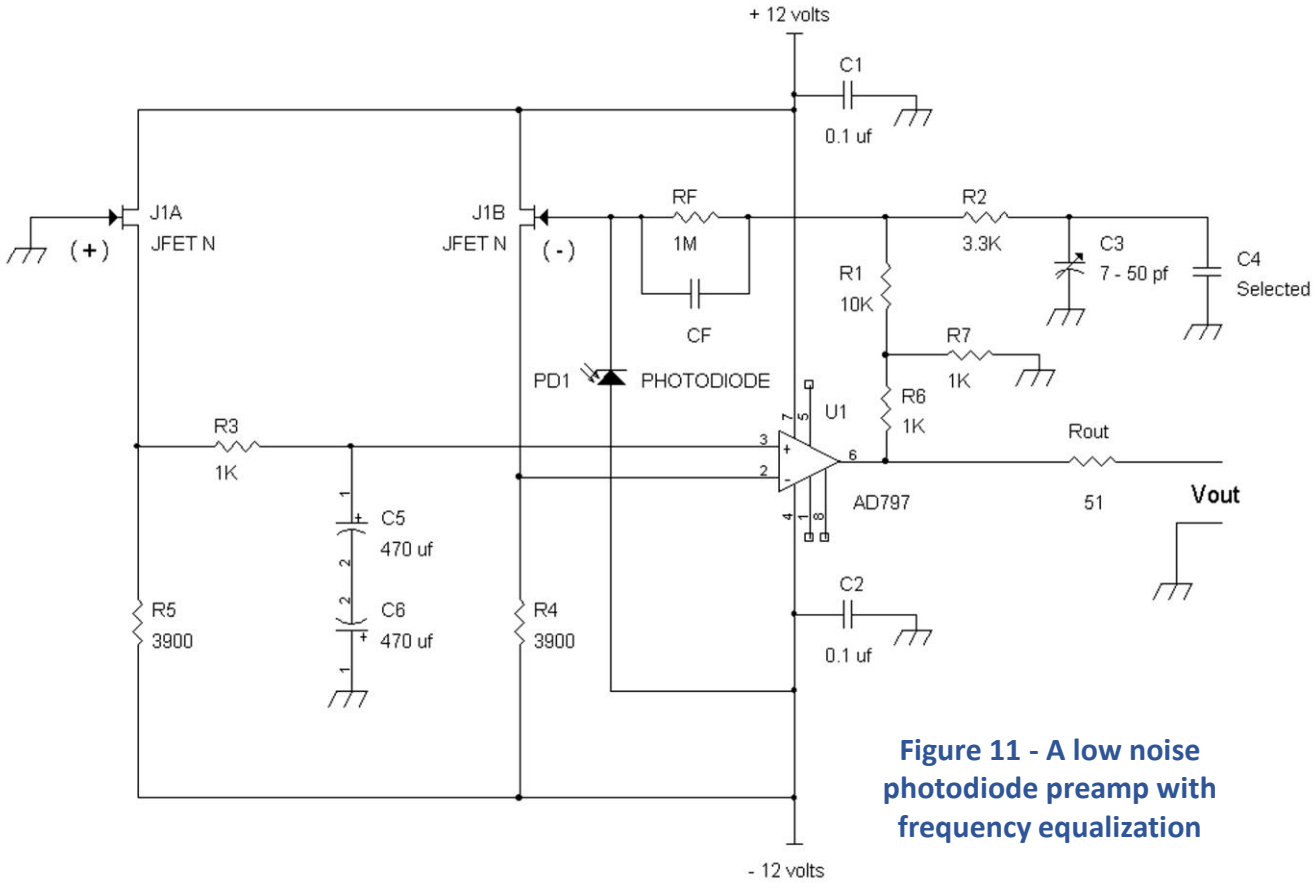


Figure 11 - A low noise photodiode preamp with frequency equalization

In Figure 11 on the previous page, the effective feedback resistor is about 2MΩ because R6 and R7 provide a divide by two voltage divider. The effective feedback resistance is [1 + (R6/R7)] x RF = [1 +1] x 1MΩ = 2MΩ, given that R1 << RF or 10KΩ << 1MΩ.

J1A and J1B are low noise and low capacitance matched pair JFETs such as the LSK489.

U1 can be typically a bipolar input stage op amp for the lowest equivalent input voltage noise density such as the AD797. Variable trimmer capacitor C3 is adjusted for the flattest frequency response.

Alternatively C3 may be adjusted for the best pulse response. Generally an LED is driven with a square wave signal and is pointed into the photodiode PD1. C3 is adjusted for the fastest rise and fall times while avoiding overshoot at Vout.

In Figure 11, R6 and R7 form a voltage divider to multiply RF for an effective resistance of 2MΩ. But R6 and R7 also adds some series resistance to R1. This series resistance is R6||R7 = 1KΩ||1KΩ = 500Ω, which is the Thevenin resistance from the voltage divider circuit. To calculate the proper time constants for frequency compensation we have:

[(R6||R7) + (R1 + R2)] x [C3 + C4] = RF x CF which leads to:

[C3 + C4] = [RF x CF]/ [(R6||R7) + (R1 + R2)]

For example, in Figure 11, suppose CF = 2.2 pF is the capacitance across RF = 1MΩ.

Also U1 = AD797

[C3 + C4] = [1MΩ x 2.2 pF]/ [(500Ω) + (10KΩ + 3.3KΩ)]

[C3 + C4] = [1MΩ x 2.2 pF]/ [(500Ω) + (13.3KΩ)]

[C3 + C4] = 72.46 x 2.2 pF = 159 pF

Let C4 = 130 pF so that the remaining 29 pF can be set by variable capacitor C3. Note that C3 is adjusted for best transient or frequency response.

The circuit was built with and without the equalization network, R1, R2, C3, and C4. Without the equalization network and with CF = 2.2 pF, the – 3 dB measured frequency response was about 71 kHz which matches closely to [1/2π(1MΩ)(2.2 pF)] = 72.5 kHz. The bandwidth extension is [1 + (R1/R2)] = [1 + (10K/3.3K)] = [1 +3] = 4. Thus, we will expect the frequency response to be extended to 4 x 72.5 kHz = 290 kHz. With the equalization network and C4 adjusted, the measured frequency response was extended to > 300 kHz.

Note: When an LT1028 op amp was used instead of the AD797 for U1, R7 had to be reduced to 100Ω to avoid oscillation and to provide sufficient phase margin. Not all op amps will necessarily have the enough phase margin to ensure an oscillation free condition with R6 = R7 in Figure 11. At times R7 may have to be lowered in value for stability, but also keep in mind that the effective feedback resistance is RF x [1 + (R6/R7)].

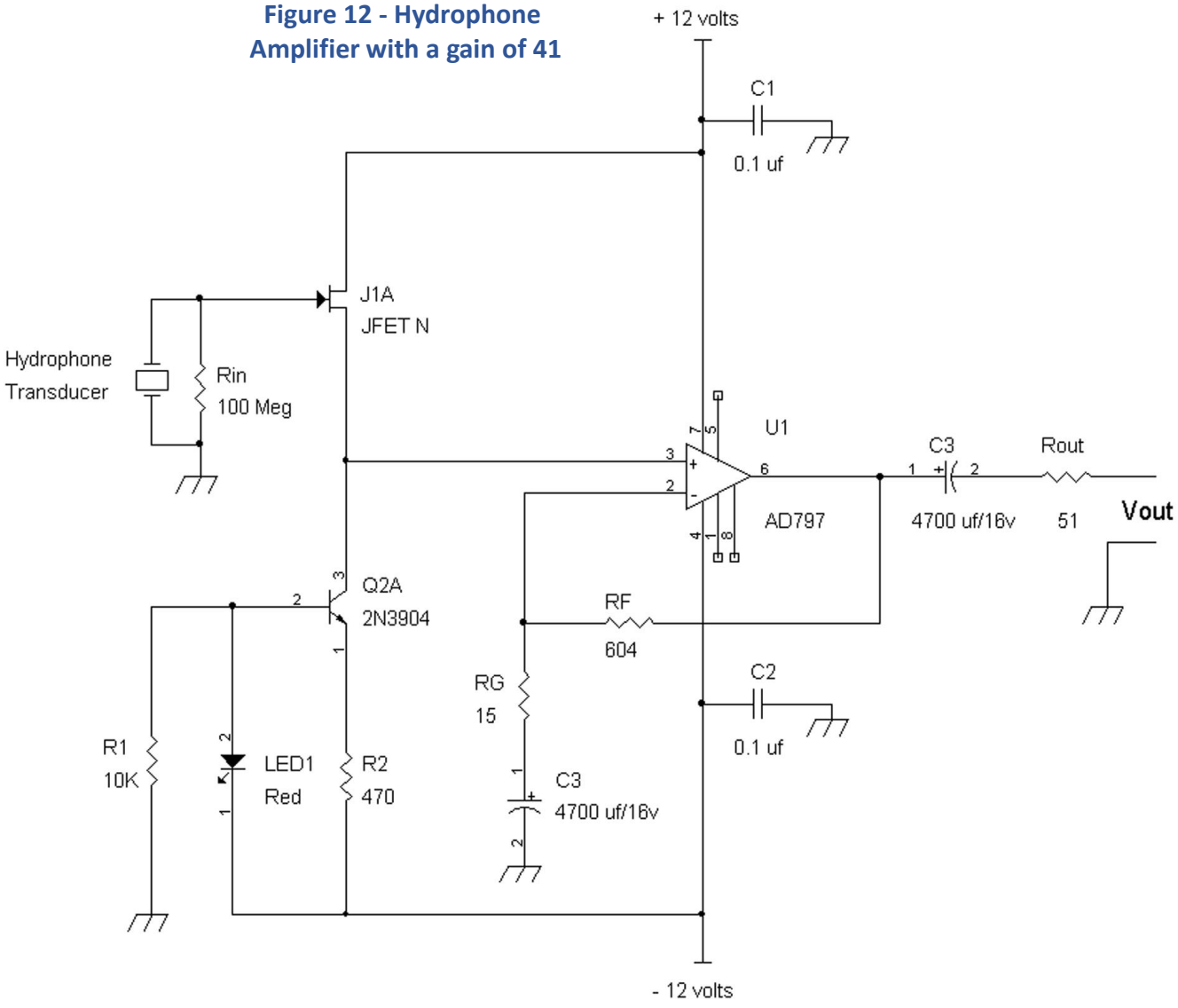
Specific Applications

Hydrophone Voltage Gain Amplifier

Figure 12 shows an example with a hydrophone amplifier.

In some instances, piezoelectric elements can be amplified with a low noise voltage amplifier instead of a charge amplifier. In this case a hydrophone transducer or microphone is connected to a source follower circuit J1A and current source Q2A. J1A can be an LSK170 for the lowest noise. Current source circuit R1, LED1, R2, and Q1A may be replaced with a 3900Ω resistor from the source of J1A to – 12 volts.

Figure 12 - Hydrophone Amplifier with a gain of 41



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LINEAR SYSTEMS

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Higher-Performance **Military** Sensor Signal Chains

By: Ron Quan

Higher-performance sensors are becoming increasingly important to modern battlefield systems. Sensors ranging from sonobuoys to radiation detectors are critical, leading-edge components of C4ISR systems. Better sensor systems enable earlier threat detection and more effective countermeasures.

Military systems employ a wide range of sensors – nuclear, biological, and chemical sensing, infrared, electro-optical, laser, radar, and acoustical – that all have one aspect in common: the requirement for ultra-low-noise signal chains to produce the best possible sensor signal. Less-than-optimal front-end amplification means C4ISR clients receive inadequate information and are not able to make effective, real-time decisions.

This paper describes techniques to employ to create the lowest-noise, most effect front-end amplification for sensor signal chains. Advanced lithography design and fab process techniques enable the creation of discrete components uniquely capable of performing the critical initial amplification of sensor signals. Integrated circuits contain a wide range of components and can include specialized design features that preclude design optimization for low noise. As this paper documents, ultra-low-noise discrete components added to an IC-based circuit will produce the lowest-noise signal chain. Though this paper focuses on the LSK489 dual monolithic N-channel JFET, many other Linear Systems parts -- including the LSK389, LSK170 and LSK189 -- also are excellent sensor system components.

Linear Systems is the world leader in ultra-low-noise monolithic dual JFETs and other front-end discrete components key to high-performance sensing systems. For over three decades, Linear Systems has led the development of this class of devices, and it continues to advance their design and introduce new sensor-specific parts.

Linear Systems provides a variety of FETs (Field Effect Transistors) suitable for use in low noise amplifier applications for photo diodes, accelerometers, transducers, and other types of sensors.

In particular, low noise JFETs exhibit low input gate currents that are desirable when working with high impedance devices at the input or with high value feedback resistors (e.g., ≥1MΩ). Operational amplifiers (op amps) with bipolar transistor input stages have much higher input noise currents than FETs.

In general, many op amps have a combination of higher noise and input capacitance when compared to some discrete FETs. For example, a typical FET input op amp may have input capacitances of about 20 pF, whereas many discrete FETs have input capacitances of less than 5 pF. Also, there are few low noise FET input op amps that have equivalent input noise voltages density of less than 4 nV/$\sqrt{Hz}$. However, there are a number of discrete FETs rated at ≤ 2 nV/$\sqrt{Hz}$ in terms of equivalent Input noise voltage density. For those op amps that are rated as low noise, normally the input stages use bipolar transistors that generate much greater noise currents at the input terminals than FETs. These noise currents flowing into high impedances form added (random) noise voltages that are often much greater than the equivalent input noise.

One advantage of using discrete FETs is that an op amp that is not rated as low noise in terms of input current can be converted into an amplifier with low input current noise. For example, see the circuit shown in Figure 1.

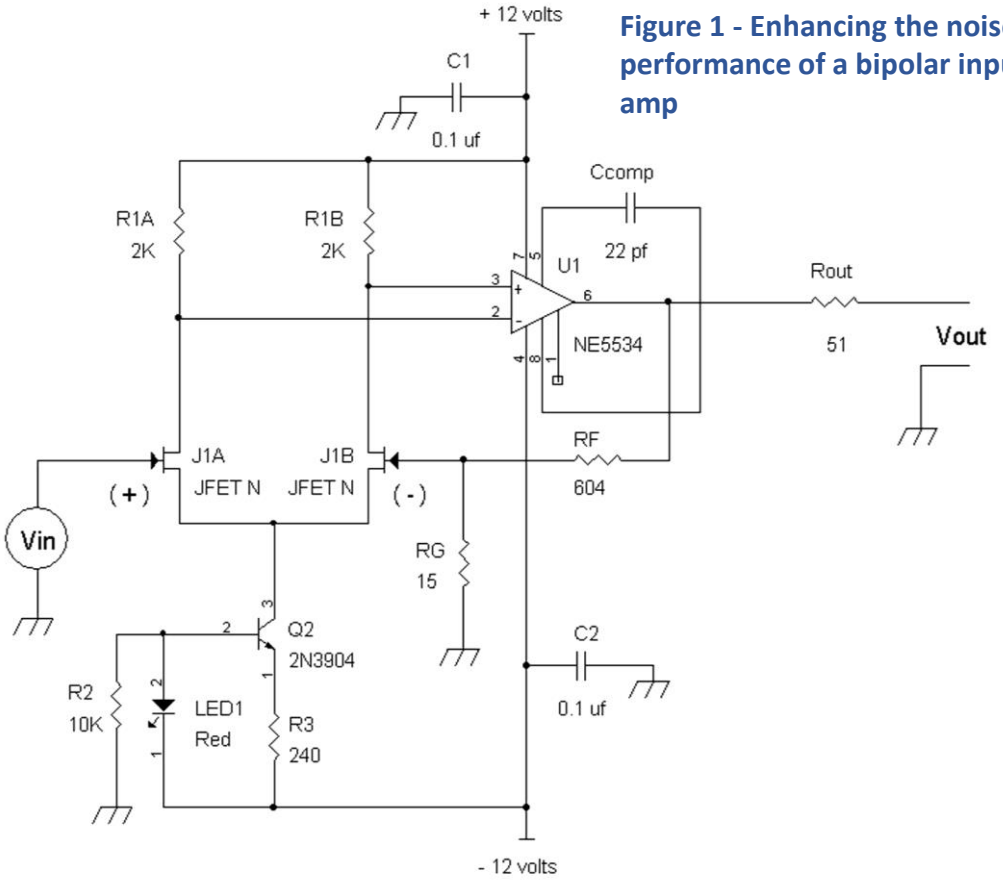


Figure 1 - Enhancing the noise performance of a bipolar input stage op amp

In Figure 1 on the previous page, current source Q2, JFETs J1A and J1B with load resistors R1A and R1B form a preamp to the input of U1 to provide better noise performance in terms of input bias current noise and equivalent input noise voltage. The collector current of Q2 is approximately 1 volt across R3 or about 4 mA. The drain currents of J1A and J1B are equal when Vin = 0, or about 2 mA each. With the load resistors set at 2KΩ, there are about 4 volts DC across each of these resistors. The typical transconductance, g_m, for an LSK489 matched dual JFET is about 3 mS = 3 mmho at 2 mA drain current. Thus, the differential mode gain from the gates of J1A and J1B to the drains of J1A and J1B will be approximately 3 mS x 2KΩ = 6.

Note: 1 mho = 1 S = 1 amp/volt, and 1 mmho = 1 mS = 1 ma/volt.

Although an NE5534 op amp has about 4 nV per root Hertz in terms of equivalent noise voltage density, its input bias noise current in the order of 0.60 pA per root Hertz. The DC gate current of a JFET will typically be less than 0.1 nA, and the input noise current will be:

$\sqrt{2qIg\ B}$ = noise current from the gate of the JFET

Ig = gate bias current
q = electron charge = 1.6 x 10^{-19} coulomb
B = bandwidth in Hertz. For a noise density calculation, the bandwidth is 1 Hz. Thus, B = 1.

For 0.1 nA = Ig.

$\sqrt{2qIg\ B}$ = 0.00566 pA/$\sqrt{Hz}$ = noise density current from the gate of the JFET.

In comparison to 0.60 pA/$\sqrt{Hz}$ for the input noise density current for the NE5534, the JFET has about 100 times lower input noise current at 0.00566 pA/$\sqrt{Hz}$. The LSK489 has 1.8 nV/$\sqrt{Hz}$ of noise voltage density per FET.

For J1A and J1B to be a dual matched JFET transistor such as the LSK489, the equivalent input noise voltage will be about 2.54 nV per root Hertz, or about 3.925 dB lower noise than the 4 nV/$\sqrt{Hz}$ rating of the NE5534. Alternatively, even lower noise can be achieved by using an LSK389B for J1A and J1B, which will result in an equivalent input noise voltage of 1.27 nV/$\sqrt{Hz}$. The LSK389B has typically 0.9 nV/$\sqrt{Hz}$ per FET. One should note that the added JFET front circuit (J1A and J1B) will increase the gain bandwidth product of the amplifier by the gain of the FET circuit. For example, at 2 mA per JFET, the tranconductance of the LSK489 is typically 3 mmho or 3 mS. With the 2KΩ load resistors, R1A and R1B, the differential mode gain is about 6. Thus, the 10 MHz gain bandwidth product of the NE5534 is increased to 60 MHz (6 x 10 MHz = 60 MHz). Note the feedback resistors, RF and RG, are set for a gain ≥ 6 to ensure stability in the amplifier without oscillation. That is, (RF/RG) ≥ 5 since the gain is [1 + (RF/RG)]. The tranconductance of the LSK389B is about 3 times more than the LSK489. Thus, if the LSK389 is used in Figure 1, (RF/RG) ≥ 20 to ensure stability without oscillation. Another way to reduce input bias current noise is shown in **Figure 2** via source followers, on the following page.

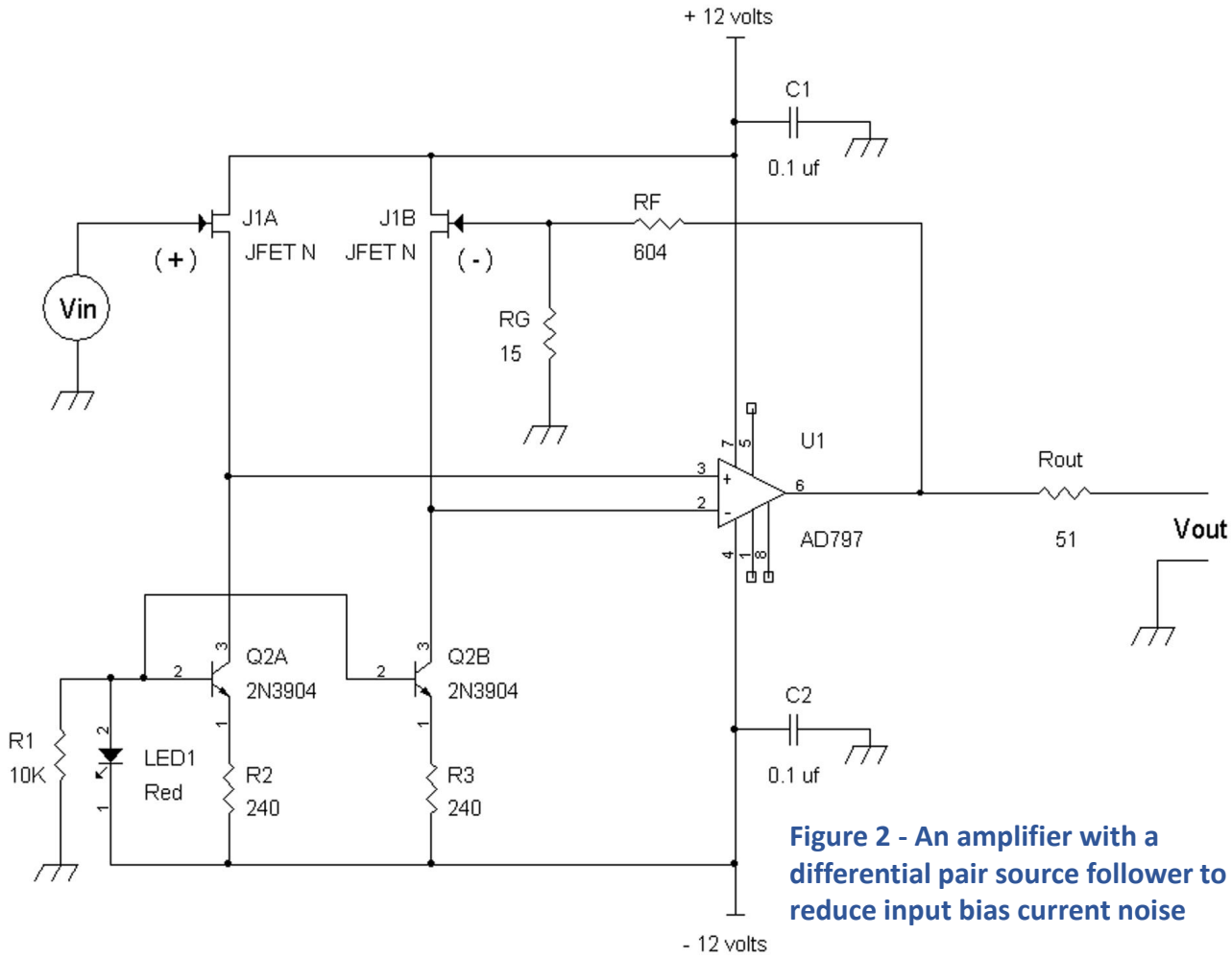


Figure 2 - An amplifier with a differential pair source follower to reduce input bias current noise

In Figure 2 above, FETs, J1A and J1B, are configured as source followers to the inputs of an op amp such as a low noise type, AD797 (or LT1028).

In terms of equivalent input voltage noise the AD797 and LT1028 are rated at about 0.9 nV/$\sqrt{Hz}$. However, their input noise currents are in the order of 1.0 pA/$\sqrt{Hz}$.

By using the source followers as shown, the input noise currents are reduced to about 0.00566 pA/$\sqrt{Hz}$.

For low input capacitance operation (< 3 pF), J1A and J1B can be a matched pair LSK489.

This will result in an equivalent input noise voltage of 2.7 nV/$\sqrt{Hz}$ with an LSK489. If slightly higher input capacitance is tolerated (< 5 pF), then an LSK389 B is used for an equivalent input noise voltage of 1.55 nV/$\sqrt{Hz}$.

Q2A and Q2B should be a matched pair of NPN transistors to ensure equal source currents for J1A and J1B. However, often purchasing discrete transistors on tape provides very close DC matching in terms of base to emitter turn on voltage.

Specific Applications

Piezoelectric Element Preamps

One of the common types of sensors today is based on the piezoelectric effect. These types of sensors include accelerometers and hydrophone transducers.

The basic piezoelectric device is modeled at the bottom of the page.

Figure 3(a): Charge model of piezo device.

Figure 3(b): Equivalent voltage model.

In Figure 3(a), a piezoelectric device delivers charge instead of current. The charge, Qpiezo, flows into a capacitor, Cpiezo, to develop a voltage. Recall that:

Qpiezo = Cpiezo x Vpiezo, or expressed another way via algebra:

Vpiezo = Qpiezo/Cpiezo (where Vpiezo is the voltage across the capacitor Cpiezo)

As shown in Figure 3(a), there is also a resistor, Rpiezo, in parallel with the charge generator and capacitor. Rpiezo has a very high resistance, usually very close to an open circuit. For example, the measured DC resistance across a piezoelectric earphone/microphone is > 2000 MΩ.

However, it may be easier to look at a piezoelectric device as a voltage generator. By equivalently converting the charge source, Qpiezo, and capacitor, Cpiezo into a “Thevenin” voltage source and series impedance, we have the model as shown in Figure 3(b).

From Figure 3(b) we see that the piezoelectric device provides an AC coupled signal and it cannot provide a sustained DC voltage across Rpiezo.

Figure 3(a) - Charge model of piezo device

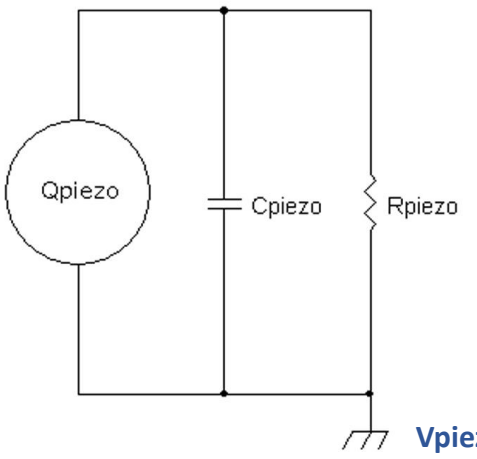
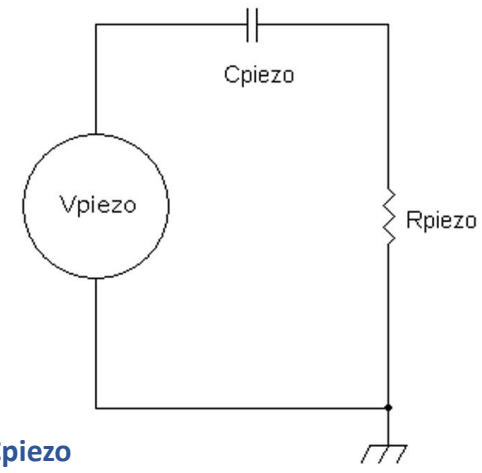


Figure 3(b) - Equivalent voltage model



Vpiezo = Qpiezo/Cpiezo

From Figure 3(b), we see that the low frequency cut-off response is dependent on the values of Cpiezo and Rpiezo. In practice for the most extended low frequency response, we need Cpiezo to load into a very high resistance value.

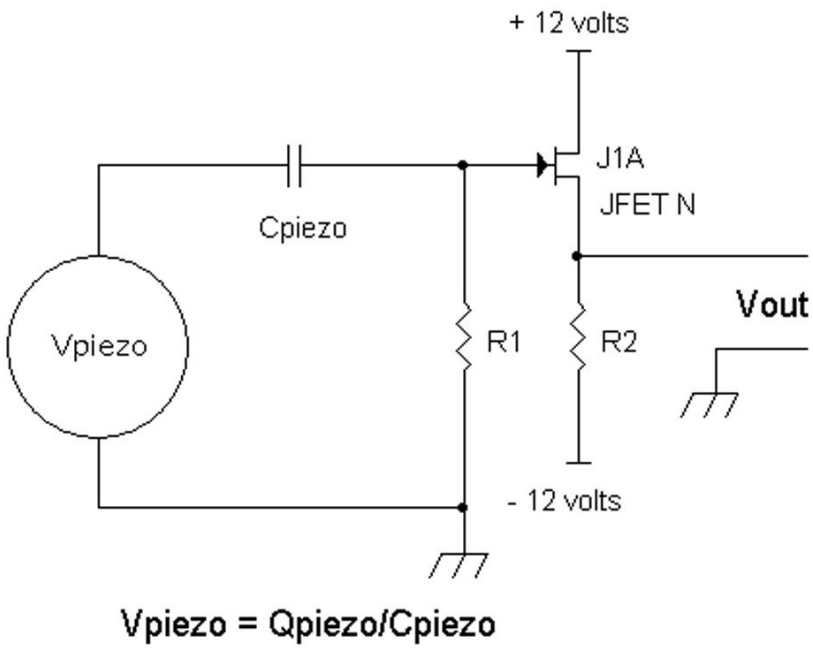
For simplicity, let's take a look at a simple FET buffer amplifier in Figure 4 at the bottom of the page.

Figure 4 A piezo device connected to a simple JFET source follower amplifier.

Generally, R1 can be in the range of 1MΩ to 10MΩ. However, it is not uncommon to have R1 in the order of 100MΩ to 1000MΩ. Source resistor R2 is set to bias the source to a DC bias current from about 100 µA to 5 mA or R2 can be in the range of 100KΩ to 2KΩ. J1A can be an LSK170 JFET. The drain of J1 is connected to a plus supply voltage and the source provides a signal voltage, Vout with a medium to low impedance output resistance that is able to drive another amplifier. Note that Vout may be connected in series to an AC coupling capacitor to remove the DC voltage at the source of J1A.

Another way to amplify the signal from a piezo device is shown in Figure 5 on the next page. For simplicity, we will ignore the effect of Rpiezo, which is close to infinite resistance.

Figure 4 - A piezo device connected to a simple JFET source follower amplifier



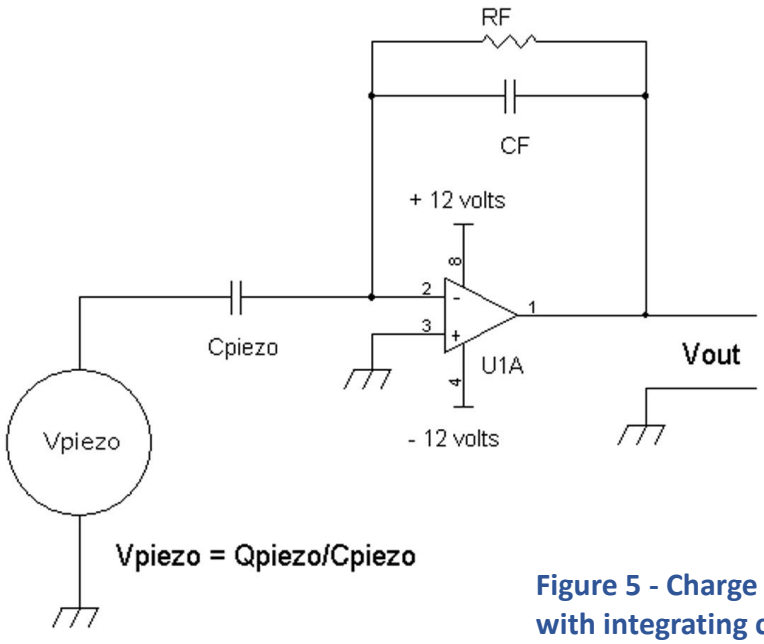


Figure 5 - Charge amplifier with integrating capacitor CF

If we ignore the feedback resistor, RF, for now, then we see that the gain is:

Vout/Vpiezo = - ZCF/ZCpiezo

Where ZCF and ZCpiezo are the impedances for CF and Cpiezo

Vout/Vpiezo = - ZCF/ZCpiezo = - [1/jωCF]/[1/jωCpiezo] = - Cpiezo/CF

Since Cpiezo is fixed and is internal to the piezo device, the gain is changed by setting the value of CF. For example, the smaller the value of CF, the larger the gain.

Ideally, CF should work as an integrating capacitor. However, to prevent Vout from latching to the supply rails, RF is connected in parallel to CF provide a DC path from the output of U1A to the (-) input of the op amp. Resistor RF also provides a discharge path for CF.

It may be “counter intuitive” but RF actually works as a high pass filter and sets the low cut-off frequency. To see how this happens, let’s suppose RF = 1MΩ and CF = 1000 pF. At 10 Hz, the magnitude of the ZCF ~ 16M. Since CF is in parallel with RF, we see that RF at 1MΩ dominates ZCF||RF at 10 Hz. At low frequencies, we can then “ignore” CF and now see that Figure 5 looks like a differentiator circuit (imagine removing CF from the schematic) with Cpiezo as the input capacitor and RF as the feedback resistor. Now note that a differentiator circuit has a high pass filtering effect.

When the AC gain is calculated for magnitude versus frequency, the – 3 dB cut-off frequency for the high pass filter effect is 1/2π(RF)(CF), and the gain is Vout/Vpiezo = Cpiezo/CF.

As an example, consider the model 765M25 dynamic pressure sensor from Columbia Research Laboratories. It has a transducer capacitance of Cpiezo = 6500 pF and a charge sensitivity of 1200 pC/psi where pC = pico coulombs, and psi = pounds per square inch. Suppose CF = 1000 pF and RF = 10MΩ. We have the following

Voltage Gain = Cpiezo/CF = 6500 pF/1000 pF = 6.5

Vpiezo = Qpiezo/Cpiezo = [1200 pC/psi]/6500 pF

Vout = Vpiezo x Voltage Gain = {[1200 pC/psi]/6500 pF} x 6.5 = 1.2 volts/psi

High pass filter cut-off frequency @ - 3 dB = 1/2π(10MΩ)(1000 pF) = 15.924 Hz

We will now look at am example of a low noise FET amplifier for a piezo device is shown in Figure 6.

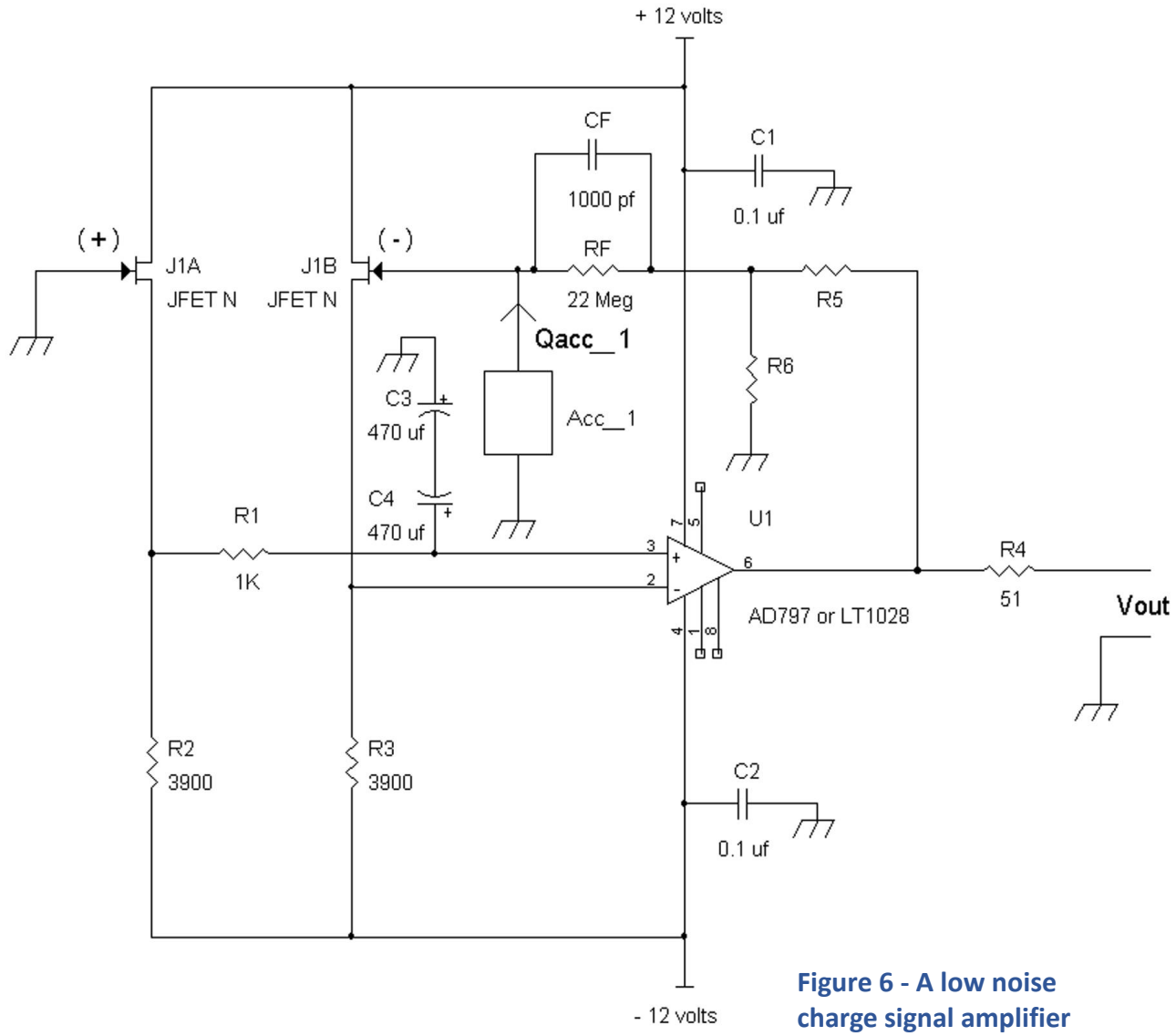


Figure 6 - A low noise charge signal amplifier

The charge amplifier above uses an piezo signal source such as a piezo accelerometer, Acc_1 that provides a charge signal Qacc_1 into the gate input terminal of FET J1. Although the schematic shows an accelerometer as the signal source, other types of charge output devices can be used such as a quartz accelerometer, piezoelectric pressure sensor, or piezoelectric hydrophone.

JFETs J1A and J1B such as the LSK389 or LSK489 are source followers. They are coupled to the (+) and (-) inputs of U1, a low noise bipolar input stage op amp. By taking advantage of the low gate current in J1B, noise is kept to a minimum. However, source follower J1B does provide some phase shift (in the negative feedback loop) at high frequencies that can cause the charge amplifier to oscillate if the output of U1 were to be connected to RF and CF directly via bypassing R5 and R6, which "wires" the amplifier in unity gain configuration.

To ensure sufficient phase margin that avoids oscillation, the amplifier's voltage gain factor is increased above unity gain via voltage divider R5 and R6. The voltage division by R5 and R6 adds more phase margin to the negative feedback amplifier to ensure stable and oscillation free operation. With the insertion of R5 and R6 in the feedback path, the voltage gain factor is [1 + (R5/R6)].

For example, if R5 = 510Ω and R6 = 100Ω, the amplifier system starts off with a voltage gain of [1 + (510/100)] = 6.1, which was found experimentally to provide sufficient phase margin to avoid oscillation in some op amps.

It is recommended that R5||R6 << RF, and for the values chosen 510Ω||100Ω is indeed << 10MΩ. Also it is preferred that RF is driven with a low impedance source < 100Ω, and the drive resistance (via the Thevenin resistance) is R5||R6 = 510Ω||100Ω = 83Ω < 100Ω.

The overall gain of the system given the piezo device that has a rated capacitance of Cpiezo is:

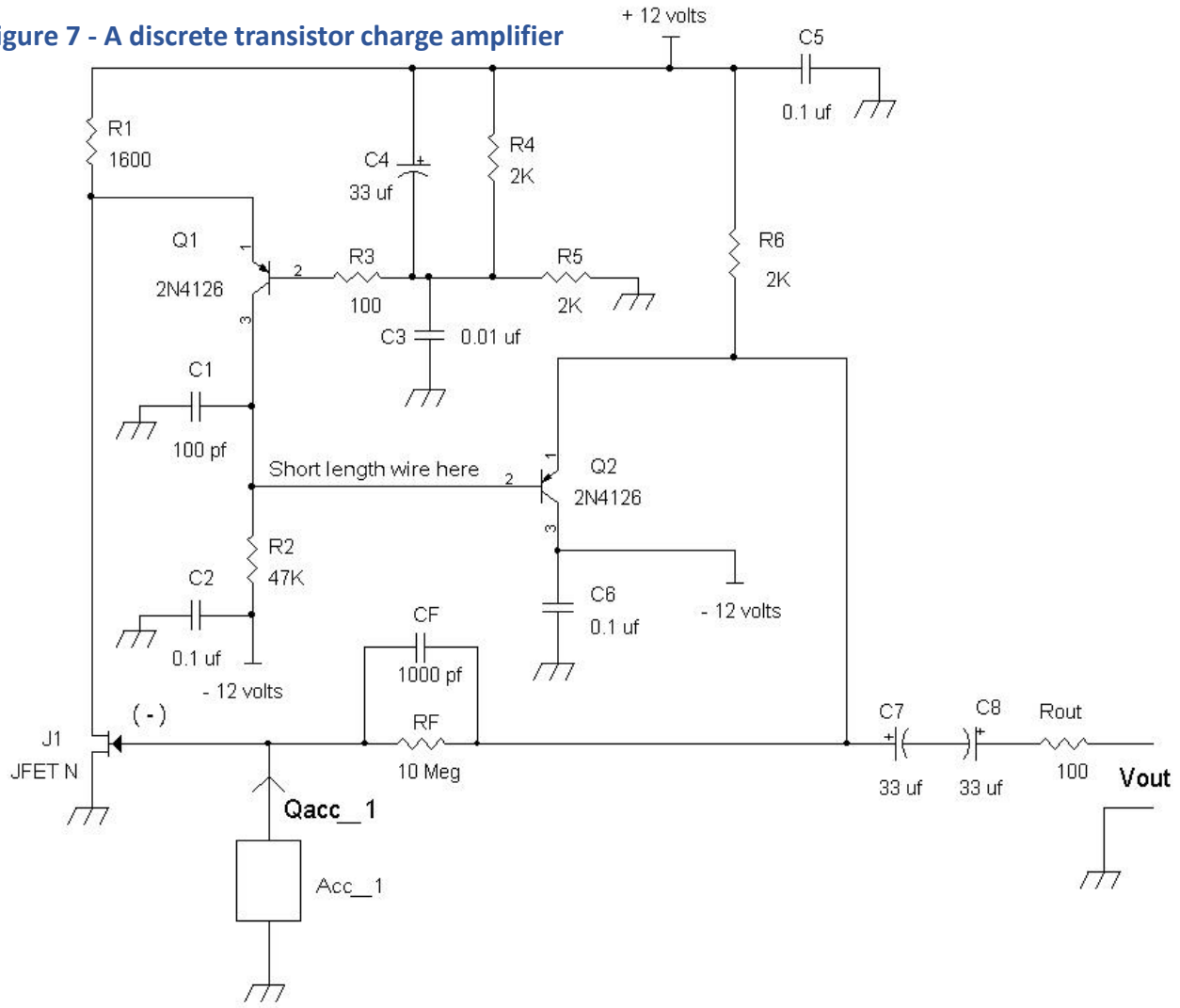
$$V_{out}/V_{piezo} = -[1 + (R5/R6)] \times C_{piezo}/CF$$

Where $V_{piezo} = Q_{piezo}/C_{piezo}$
Figure 6 shows nominally CF = 1000 pF and RF = 22MΩ, but other values may be used. Also keep in mind that the high pass filter cut-off frequency is $1/2\pi(RF)(CF)$

In Figure 6, JFETs, J1A and J1B, are configured as differential source followers. Although normally, the source of J1A would be tied directly to the (+) input of U1 (pin 3), lower noise can be achieved via low pass filter R1, C3, and C4 that removes random noise from the source of J1A. Achieving the lowest possible equivalent input noise is necessary when the high impedance signal source includes capacitance across it.

For a discrete charge amplifier implementation see Figure 7 below.

Figure 7 - A discrete transistor charge amplifier



In the charge amplifier in Figure 7 A on the previous page, a low noise JFET, J1 may be an LSK170. Although the capacitance of the LSK170 is higher than an LSK489, which can also be used, the accelerometer's capacitance (e.g., Cpiezo in Figure 3(a)) is much higher making the input capacitance of the JFET negligible.

The advantage of using a discrete design is that this amplifier has only one voltage gain stage that allows its output at the emitter of Q3 to be connected directly to RF and CF for an oscillation free operation. Because of the finite open loop gain of this amplifier, the voltage gain, Cpiezo/CF, should be generally kept to ≤ 10.

FET J1 and bipolar transistor Q1 form a folded cascade amplifier. With about 6 volts at the base of Q1, there is about 6.7 volts at Q1's emitter, which forms 5.3 volts across R1 = 1600Ω. This results in about 3.3 mA of current flowing into R1. The DC voltage at the gate of J1 will be approximately – 0.5 volt or so due to the negative feedback configuration via RF. Working backwards from the emitters of Q3 and Q2, the base of Q2 should have about [(– 0.5 volt – VEB_{Q2}) = -1.2 volts at the base of Q2 and the collector of Q1.

The voltage across R2 is then [-1.2 volts – (- 12 volts)] = 10.8 volts, which results in Q1's collector current of (10.8 volts/47KΩ) = IC_{Q1} = 0.230 mA. Since β >>1, the emitter current is essentially equal to the collector current, which is 0.230 mA.

The sum of Q1's emitter current and J1's drain current is the current flowing through R1, which is 3.3 mA.

Put in another way, the $I_{R1} = ID_{J1} + IE_{Q1}$

Also note that the current gain of Q1 (and Q2) is high with β >>1, which leads to $IE_{Q1} = IC_{Q1}$.

Therefore, $I_{R1} = ID_{J1} + IC_{Q1}$

By use of algebra,

$ID_{J1} = I_{R1} - IC_{Q1}$

I_{R1} = 3.3 mA and IC_{Q1} = 0.230 mA

Therefore, the drain current of J1,

ID_{J1} = 3.3 mA – 0.230 mA

ID_{J1} = 3.07 mA = drain current of J1.

Open loop gain of the charge amplifier is the transconductance of J1, g_{mJ1}, muliplied by R2 and K_1. The scaling factor K_1 represents the transfer of signal from the drain of J1 to Q1. There is a small amount of signal taken away from R1. Also we can approximate that the gain of emitter follower, Q2 = 1.

Open loop gain = g_{mJ1} x R2 x K_1

For an LSK170 biased at about 3 mA, g_{mJ1} = 15 mS = 15 mmho

R2 = 47KΩ

$K_1 = R1/[(R1) + (1/g_{mQ1})]$

Note that: $(1/g_{mQ1})$ = 0.026 volt/IC_{Q1} =0.026 volt/0.230 mA = 113Ω = $(1/g_{mQ1})$

K_1 = 1600Ω/[1600Ω + 113Ω] = 0.934

Open loop gain = g_{mJ1} x R2 x K_1 = 15 x 47 x 0.934 = 705 x 0.934 = 658.

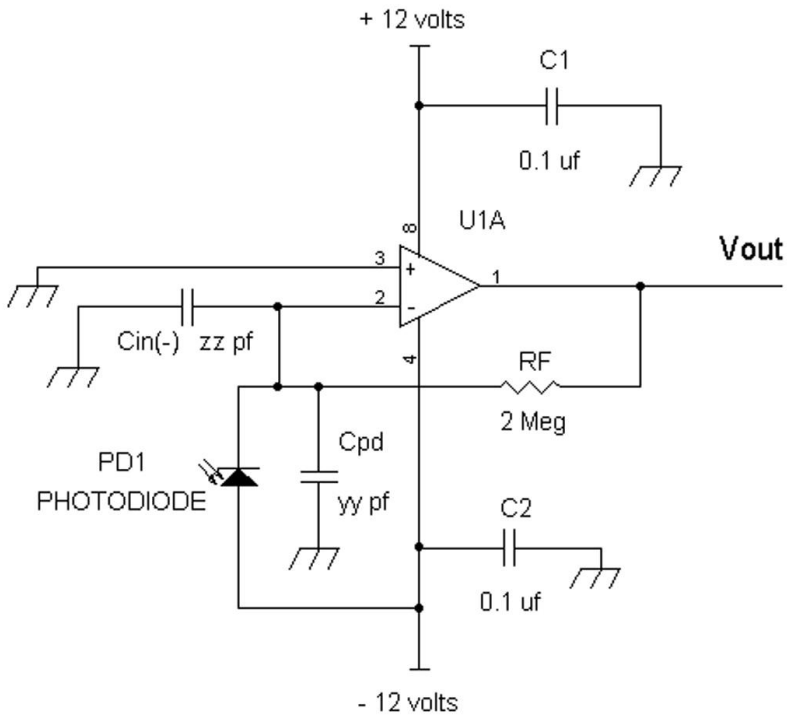
Note that Q2 form an emitter follower circuit and Q2 provides a low impedance output for Vout. Because there will be an offset voltage, DC blocking capacitors C7 and C8 are used.

Specific Applications
Photodiode Preamps

In some JFET op amps such as the AD743, the input capacitance is in the order of 18 to 20 pF. In comparison, with an LSK489 dual FET, the input capacitance is in the order of 3 pF, which will be suitable for low noise photodiode applications. In this section we will see why it is important to have low equivalent input noise and low input capacitance in a photodiode preamp. A simple photodiode is shown in Figure 8 below, which uses an op amp.

In the photodiode amplifier below, when light is shined onto the photodiode, current is generated by the photodiode, PD1. As configured with the cathode of PD1 connected to the (-) input terminal of U1, Vout generates a positive voltage proportional to the amount of light into the photodiode. Also shown in Figure 8 are the equivalent capacitances from the photodiode, Cpd, and (-) input terminal, Cin(-), which are connected in parallel. To minimize Cpd, the photodiode capacitance, the anode of PD1 is connected to the minus 12 volt power supply for maximum reverse bias to lower its junction capacitance. For example, if a BPV10 photodiode is used, Cpd is about 2.7 pF at 12 volts reverse bias. At a lower reverse bias voltage such as 1 volt, Cpd is about 7 pf.

Figure 8 - A simple photodiode transresistance amplifier



For low noise considerations, these two capacitances, Cpd and Cin(-), should be low as possible. The reason is that the equivalent input noise density voltage, Vnoise_input of the op amp will be amplified in the following manner at Vout, neglecting any noise current from the photodiode:

Vout_noise for a bandwidth of 1 Hz = (Vnoise_input) $\sqrt{1 + (\omega RFCt)^2}$ + $\sqrt{4kTRF}$ (1)

Where ω = $2\pi f$, RF = feedback resistor, k = 1.38 x10^{-23} Joules per degrees Kelvin, T = 298 degrees Kelvin

Ct = Cpd||Cin(-) = total capacitance at the (-) input terminal, and
Ct = Cpd + Cin(-)

$\sqrt{4kTRF}$ = thermal noise voltage of the feedback resistor RF for a bandwidth of 1 Hz.

As we can see from the equation above, the output noise, Vout_noise, goes higher if *Ct* is increased.

In designing a low noise transresistance preamps the goals are to:

1. Minimum equivalent input noise voltage. Equation (1) above shows that the output noise voltage is dependent on the equivalent input noise voltage, Vnoise_input.
2. Minimize noise current from the (-) input because the noise current at the input will form a noise voltage across the feedback resistor. Generally, a JFET is desirable for the (-) input because of its low gate noise current.
3. Minimize the capacitance from the (-) input to ground. The equation (1) shows that more noise is generated at the output when the capacitance, Ct = Cpd + Cin(-), at the (-) input terminal is increased.
4. Use as large value RF as possible. At first glance, it would appear increasing the resistance in RF would increase the output noise because of the resistor's thermal noise. This is true but the signal amplification from the photodiode is increased more so that results in a net increase in signal to noise ratio when RF is increased in value. For example, doubling the value in RF increases the resistor noise from RF by $\sqrt{2}$ = 1.41 while increasing the photodiode signal output voltage by 2. Thus, there is a net gain of $\sqrt{2}$ or + 3 dB, in terms of signal to noise ratio in this example.

In Figure 8, the typical input capacitance, Cin(-) at the (-) input of an FET op amp is about 18 pf. To lower the capacitance of the op amp, a low capacitance and low noise JFET is used as a buffer or source follower to the (-) input. See Figure 9 on the following page.

A low noise JFET such as an LSK189 is configured as a source follower, with a source biasing resistor R3. In terms of input capacitance at the gate of J1 with an LSK189, it is about 3 pF from the gate to the drain, which is much less than the 18 pF of Cin(-). Capacitance between the gate and ground due to the gate to source capacitance approaches zero. This is because the source follower configuration provides substantially the same AC voltage at the gate and at the source, which substantially cancels out the capacitance between the gate and the source. The source follower also greatly reduces the capacitance seen at the gate to ground even when the source is driving signal into a capacitive load, Cin(-), the capacitance at the (-) input terminal of the op amp U1A.

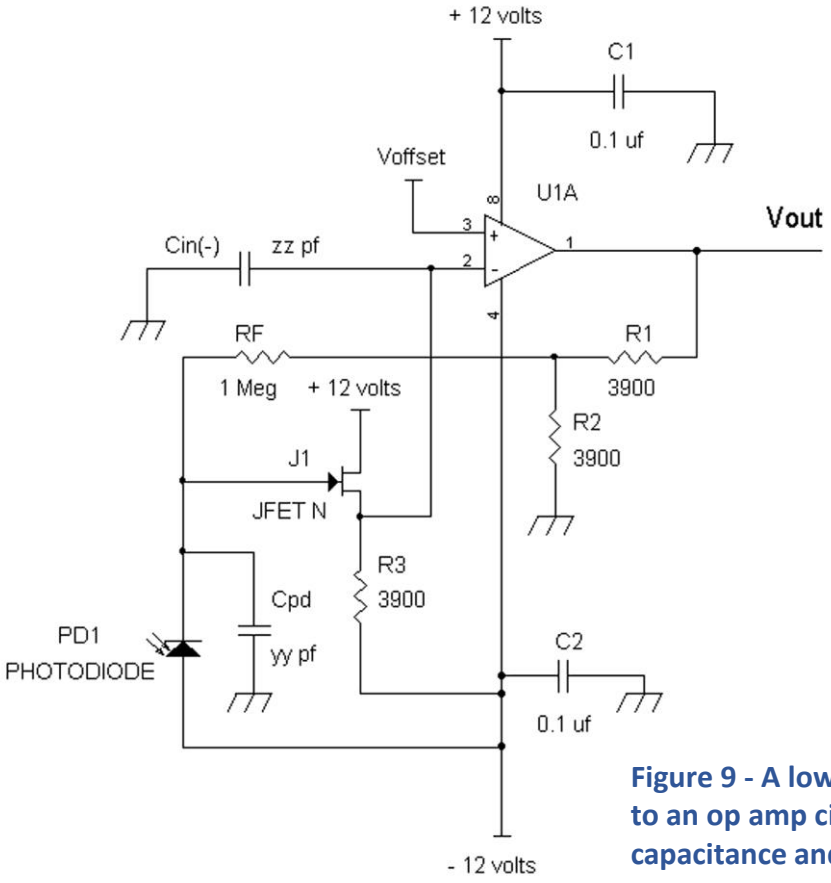


Figure 9 - A low capacitance JFET added to an op amp circuit to lower input capacitance and reduce noise

It should be noted that the source follower circuit may add some phase shift to the overall amplifier circuit. To ensure phase margin and no oscillations, a resistive divider R1 and R2 is used. With the values given at 3900Ω for R1 and R2, the equivalent feedback resistance is [1 + (R2/R1)] x RF = 2 x 1MΩ = 2MΩ, the same resistance value shown in Figure 8 for RF.

If the (+) input of the op amp in Figure 9 is grounded, such that Voffset = 0 volts, Vout will most likely have a DC offset. To "zero" Vout when there is no signal from the photodiode, a clean DC voltage, Voffset may be applied to the (+) input of U1.

Op amp U1A = AD797 has an equivalent input noise voltage of 0.9 nV/$\sqrt{Hz}$ and J1 =LSK189 with an equivalent input noise voltage of 1.8 nV/$\sqrt{Hz}$, the total equivalent input noise voltage is about 2.0 nV/$\sqrt{Hz}$. This is lower than a very low noise JFET op amp such as an AD743 that has 3.2 nV/$\sqrt{Hz}$. Note that bipolar input stage op amps AD797 with 0.9 nV/$\sqrt{Hz}$ has lower equivalent input noise voltage than 2.0 nV/$\sqrt{Hz}$, but the AD797's input noise current is too high and are not suitable for amplifier circuits with large value feedback resistors (RF) in the MΩ such as the circuit shown in Figure 8.

Note that J1 may be substituted with an LSK170 (0.9nV/$\sqrt{Hz}$) if a slight increase in capacitance from the gate to ground is acceptable. This FET has about half the equivalent input noise of the LSK189.

Specific Applications

Extending the Frequency Response of a Transresistance Amplifier

In transresistance amplifiers, a feedback resistor will have a capacitance, CF, across its leads. This capacitance will reduce the bandwidth of the output signal at high frequencies. See Figures 10(a) and 10(b) below.

Figure 10(a) shows a photodiode preamp with Ct = Cpd + Cin(-), and CF a capacitor across the feedback resistor RF. CF can be the internal parasitic capacitance from resistor RF, or it can be capacitor often connected across RF to add positive phase shift that offsets the negative shift from Ct. This added positive phase shift due to CF ensures stability in the photodiode preamp. However, one side effect from CF is reducing the bandwidth of the amplified photodiode signal at Vout.

The -3 dB bandwidth at Vout is $1/[2\pi(RF)(CF)] = f_{-3dB}$
For example, RF = 2MΩ and CF = 1pF, then $f_{-3dB} = 1/[2\pi(2M\Omega)(1pF)] = 79.6$ kHz
One way to reduce the effects this roll off in frequency response is to make RF a series connection of ten 200KΩ resistors. If CF is still 1pF, the new bandwidth will be: $f_{-3dB} = 1/[2\pi(200K\Omega)(1pF)] = 796$ kHz

However, there is another alternative and that is to equalize the frequency response as shown in Figure 10(b).

Figure 10(a) - Simple preamp.

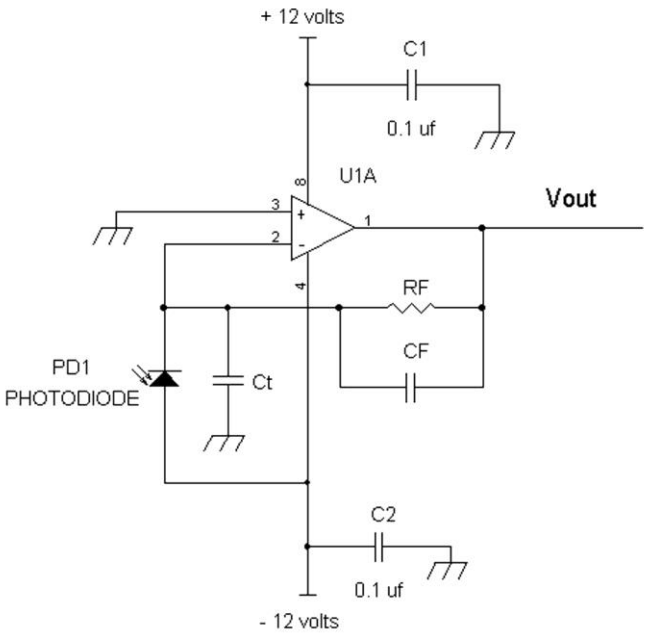
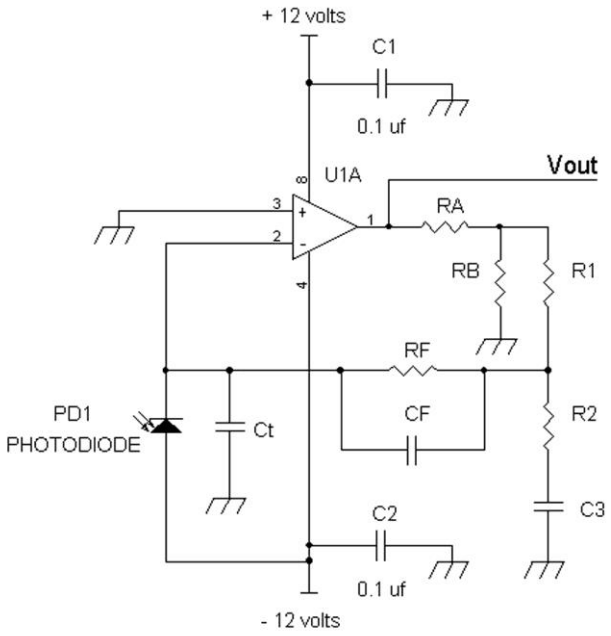


Figure 10(b) - Simple preamp with equalization.



For now, let's assume that that op amp U1A in Figure10(b) has sufficient phase margin to not oscillate when RA = 0Ω, and when RB = open circuit or removed.

If (R1 + R2)(C3) = (RF)(CF) there will be a "boost" that compensates for the roll-off. When the boost ends is determined by the (R2)(C2) time constant. The amount of bandwidth extension is [1+ (R1/R2)]. Generally there is a limit on bandwidth extension. If R2 → 0Ω, then C3 is grounded and forms a low pass filter and lagging phase shift network with R1, that will most likely cause oscillation.

Generally, it is recommended to start with R2 = 33% of R1, which gives a bandwidth extension of [1 + (R1/0.33R1)] = [1 + 3] = 4 = bandwidth extension.

For example, if RF= 2MΩ and CF = 1pF, we want R1 <<RF, so let's make R1 = 10KΩ and R2 = 3.3KΩ, then (R1 + R2)(C3) = (RF)(CF) or (10KΩ + 3.3KΩ)(C3) = (13.3KΩ)(C3) = (2MΩ)(1pF), or

C3 = (2MΩ)(1pF)/(13.3KΩ) = 150 pf = C3. With these values, the frequency response will increase from 79.6 kHz to about 318 kHz for Figure 10(b).

Note: Often the op amp U1A may require voltage divider resistors RA and RB to ensure sufficient phase margin so that the amplifier in Figure10(b) does not oscillate. Typically, start out with a voltage divider of 2 or more. That is, (RA/RB) ≥ 1. Also, it is recommended that RA||RB ≤ 500Ω and that RA||RB << R1.

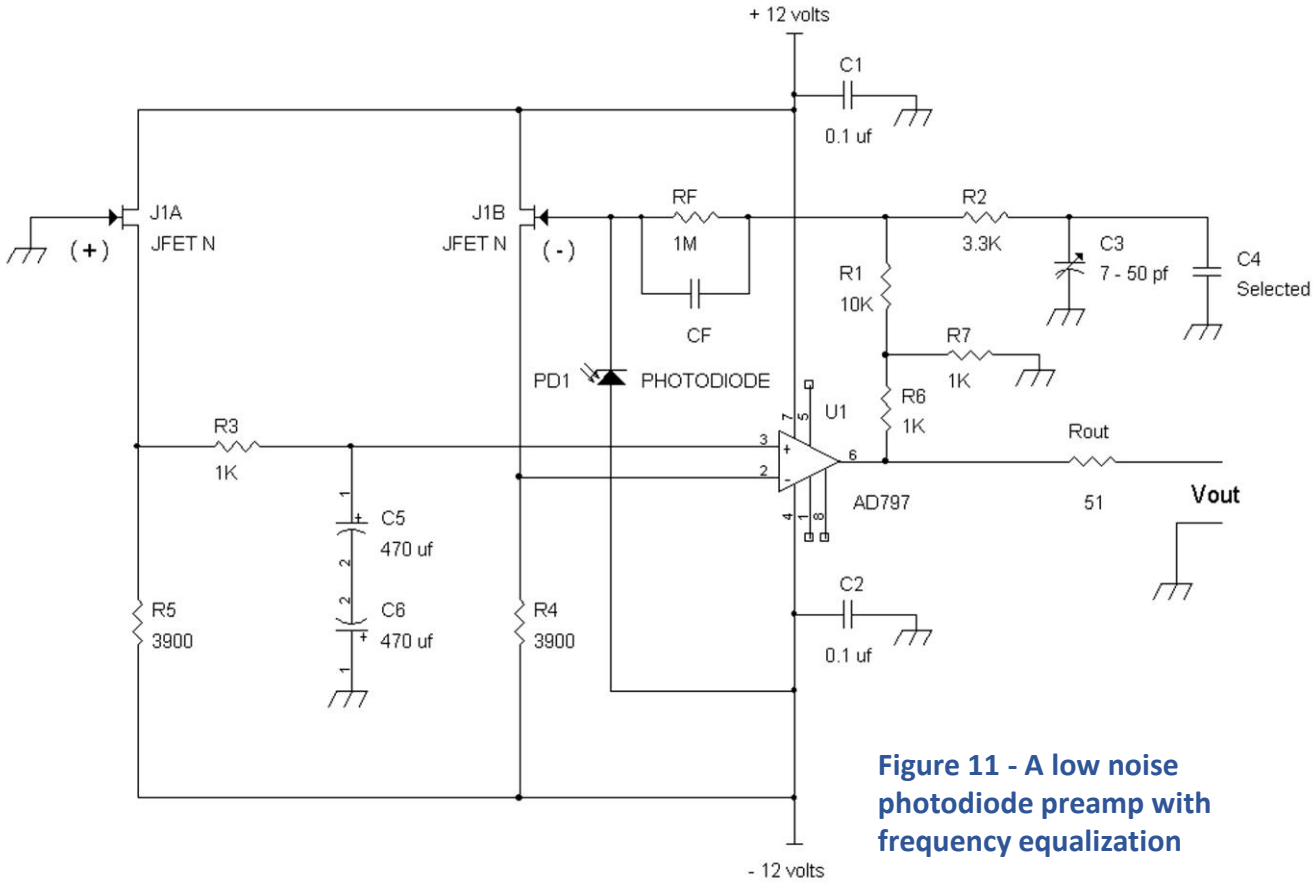


Figure 11 - A low noise photodiode preamp with frequency equalization

In Figure 11 on the previous page, the effective feedback resistor is about 2MΩ because R6 and R7 provide a divide by two voltage divider. The effective feedback resistance is [1 + (R6/R7)] x RF = [1 +1] x 1MΩ = 2MΩ, given that R1 << RF or 10KΩ << 1MΩ.

J1A and J1B are low noise and low capacitance matched pair JFETs such as the LSK489.

U1 can be typically a bipolar input stage op amp for the lowest equivalent input voltage noise density such as the AD797. Variable trimmer capacitor C3 is adjusted for the flattest frequency response.

Alternatively C3 may be adjusted for the best pulse response. Generally an LED is driven with a square wave signal and is pointed into the photodiode PD1. C3 is adjusted for the fastest rise and fall times while avoiding overshoot at Vout.

In Figure 11, R6 and R7 form a voltage divider to multiply RF for an effective resistance of 2MΩ. But R6 and R7 also adds some series resistance to R1. This series resistance is R6||R7 = 1KΩ||1KΩ = 500Ω, which is the Thevenin resistance from the voltage divider circuit. To calculate the proper time constants for frequency compensation we have:

[(R6||R7) + (R1 + R2)] x [C3 + C4] = RF x CF which leads to:

[C3 + C4] = [RF x CF]/ [(R6||R7) + (R1 + R2)]

For example, in Figure 11, suppose CF = 2.2 pF is the capacitance across RF = 1MΩ.

Also U1 = AD797

[C3 + C4] = [1MΩ x 2.2 pF]/ [(500Ω) + (10KΩ + 3.3KΩ)]

[C3 + C4] = [1MΩ x 2.2 pF]/ [(500Ω) + (13.3KΩ)]

[C3 + C4] = 72.46 x 2.2 pF = 159 pF

Let C4 = 130 pF so that the remaining 29 pF can be set by variable capacitor C3. Note that C3 is adjusted for best transient or frequency response.

The circuit was built with and without the equalization network, R1, R2, C3, and C4. Without the equalization network and with CF = 2.2 pF, the – 3 dB measured frequency response was about 71 kHz which matches closely to [1/2π(1MΩ)(2.2 pF)] = 72.5 kHz. The bandwidth extension is [1 + (R1/R2)] = [1 + (10K/3.3K)] = [1 +3] = 4. Thus, we will expect the frequency response to be extended to 4 x 72.5 kHz = 290 kHz. With the equalization network and C4 adjusted, the measured frequency response was extended to > 300 kHz.

Note: When an LT1028 op amp was used instead of the AD797 for U1, R7 had to be reduced to 100Ω to avoid oscillation and to provide sufficient phase margin. Not all op amps will necessarily have the enough phase margin to ensure an oscillation free condition with R6 = R7 in Figure 11. At times R7 may have to be lowered in value for stability, but also keep in mind that the effective feedback resistance is RF x [1 + (R6/R7)].

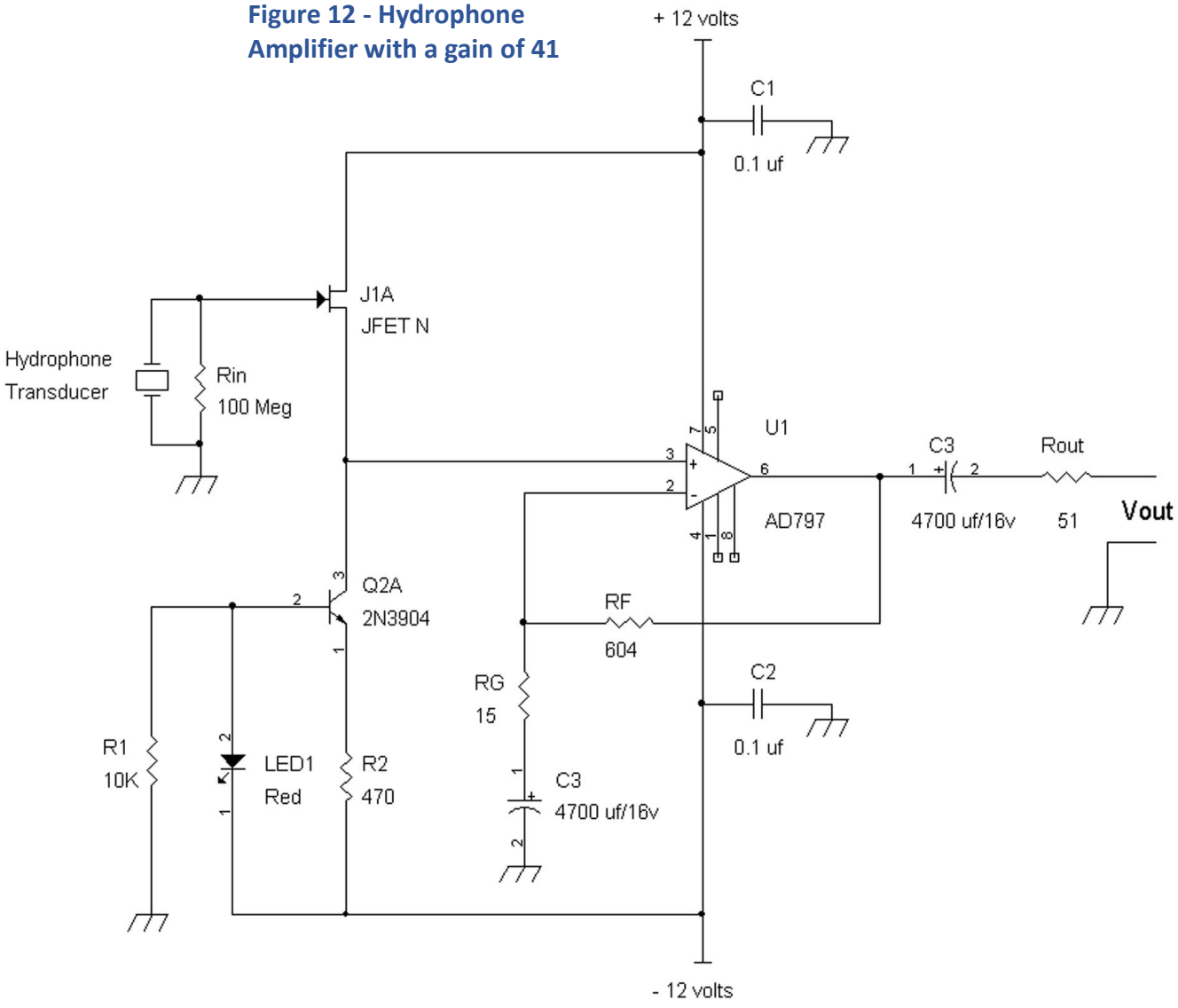
Specific Applications

Hydrophone Voltage Gain Amplifier

Figure 12 shows an example with a hydrophone amplifier.

In some instances, piezoelectric elements can be amplified with a low noise voltage amplifier instead of a charge amplifier. In this case a hydrophone transducer or microphone is connected to a source follower circuit J1A and current source Q2A. J1A can be an LSK170 for the lowest noise. Current source circuit R1, LED1, R2, and Q1A may be replaced with a 3900Ω resistor from the source of J1A to – 12 volts.

Figure 12 - Hydrophone Amplifier with a gain of 41



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2) Columbia Research Laboratories, General Purpose Accelerometers, Models 3021,3022, 3023, 5001, and 5002.
3) Columbia Research Laboratories, Dynamic Pressor Sensors, Models P-308-C, P-766, 765M25, and 765M27.
4) Kistler Instrument Corporation, Quartz High Resonant Frequency, Charge Mode, Shock Accelerometer, Type 8044.
5) Analog Devices, Data Sheet, AD797.
6) Analog Devices, Data Sheet, AD743.
7) Linear Technology, Data Sheet, LTC6078.
8) Linear Technology, Data Sheet,LT1028.
9) Vishay Semiconductors, Data Sheet, BVP10 Silicon PIN Photodiode.

LINEAR SYSTEMS

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LINEAR SYSTEMS'

J201

HIGH GAIN N-CH JFET

Linear Systems' products enable customers to build the lowest-noise signal chains possible.

The J201 N-channel JFET is optimized for high gain. The part is particularly suitable for use in low power or high impedance amplifiers.

J201 Benefits:

1. High Input Impedance
2. Low Cutoff Voltage
3. Low Noise

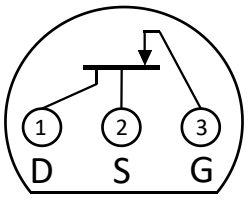
J201 Applications:

1. Battery Powered Amplifiers
2. Anti-polarization Circuit For Sensors
3. Audio Pre-Amplifiers
4. Infra-Red Detector Amplifiers
5. Phase Shift Oscillator
6. Current Limiter
7. Low frequency noise requirements for both low and high source impedance circuits

Package Figure 1.

The J201 is available in the TO-226 (TO-92) plastic package and TO-236 (SOT-23) package. The J series TO-226 package provides low cost, while the SST series, TO-236 (SOT-23) package provides surface-mount capability. Both the J and SST series are available in tape-and-reel for automated assembly and in die form.

TO-92 (3L)
Top View



SOT-23 (3L)
Top View

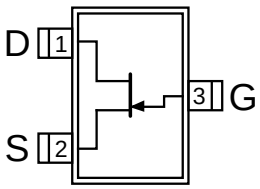


Figure 1.

JFET designs are suitable for battery operated circuits, therefore JFETs are used in guitar, audio and MIC preamps and cable boosters. Some of the designs can be compressed further, eliminating certain components if space is an issue and there is minimal impacts on the behavior of the circuit. The voltage battery is 6 volts as. Since the batteries are small in size, they can easily fit in a small package. Button batteries are not recommended. The circuits are all preamplifiers that do not drive power amplifiers or lines, but for a better signal for the power amplifier. The voltage drain to source is around 4.5V.

Characteristics

N-Channel JFETs have either or both constant voltage or self-bias configurations. The best consistent performance is to have a configuration that uses constant voltage and/or self-bias. The combination of both biasing schemes is the best approach that does not decrease the dynamic range and has low value gain fluctuation.

The J201 Series JFET is an N-Type material sandwiched between two layers of electrically connected P-Type material. The N-Type material is the "GATE" and the P-Type material ends are "Drain" and "Source". Drain and source ends are interchangeable.

Figure 2. shows the N-Channel JFET Characteristics Curve.

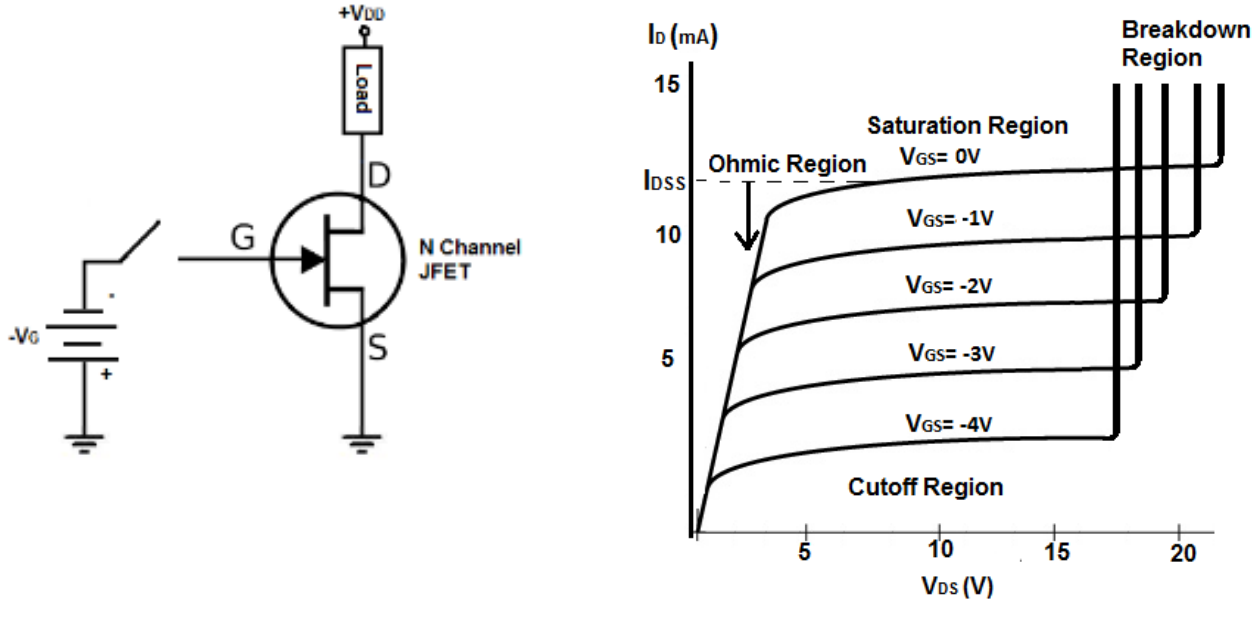


Figure 2.

In order to turn on the N-Channel JFET, a positive voltage +VDD is applied to the drain terminal. The current will flow through the drain-source channel. If the gate voltage, VG, is 0V, the drain current is at its largest value.

If the bias positive voltage, VDD, which powers the drain, is removed then the JFET will turn off. If the bias voltage is not removed, but a negative voltage is applied to the gate, the drain current is reduced. The more the gate voltage, VG, becomes negative, the less the current is until cutoff, which is when the JFET is in the OFF region.

The gain of the JFET decreases as the negative voltage to the gate increases. The current ID output by the transistor, is highest when the voltage fed to the gate terminal is 0V.

Amplification

The J201 Series has very high input impedance and it isolates previous stages from previous stages. The output of the previous stage appears at the input of the next stage because of the low output impedance of the previous stage. Therefore the JFET is used in boosters or amplifications and are capable of driving heavy load or small load resistances.

FETs are low noise devices and are useful component to be used as an amplifier at the receiver front-end as one needs the minimal amount of noise at the final output. Furthermore JFETs are voltage controlled devices and are ideal to be used in Radio Frequency (RF) amplifiers.

The circuit in **Figure 3.** is a pre amp and a buffer. The JFET is biased, and the input signal is AC biased.
If an audio signal is fed in the input "I", the signal at "out" would be a volume.

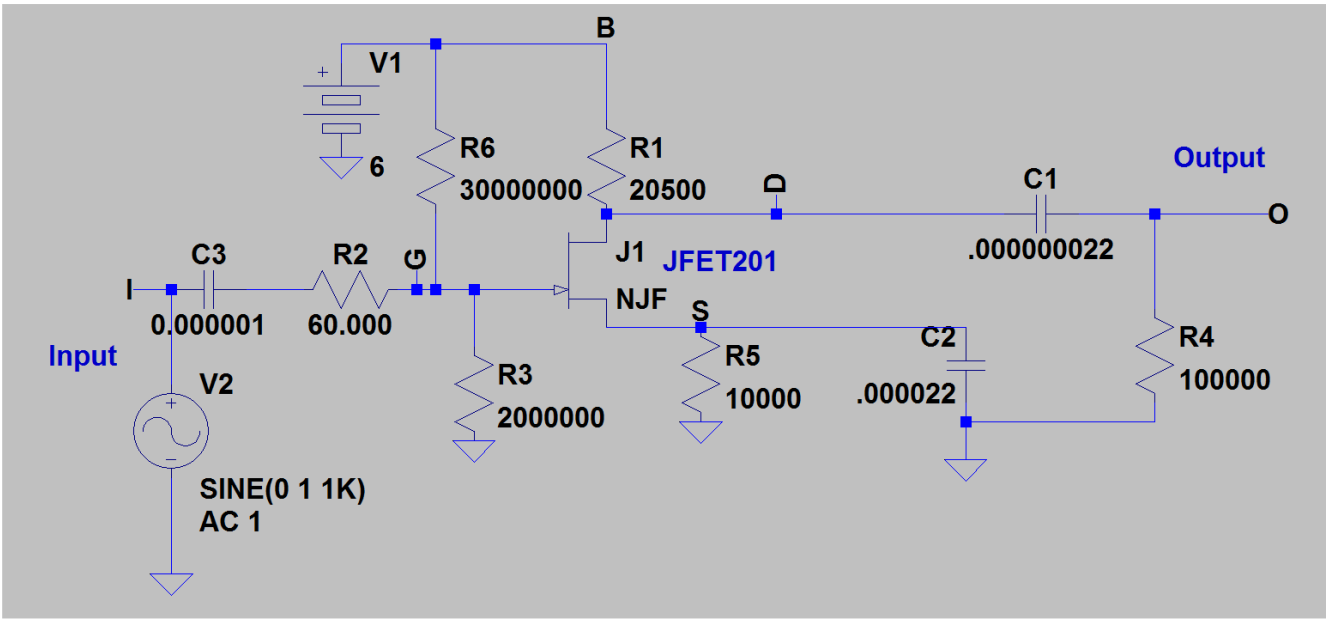


Figure 3.

Figure 4. is the simulation results using a spice software that shows the various waveforms at various points in the circuit including input voltage and current and output voltage waveforms. The input impedance is very high, the combination of R6 and R3.

The circuit in **Figure 5.** is similar to the previous one but the JFET is not biased

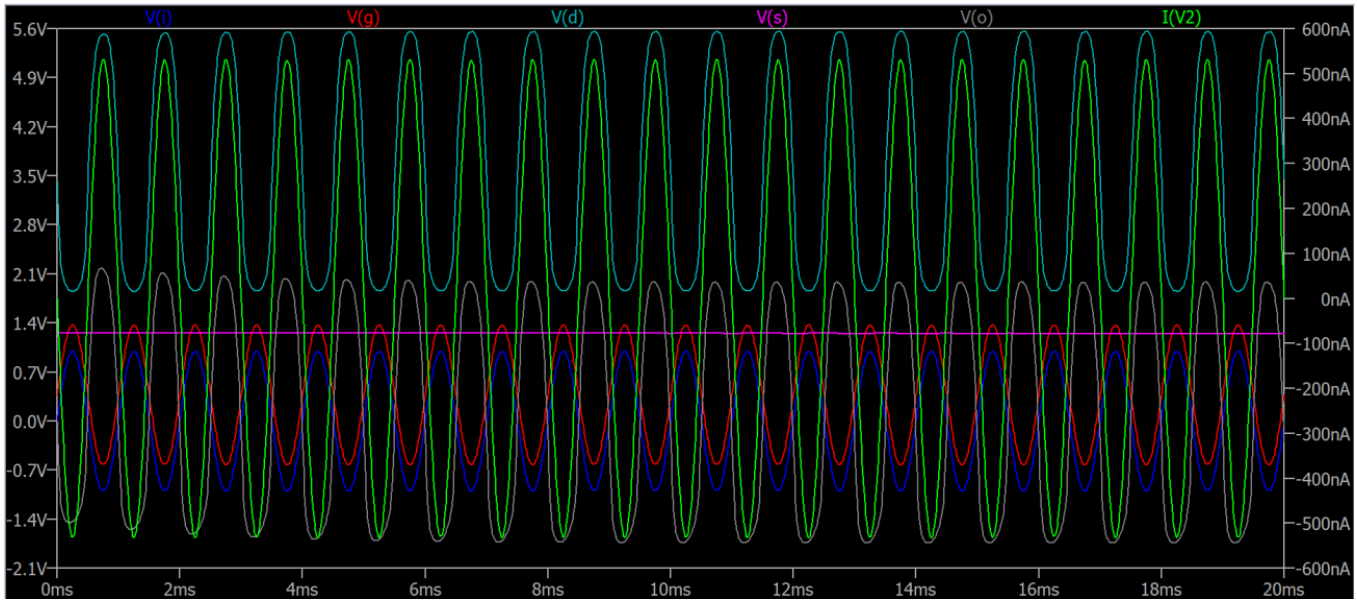


Figure 4.

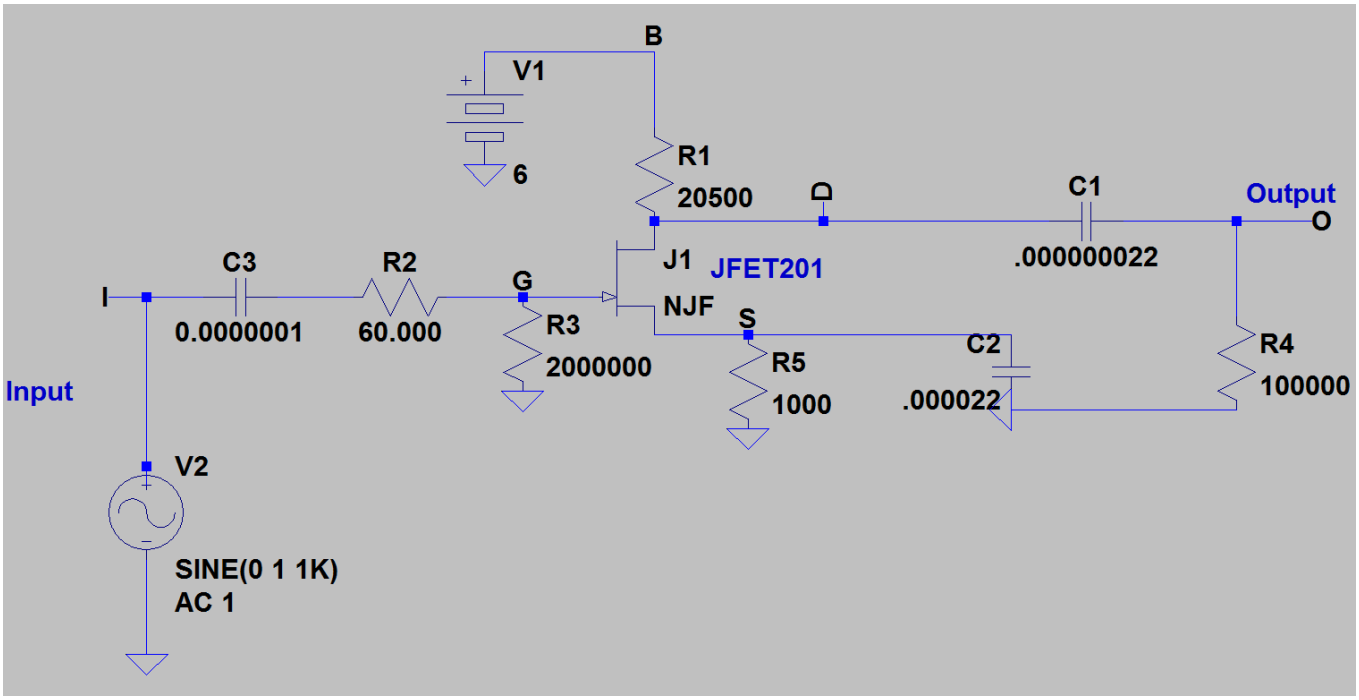


Figure 5.

The simulation waveforms in **Figure 6.** are in the following drawing. In the plot you can notice the waveforms at various points in the circuit including input and output voltage waveforms. The input waveform is a 1V Peak to Peak and I KHz frequency for both circuits. Small signals are even less than that in preamp circuits.

The waveform of the output voltage is similar in both circuits in frequency and voltage. The only difference is the DC offset of the waveform as a result of biasing.

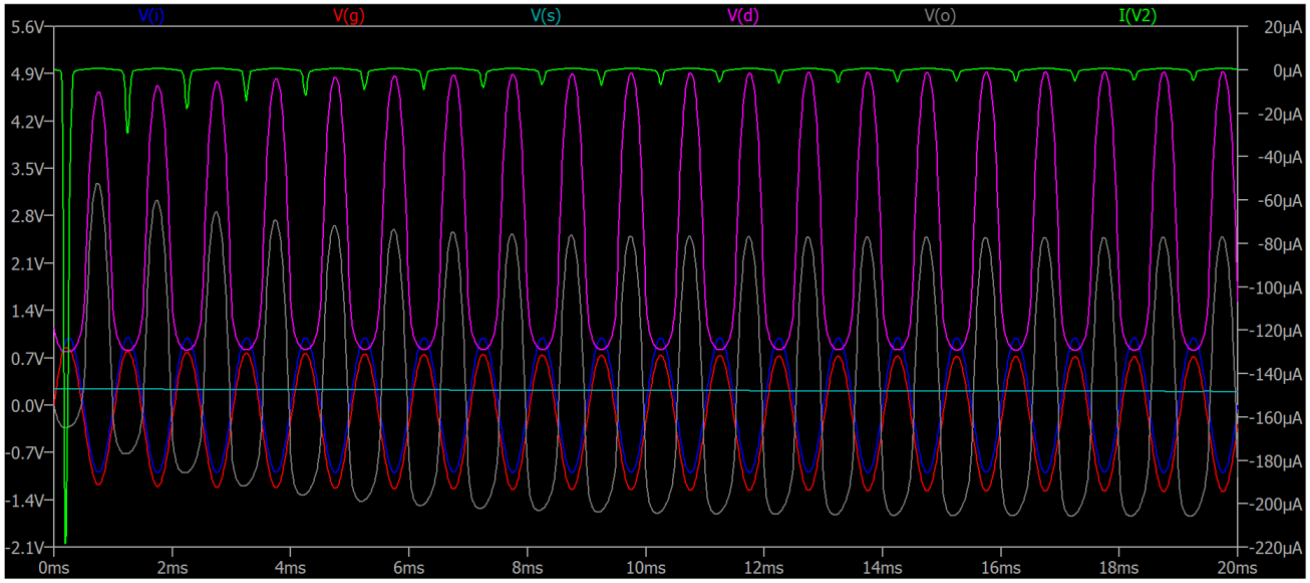


Figure 6.

The circuit in **Figure 7.** is a switch, the switch can be a manual switch or a pedal that would pass through the signal when the switch is connected.

Switch

JFET is essentially a voltage controlled resistor. The "ON" state resistance is low while the "OFF" state resistance is extremely very high. Thus JFETs are used as switches.
The gate junction is reverse biased and there is no current flow through the device and hence is the extremely high input impedance characteristic of JFET devices.

JFET devices are controlled in the depletion mode by removing or depleting charge carriers from the n-channel. The amount of depletion depends on the Gate voltage. When the Gate is made more negative, the current flow for a given value of Source-to-Drain voltage is reduced. Modulating the Gate voltage modulates the current flow through the device. That is essentially is a switch behavior and the output signal of the JFET is a copy of the input signal.

When the Gate-Source voltage, VGS is zero, n-channel FET will operate in saturation region and behave almost as a short circuit and the output voltage will be zero. When the voltage between gate and source is negative then the FET is in its cut-off or pinch-off region which means there is practically no channel and the FET acts like an open circuit with the drain current, ID is equal to zero.

The signal at the gate has to be AC coupled in order to remove the DC component or bias and allow the NJFET to operate as a switch. The RC time of the capacitor and the resistor at the switch determine the delays of the switch from one state to the other.

In order to turn off the switch and not let signal through, the switch or pedal is flipped and that causes the gate to be more negative than the drain and source and getting it close to 0V, the diode is reversed biased, not conducting, and guarantees that the gate is off. In order to turn the switch on and let the signal through the gate voltage is around 0 V or ground, the diode in this case is forward biased and conducting.

Switching time is dependent on gate capacitance. When the control voltage goes low, the gate capacitance is rapidly discharged through the diode, which is very low impedance when conducting. When the control voltage goes high, cutting off the diode, the gate has to recharge through the resistor, which is a much longer time constant.

The switch voltage is the battery voltage of 6V. The current of the input signal is represented also. The input signal is sinewave of 1V amplitude.

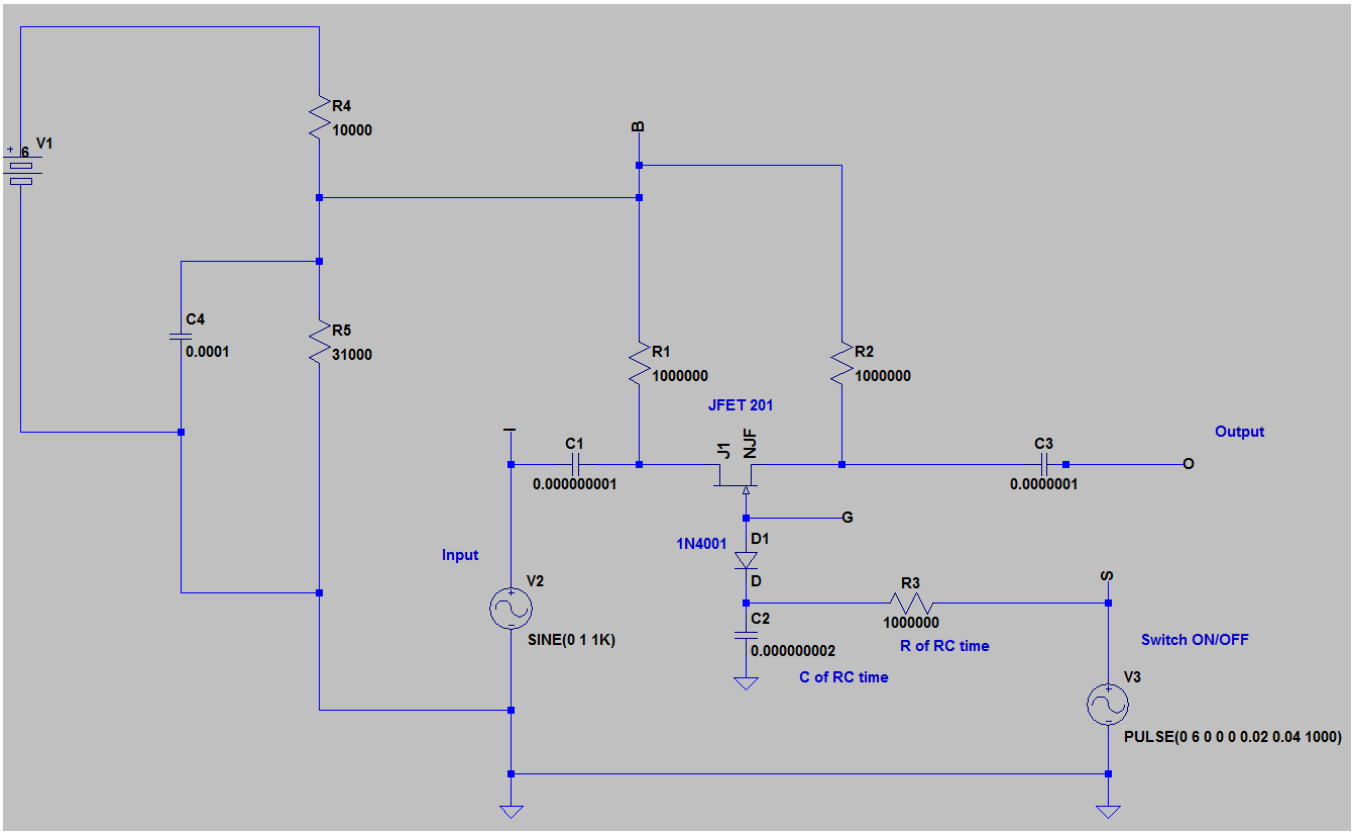
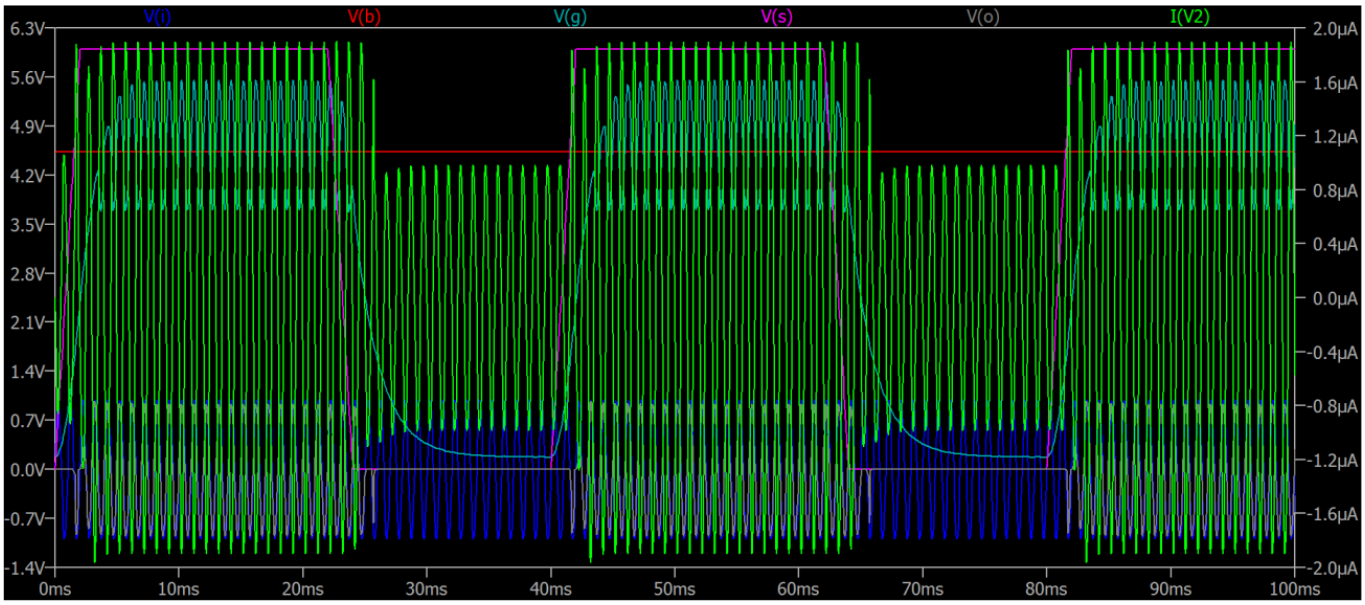


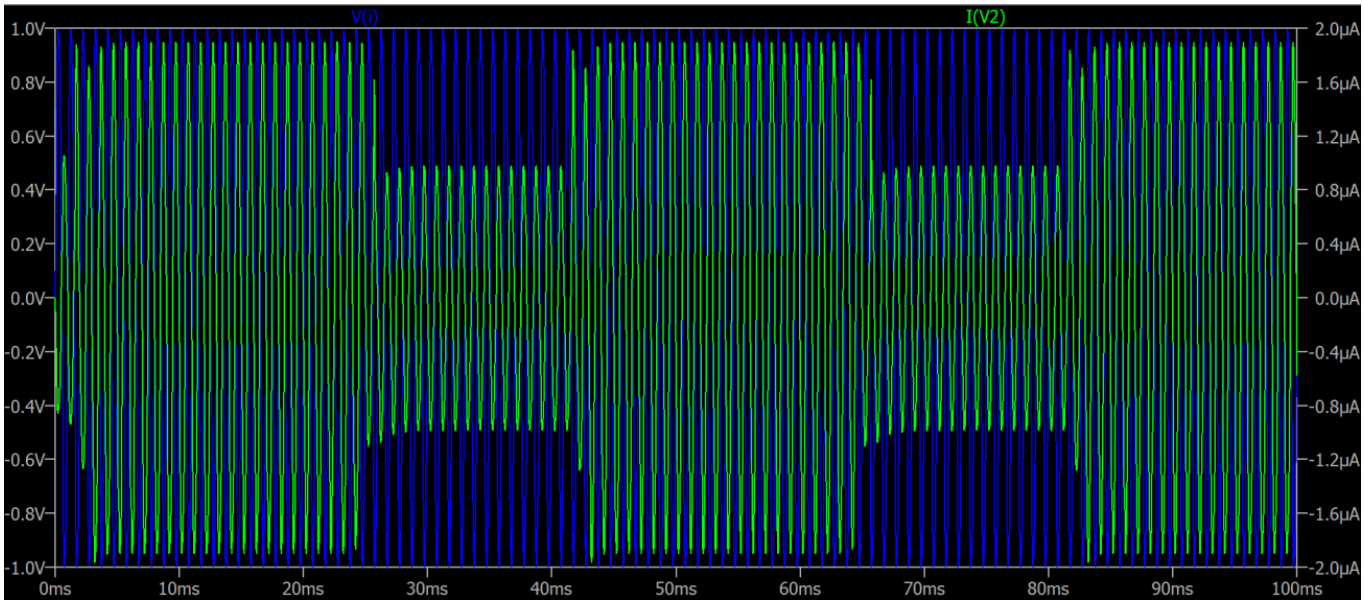
Figure 7.

The waveforms are represented in several plots for clarities. Signal waveforms do not have the same color in the various plots.

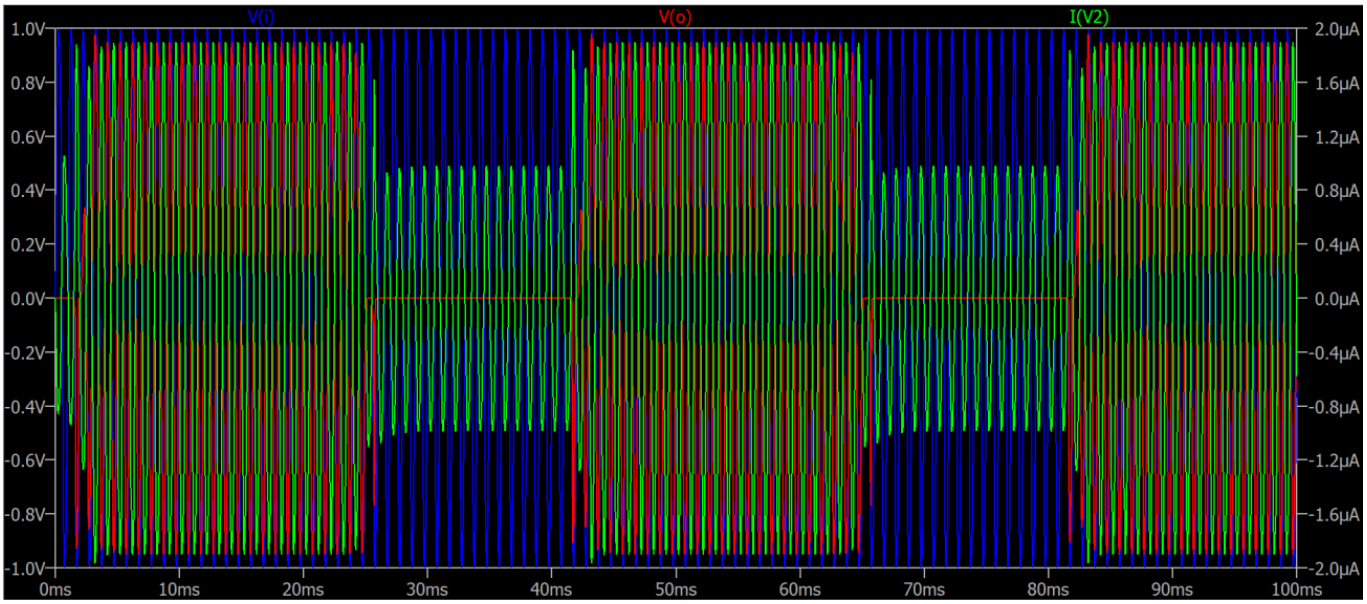
The switch is waveform S, when it is connected or high, the input signal is passed through with delay. When the switch is off, open, then the input waveform is not passing through to the output.



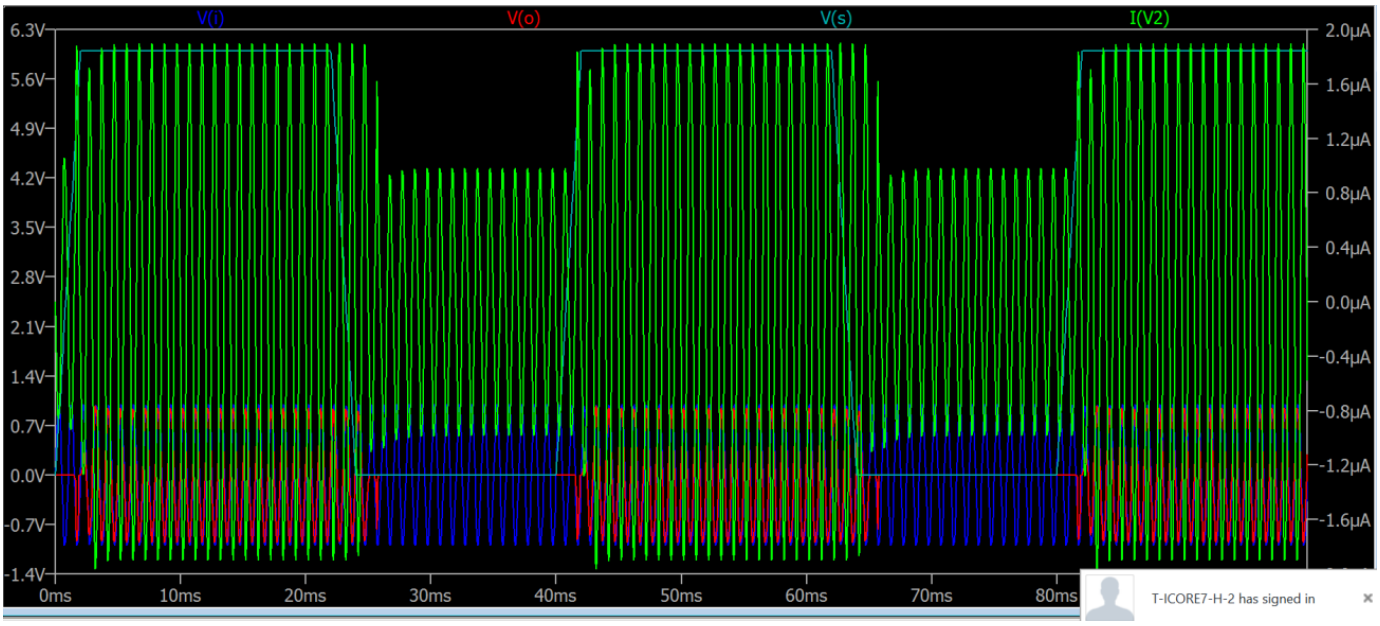
The next waveform plot is the current and voltage of the input signal. It is a sine wave in blue color.



The next plot is showing the output signal in red. The output signal is a copy of the input signal when the switch is connected.



The next plot shows the switch waveform in Turquoise color. The output signal in red is not a copy of the input signals, it is constant, when the switch, green waveform is low or disconnected.



LINEAR SYSTEMS

Quality Through Innovation Since 1987

HIGH-SPEED DMOS **FET ANALOG SWITCHES** AND SWITCH ARRAYS

Introduction

This Application Note describes in detail the principle of operation of the SD210/5000 series of high-speed analog switches and switch arrays. It contains an explanation of the most important switch characteristics, application examples, test data, and other application hints.

Description

The Linear Systems SD210 and SD5000 series are discretes and quad monolithic arrays, respectively, of single-pole single-throw analog switches. These switches are n-channel enhancement-mode silicon field effect transistors built using double-diffusion MOS (DMOS) silicon gate technology. Surface mount versions (SST211, SD5400 Series) are also available.

This family of devices is designed to handle a wide variety of video, fast ATE, and telecom analog switching applications. They are capable of ultrafast switching speeds (tr = 1 ns, tOFF = 3 ns) and excellent transient response. Thanks to the reduced parasitic capacitances, DMOS can handle wideband signals with high off-isolation and minimum crosstalk.

The SD210 series of single-channel FETs is produced without Zener protection to reduce leakage and in Zener protected versions to reduce electrostatic discharge hazards. The SD5000 series is available in 16-lead dual inline surface mount or sidebraze ceramic packages. Analog signal voltage ranges up to ±10 V and frequencies up to 1 GHz can be controlled.

For surface-mount applications the SST211 series is offered in the TO-253 (SOT-143) package. The SD5400 series comes in the narrow body gull-wing SO-14 package.

Applications

Fast switching speeds, low on-state resistance, high channel-to-channel isolation, low capacitance, and low charge injection make these DMOS devices especially well suited for a variety of applications.

A few of the many possible application areas for DMOS analog switches are as follows:

1. Video and RF switching (high speed, high offisolation, low crosstalk):
    -Multiple video distribution networks
    -Sampling scanners for RF systems

2. Audio routing (glitch- and noise-free):
    -High-speed switching
    -Audio switching systems using digitized remote control

3. Data acquisition (highspeed, low charge injection, low leakage):
    -High-speed sample-and-holds
    -Audio and communication A/D converters

4. Other:
    -Digital switching
    -PCM distribution networks
    -UHF Amplifiers
    -VHF Modulators and Double
    -Balanced Mixers
    -High-speed inverters/drivers
    -Switched capacitor filters
    -Choppers

Principle of Operation

Figure 1 depicts an n-channel enhancementmode device with an insulated gate and asymmetrical structure. The gate protection Zener is shown with broken lines to indicate that, although it is present on the chip, it is not a main constituent of the fundamental switch structure.

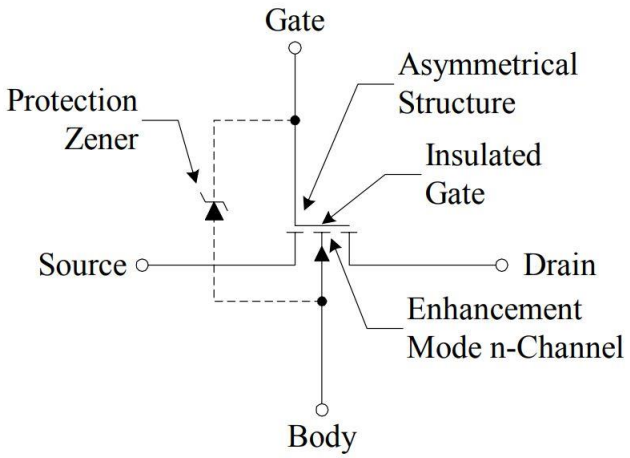


Figure 1. DMOS Electrical System

The DMOS field-effect transistor (FET) is normally off when the gate-to-source voltage (VGS) is 0 V. The lateral DMOS transistor, shown in cross-section in Figure 2, has three terminals (source, gate, and drain) on the top surface and one (the body or substrate) on the bottom. A Zener diode with a breakdown voltage of approximately 40 V is added to protect the gate against overvoltage and electrostatic discharges.

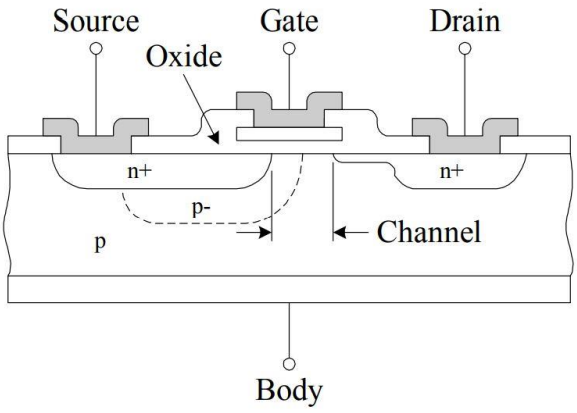
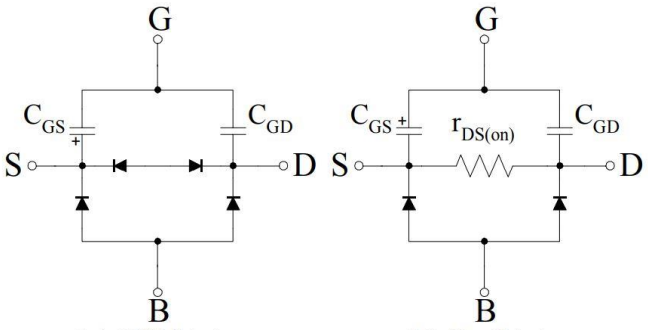


Figure 2. Cross Sectional View of an Idealized DMOS Structure

The double-diffusion process creates a thin self-aligning region of p-type material, isolating the source from the drain region. The very short channel length that results between the two junction depths produces extremely low source-to-drain and gate-to-drain capacitances at the same time that it provides good breakdown voltages.

When the gate potential is equal to or negative with respect to the source, the switch is off. In this state, the p-type material in the channel forms two back-to-back diodes and prevents channel conduction (Figure 3a). If a voltage is applied between the S and D regions, only a small junction leakage current will flow.



(a) Off State **(b) On State**

Figure 3. Equivalent Circuits

The silicon oxide insulation present between gate and source forms a small capacitor that accumulates charge.

If the gate-to-source potential (VGS) is made positive, the capacitive effect attracts electrons to the channel area immediately adjacent to gate oxide. As VGS increases, the electron density in the channel will exceed the hole density, and the channel will become an n-type region. As the channel conductivity is enhanced, the n-n-n structure becomes a simple silicon resistor through which current can easily flow in either direction.

Figure 4 shows typical biasing for ±10 V analog signal processing. Note that the drain is recommended for the output. Since CGD < CGS this causes less charge injection noise on the load.

As can be seen from Figures 3a and 3b, the body-source and body-drain pn junctions should be kept reverse biased at all times-otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to V-.

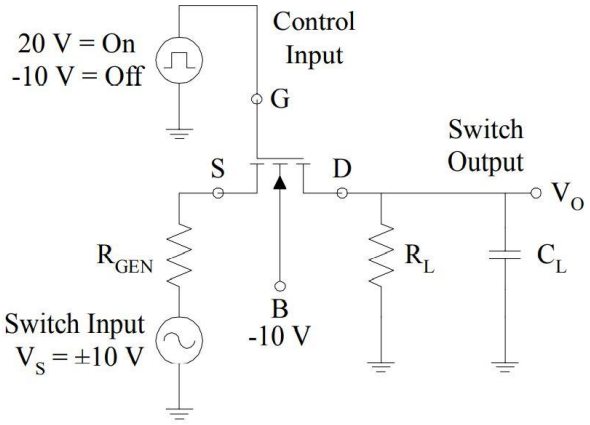


Figure 4. Normal Switch Configuration for a ±10 V Analog Switch

Main Switch Characteristics

rDS(on)

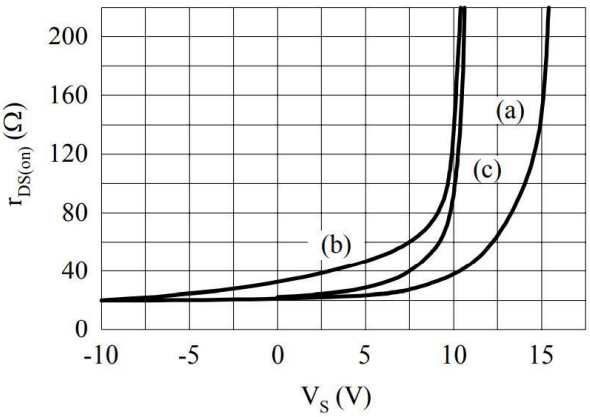
Channel on-resistance is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When VGS exceeds the threshold voltage (VGS(th)), the FET starts to turn on.

Numerous applications call for switching a point to ground. In these cases the source and substrate are connected to ground and a gate voltage of 3 to 4 V is sufficient to ensure switching action.

With a VGS in excess of +5 V, a low resistance path exists between the source and the drain.

The circuit shown in Figure 4 exhibits the rDS(on) vs. analog signal voltage relationship shown in Figure 5.

When the analog signal excursion is large (for example ±10 V) the channel on-resistance changes as a function of signal level. To achieve minimum distortion, this channel onresistance modulation should be kept in mind, and the amount of resistance in series with the switch should be properly sized. For instance, if the switch resistance varies between 20 Ω and 30 Ω over the signal range and the switch is in series with a 200 Ω load, the result will be a total ΔR = 4.5 %. Whereas, if the load is 100 kΩ, ΔR will only be 0.01 %.



(a) V_{BODY} = -10 V, V_{GATE} = 20 V
(b) V_{BODY} = -10 V, V_{GATE} = 15 V
(c) V_{BODY} = 0 V, V_{GATE} = 20 V

Figure 5. On Resistance Characteristics

Figure 4 shows typical biasing for ±10 V analog signal processing. Note that the drain is recommended for the output. Since CGD < CGS this causes less charge injection noise on the load. As can be seen from Figures 3a and 3b, the body-source and body-drain pn junctions should be kept reverse biased at all times-otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to V-.

Threshold Voltage

The threshold voltage (VGS(th)) is a parameter used to describe how much voltage is needed to initiate channel conduction. Figure 6 shows the applicable test configuration. In this circuit, it is worth noting, for instance, that if the device has a VGS(th) = 0.5 V, when V+ = 0.5 V, the channel resistance will be:

$$R_{CHANNEL} = \frac{0.5V}{1\mu A} = 500k\Omega$$

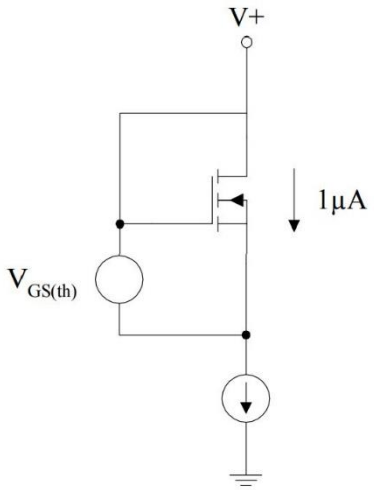


Figure 6. Threshold Voltage Test Configuration

Body Effect

For a MOSFET with a uniformly doped substrate, the threshold voltage is proportional to the square root of the applied source-to-body voltage. The SD5000 family has a non-uniform substrate, and the VGS(th) behaves somewhat differently. Figure 7 shows the typical VGS(th) variation as a function of the source-to-body voltage VSB.

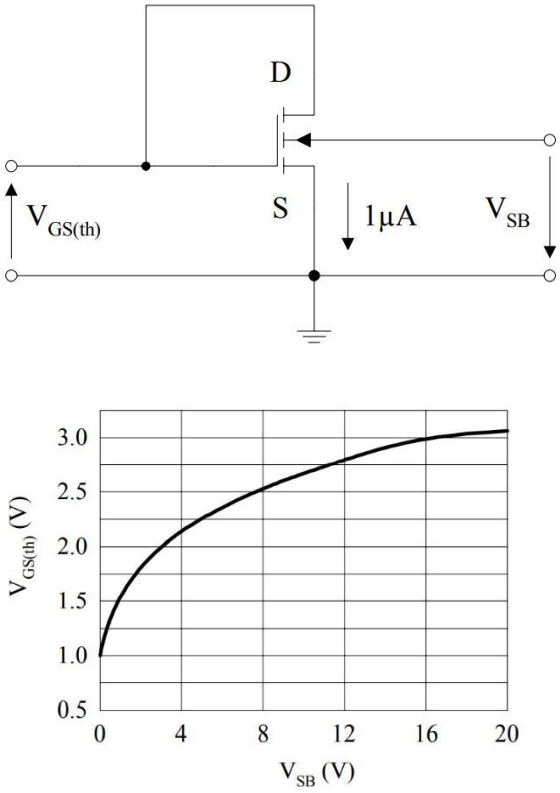


Figure 7. Threshold vs Source to Body Voltage

As the body voltage increases in the negative direction, the threshold goes up. Consequently, if VGS is small, the on-resistance of the channel can be very high. Figure 8 shows the effects of VSB and VGS on rDS(on). Therefore, to maintain a low on-resistance it is preferable to bias the body to a voltage close to the negative peaks of VS and use a gate voltage as high as possible.

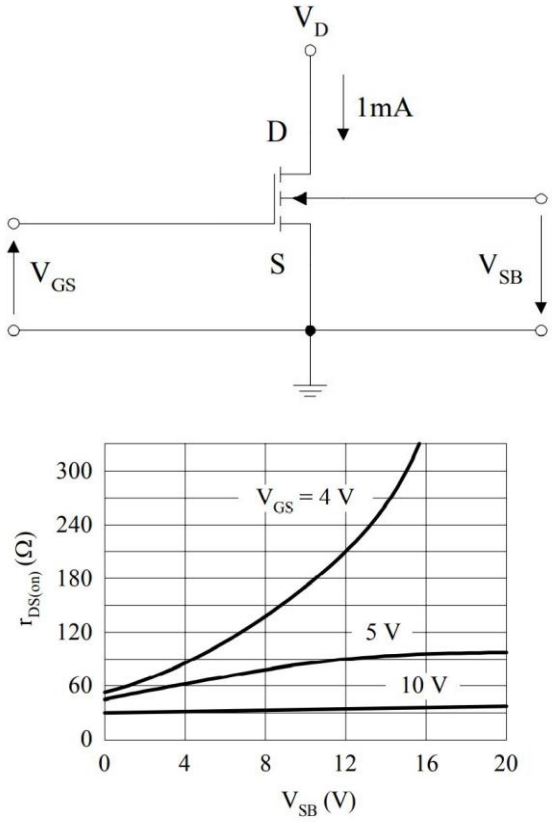


Figure 8. On Resistance vs Source to Body and Gate to Source Voltages

Charge Injection

Charge injection describes that phenomenon by which a voltage excursion at the gate produces an injection of electric charges via the gate-to-drain and the gate-to-source capacitances into the analog signal path. Another popular name for this phenomenon is “switching spikes."

Since these DMOS devices are asymmetrical[1] , the charge injected into the S and D terminals is different. Typical parasitic capacitances are on the order of 0.2 pF for C_{DG} and 1.5 pF for C_{SG}.

Another factor that influences the amount of charge injected is the amplitude of the gatevoltage excursion. This is a directly proportional relationship: the larger the excursion, the larger the injected charge. This can be seen by comparing curves (a) and (c) in Figure 9. One other variable to consider is the rate of gate-voltage change. Large amounts of charge are injected when faster rise and fall times are present at the gate. This is shown by curves (a) and (b) in Figure 9.

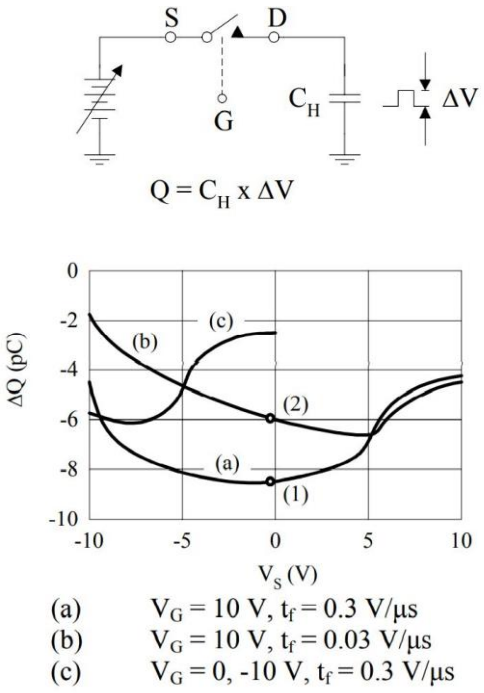


Figure 9. SD5000 Charge Injection

Switching spikes occur at switch turn-on as well as turn-off time. When the switch turns on, the charge injection effect is minimized by the usually low signal-source impedance. This low impedance tends to produce a rapid decay of the extra charge introduced in the channel. At turnoff, however, the injected charge might become stored in a sampling capacitor and create offsets and errors. These errors will have a magnitude that is inversely proportional to the magnitude of the holding capacitance.

Figure 9 illustrates several typical charge injection characteristics. Figure 10 shows some of the corresponding waveforms. The DMOS FETs, because of their inherent low parasitic capacitances, produce very low charge injection when compared to other analog switches (PMOS, CMOS, JFET, BIFET etc.). Still, when the offsets created are unacceptable, charge injection compensation techniques exist that eliminate or minimize them. The solution basically consists of injecting another charge of equal amplitude but opposite polarity at the time when the switch turns off.

Off-Isolation and Crosstalk

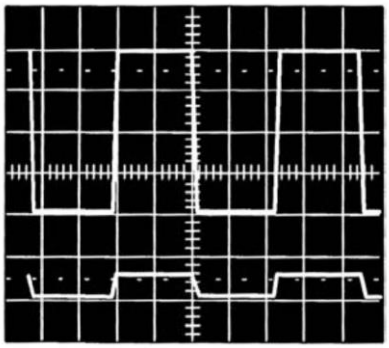
The dc on-state resistance is typically 30 Ω and the off-state resistance is typically 1010 Ω, which results in an off-state to on-state resistance ratio in excess of 108 . However, for video and VHF switching applications, the upper usable frequency limit is determined by how much of the incoming signal is coupled through the parasitic capacitances and appears at the switch output when ideally no signal should appear there in the off state.

[1]The chip geometry is such that non-identical behavior occurs when the source and drain terminals are reversed in a circuit.

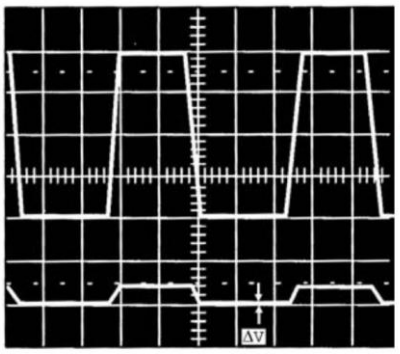
Off-Isolation is defined by the formula:

$$\text{Off - Isolation (dB)} = 20\log \frac{V_{out}}{V_{in}}$$

When several analog switches are simultaneously being used to control high frequency signals, crosstalk becomes a very important characteristic. For video applications, the stray signal coupled via parasitic capacitances to the signal of an adjacent channel can form ghosts and signal interference. To help obtain high degrees of isolation, it becomes necessary to exercise careful circuit layout, reducing parasitic capacitive and inductive couplings, and to use proper shielding and bypassing techniques. Figure 11 shows the excellent off-isolation and crosstalk performance typical of this family of DMOS analog switches.



(a) **TOP: 5 V/div** **HOR: 0.5 µs/div**
BOT: 50 mV/div **POINT (1)**



(b) **TOP: 5 V/div** **HOR: 0.5 µs/div**
BOT: 50 mV/div **POINT (2)**

Figure 10. Waveforms for Points (1) and (2) of Figure 9

Insertion Loss

At low frequencies, the attenuation caused by the switch is a function of its on-resistance and the load impedance. They form a simple series voltage divider network. As an example, for a 600 Ω load impedance the insertion loss for voice signals (1 Vrms at 3 kHz) is less than 0.3 dB. Thus, the SD5000 series make good audio crosspoint switches.

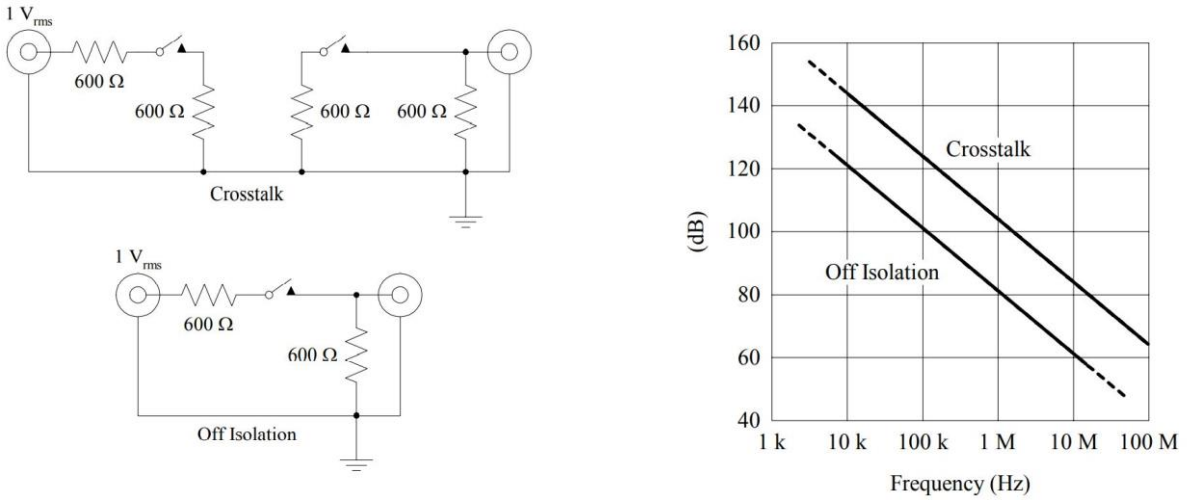


Figure 11. SD5000 Crosstalk and Off Isolation vs Frequency

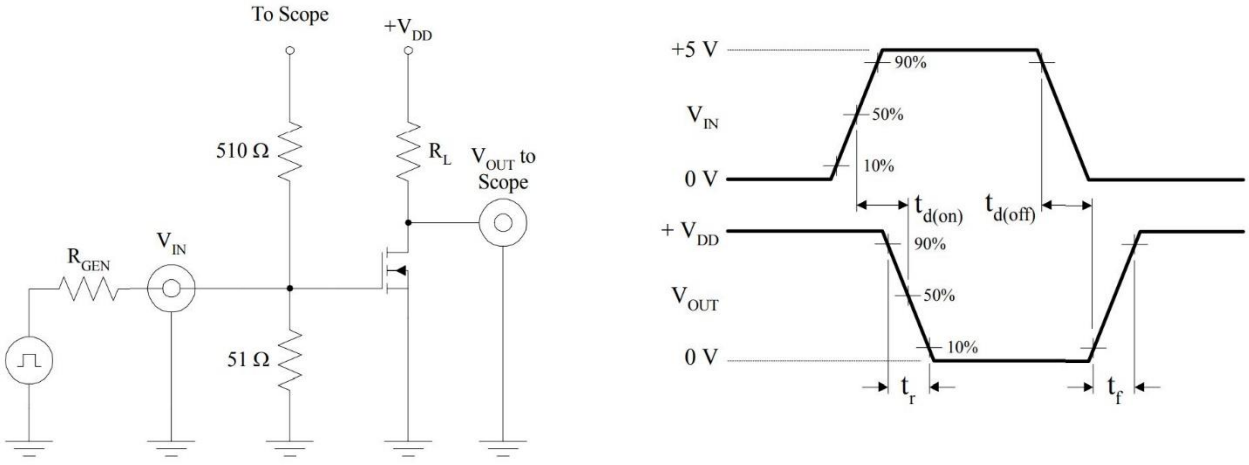


Figure 12. Switching Test Circuit

Speed

Because the on-resistance and input capacitance are low, the DMOS switches are capable of subnanosecond switching speeds. At these speeds the external circuit rather than the FET itself is often responsible for the rise and fall times that can be obtained. Let's consider the switching test circuit of Figure 12. At turn-on, the fall time observed at the drain is a function of RG and of the input pulse amplitude and rise time. The sooner CGS reaches VGS(th), the sooner turn-on will occur, and the lower the rDS(on) reached, the faster CDS will be discharged.

The turn-off time (or the rise time of VD) is not as much limited by the velocity at which CGS can be discharged by the gate control pulse, as it is by the time it takes to charge up CDS and CDG via the load resistor RL. Table 1 shows typical performances obtained. It is important to realize that stray capacitance and parasitic inductances, as well as scope probe capacitance, can seriously affect the rise and fall times (switching speed).

V_{DD} (V)	R_L (Ω)	$t_{d(on)}$ (ns)	t_r (ns)	[2] t_{OFF} (ns)
5	330	0.6	0.8	4
5	680	0.6	0.7	8
10	680	0.7	0.8	8
15	1k	0.9	1.0	12

[2] t_{OFF} is dependant on R_L and does not depend on the device characteristics.

Table 1. Typical Switching Times

Drivers

The switch driver's function is to translate logic control levels (either TTL, CMOS, or ECL) into the appropriate voltages needed at the gate so that the switch can be turned on or off. The SD5000 can be operated as an inverter capable of driving up to 20 V. This high-voltage rating, together with its high speed, make it an excellent driver for the other members of the family. Figure 13 shows several driver circuits. Since switching times depend on the CGS charge/discharge times, it is important to note that the driver's current source/sink capability plays a very important role in the process.

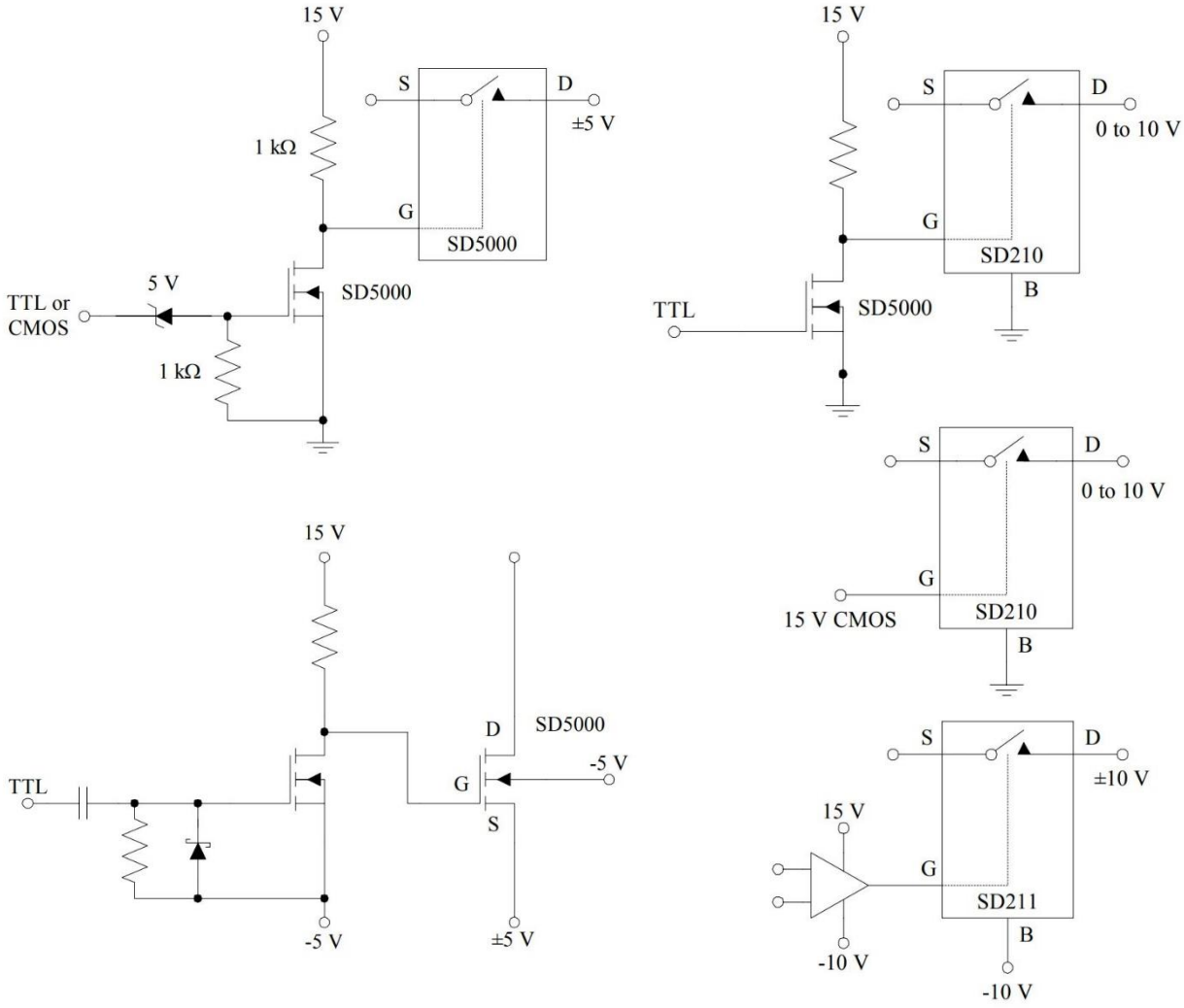


Figure 13. Various DMOS Drivers

High-Speed Multiplexer

In a typical application, the circuit of Figure 14 is used to multiplex and sample-and-hold two analog signals at a 5-MHz rate. Two of the switches in an SD5000 are used as level shifter/drivers to provide the gate drive of the single-pole-double-throw arrangement formed by switches 3 and 4. Capacitors C1 and C2 provide charge injection compensation.

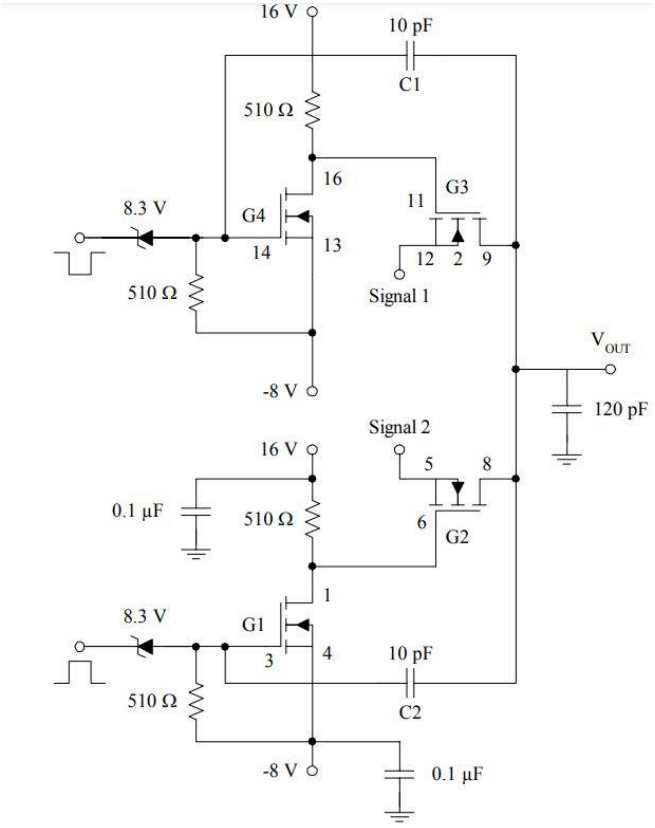


Figure 14. 5-MHz Multiplexer and Sample and Hold Circuit

Signal 1 is a 6-V, 156-kHz square wave. Signal 2 is a 2-Vpp, 78-kHz alternating waveform with a dc offset of -3.4 V (Figure 15).

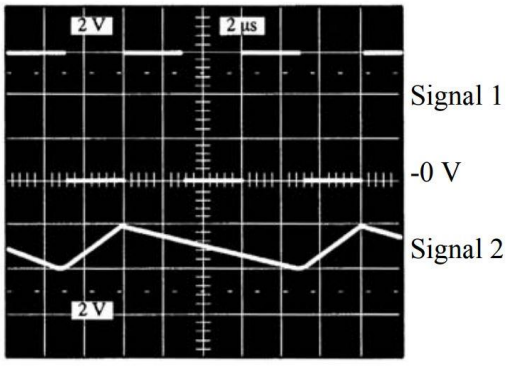


Figure 15. The Two Analog Signals to Be Sampled

Figure 16 illustrates the resulting composite waveform present at the holding capacitor along with the gate 3 control signal.

As can be seen, the switching times are about 15 ns, the acquisition time is 80 ns, and the holding time is about 90 ns. The total sample-and-hold cycle takes 200 ns. Even though not maximized, this speed is faster than what any other presently available (50 ns) analog switch products can achieve.

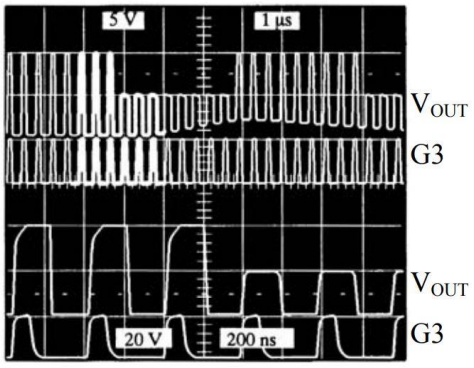


Figure 16. Composite Sample and Hold Output and the Gate 3 Control Signal

FREQ (Hz)	SIG LVL (dBm)	INS LOSS (dB)	OFF ISOL (dB)	XTALK (dB)
100 K	0	1.8	80	113
1 M	0	1.8	70	92
5 M	0	1.9	69	69
10 M	0	2.0	61	65
10 M	6	2.0	61	66
10 M	12	2.0	61	68

Table 2. SPDT Switching Performance

The timing and amplitude of gate 2 and gate 3 control-signals can be examined in Figure 17.

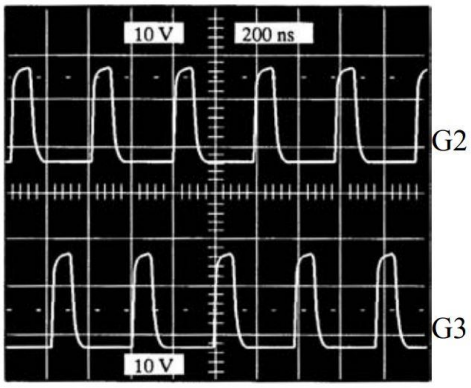


Figure 17. Gate Control Signals for the SPDT Switch Configuration

Figure 18 shows a single-pole single-throw configuration used to select one of two AM modulated 10-MHz signals. Figure 19 illustrates the two waveforms available at the output. Table 2 contains typical values of crosstalk and off-isolation attainable with this configuration.

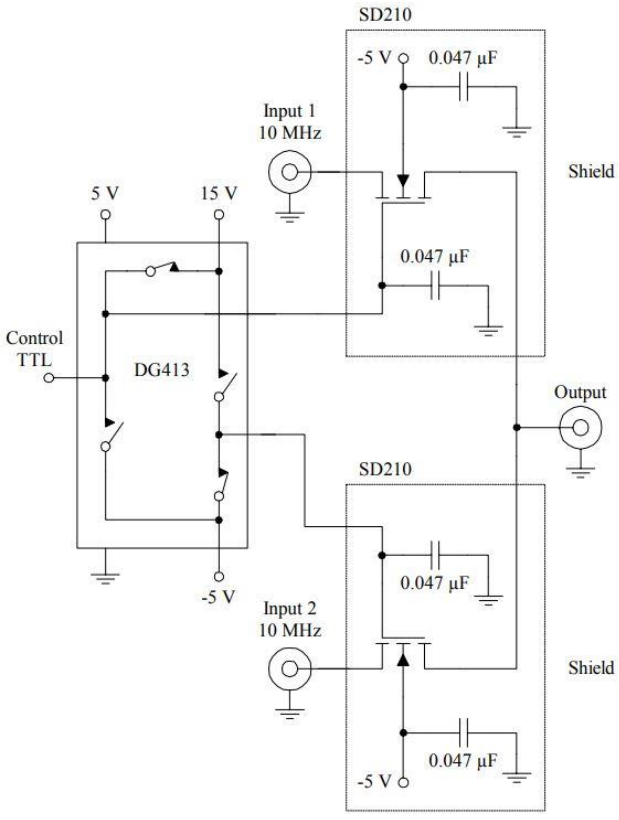


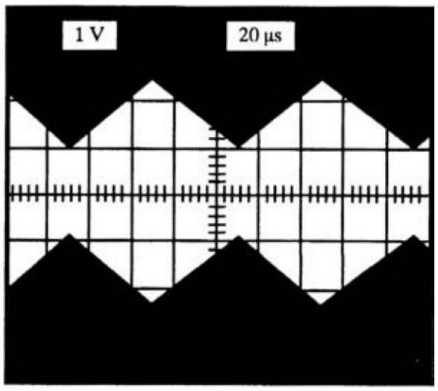
Figure 18. High Frequency SPDT Switch

A High-Speed S/H Circuit

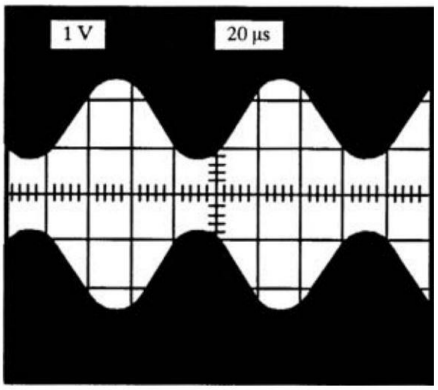
Figure 20 shows a fast unity gain input buffer (Si581) driving an SD5000 Switch. One half of the SD5000 is configured as dummy switches for charge injection compensation. A JFET output buffer minimizes droop. Transistors Q1 through Q4 level shift the ECL control input signals into a voltage (referenced to the analog signal voltage) used to drive the DMOS FETs.

DAC Deglitcher

A Very small charge injection makes DMOS FETs excellent DAC deglitcher switches. Figure 21 illustrates a typical circuit configuration.



Channel 1 On



Channel 2 On

Figure 19. Two 10-MHZ AM Modulated Outputs for the SPDT Switch of Figure 18

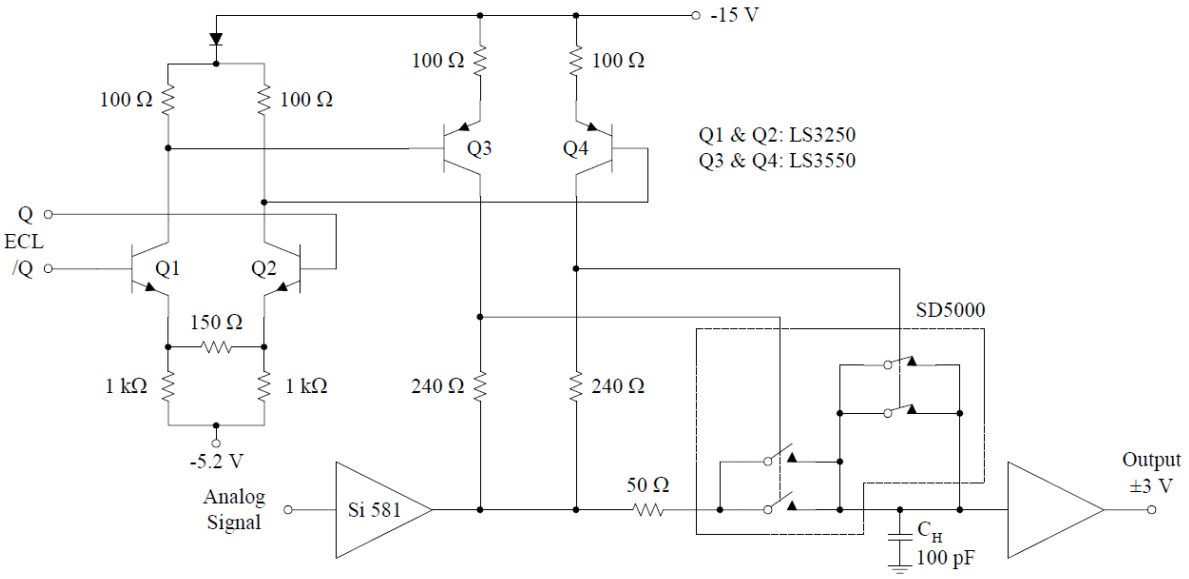


Figure 20. Fast S/H Circuit Achieves Minimum Step Errors

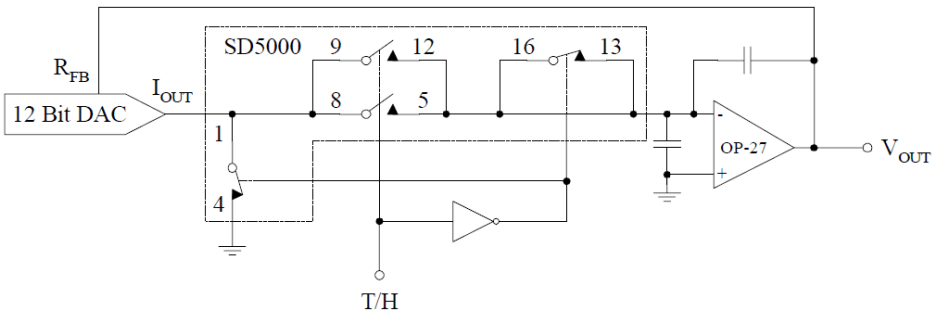


Figure 21. DAC Deglitcher Using DMOS Switches

Part Number	Package	Type	Zener Protection	$r_{DS(on)}$ (Ω)	$V_{(BR)DS}$ Min (V)
SD210DE	TO-72	Single	None	45	30
SD214DE	TO-72	Single	None	45	20
SD/SST211	TO-72/SOT-143	Single	Yes	45/50	30
SD/SST213	TO-72/SOT-143	Single	Yes	45/50	10
SD/SST215	TO-72/SOT-143	Single	Yes	45/50	20
SD5000N	PDIP	Quad	Yes	70	20
SD5001N	PDIP	Quad	Yes	70	10
SD5000I	CDIP	Quad	Yes	70	20
SD5400CY	SOIC	Quad	Yes	75	20
SD5401CY	SOIC	Quad	Yes	75	10
SD/SST823 [3]	TO-72/SOT-143	Single	Yes	5	15
SD/SST824 [3]	TO-72/SOT-143	Single	Yes	5	20

[3] Future devices available Q1 2003

Table 3. DMOS Device Part Numbers and Packages

LINEAR SYSTEMS

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APPLICATIONS FOR LOW LEAKAGE DIODES

In circuit designs for sensor signal conditioning, the design engineer must protect the input section from over-current and over-voltage conditions. Op-amps, ADC analog inputs, analog multiplexers, and [RS485] line receivers represent classes of devices that need protection. Often, the manufacturers of such devices specify the acceptable input range for voltage, or, in the case of an overvoltage condition, the allowable input current above which semiconductor or bonding wires may be damaged.

Note that an overcurrent condition may not cause immediate failure of the device, but instead may degrade the input device (increase offset voltage, increase bias current, increase noise, etc.). A typical input circuit voltage clamp using general purpose diodes such as 1N4148 and an op-amp such as the OPA604 is shown in Figure 1. Note that some details have been omitted for clarity, such as power supply bypass capacitors, frequency compensation components, and input bias current resistors.

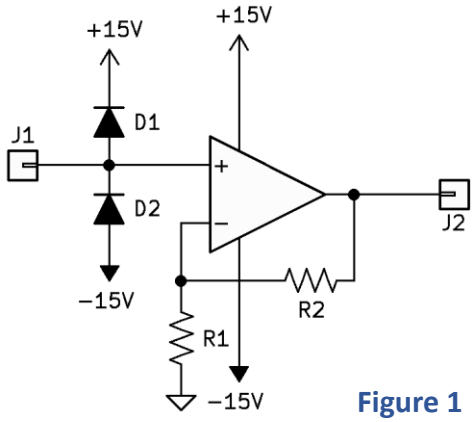

Figure 1

In this circuit, the diodes D1 and D2 connect to reference voltages that are the same as the op-amp's supply voltages. If a voltage greater than the supply rails plus the voltage drop across one silicon diode (typically 0.6V) is applied to J1 the diodes D1 and D2 limit the voltage from appearing at the op-amp's positive input. In real world applications, the over-voltage might be due to electro-static discharge; high-voltage arcing (welding equipment, X-ray generators); system power connections making contact with the J1; or, in the case of bio-medical monitoring devices, high-voltage pulses from cardiopulmonary resuscitation devices. See Reference 1 for a discussion of discharges of static electricity from someone touching the circuitry. Since we don't know the characteristics of this over-voltage source (low or high impedance; limited or virtually unlimited current), we would add extra resistance between the diodes and J1. For additional protection, we might also add extra resistance between the diodes and the op-amp. This improved version with R3 and R4 is shown in Figure 2.

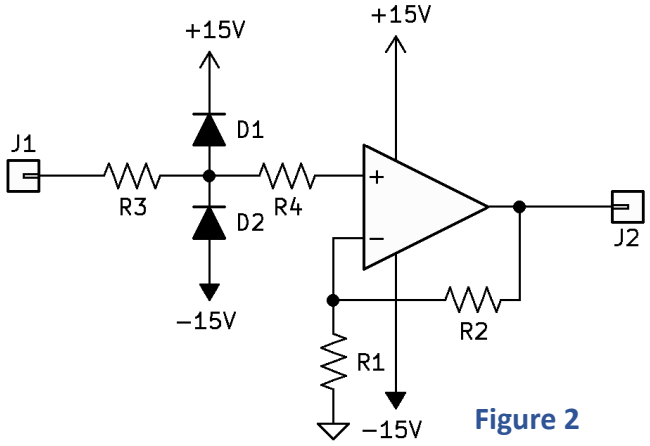

Figure 2

A variation on the previous circuit is the transimpedance (current-to-voltage) amplifier, shown in Figure 3. Note that at first glance, this looks like a voltage amplifier with R1 as the feedback resistor and R3 as the input resistor. In practice, R1 is very large compared to R3 and the voltage drop across R3 is trivial considering the extremely low signal currents being measured.

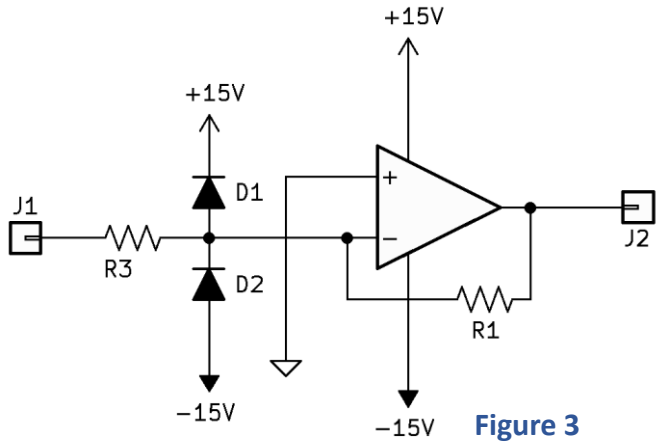

Figure 3

For many applications, this configuration would be good enough. But if the sensor output is very low (in the microvolts or pico- to femto-amps order of magnitude), measurement errors will occur.

For the circuit in Figure 2, the leakage current through the diodes creates a voltage at the junction of R3, R4, D1, and D2 that can swamp out the voltage being measured. For the circuit in Figure 3, the leakage current through the diodes may well be on the same order of magnitude as the current being measured. Examples of such current output sensors include photodiodes, photomultiplier tubes, Geiger-Müller tubes, piezo transducer accelerometers, and electrometers.

One way to reduce the diode leakage current is to use lower reference voltages at the top of D1 and the bottom of D2. For example, with ±5V instead of ±15V, the leakage current is lower. Keep in mind that the permissible signal voltage swing at the input is limited and the junction capacitance of the diodes will be higher in this scenario. More on junction capacitance induced problems in a bit.

A slight variation in lowering the reference voltage consists of a method to vary the reference voltage so it tracks the input voltage. See Figure 4 for a typical circuit. This sometimes referred to a bootstrapped drive and it touches on some of the same issues for which guard traces are used on a PC board. An excellent discussion of methods to guard sensitive circuits and minimize leakage currents across the surface of the PC board is available in Reference 2.

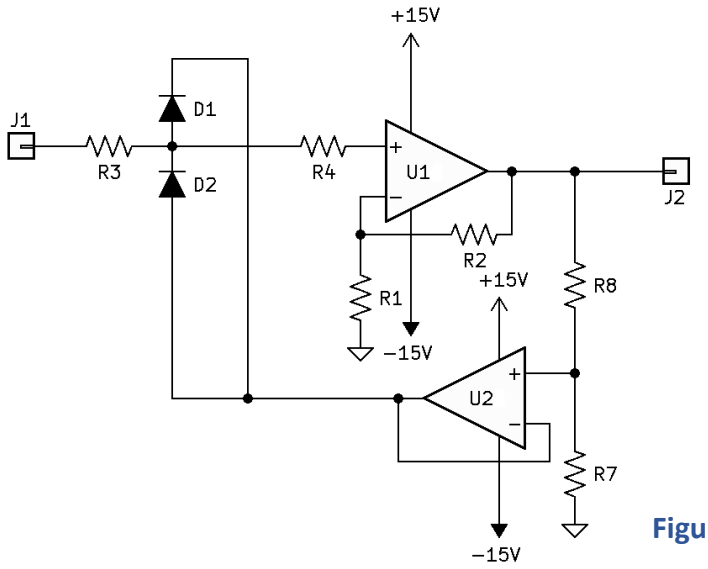

Figure 4

Note that R7 and R8 reduce the drive to U2 by an amount slightly greater than the gain of U1 (set by R1 and R2). This prevents the bootstrap circuitry from latching up or oscillating.

An additional application that has similar constraints is the sample-and-hold (S/H) circuit. The S/H is used to capture an analog signal and hold the value (voltage) steady while an analog-to-digital converter performs a conversion. See Figure 5 for a simplified version. The voltage on C1 follows the input voltage at J1, although with a slight lag based on the RC time constant. That time constant (in seconds) is the product of the sum of the resistance R3 plus the on-resistance of the analog switch (in Ohms) times the value of C1 (in Farads). At regular intervals, the Sample/Hold command is issued. As before, leakage current in diodes D1 and D2 will cause errors in the voltage measurement. Note that additional errors may be introduced due to charge injection from the analog switch.

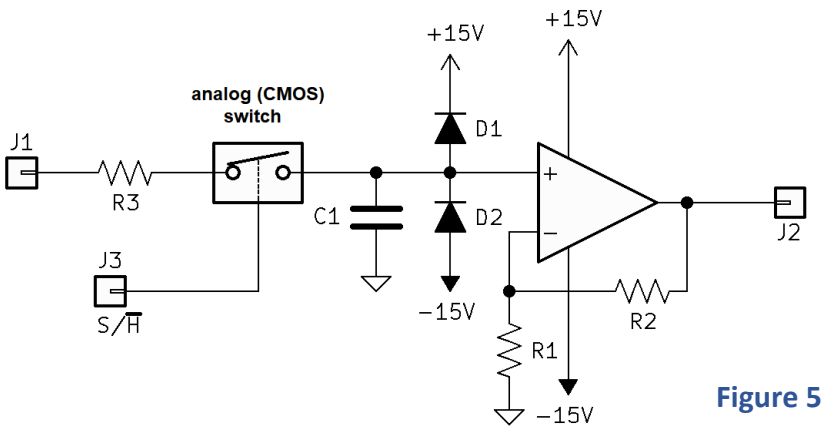

Figure 5

A variation on the S/H is the peak detector, shown in Figure 6. The voltage on C1 follows the input voltage minus the typical voltage drop across the diode (approximately 0.6V). At predetermined intervals, a RESET command is issued that returns the voltage on the capacitor to zero. Leakage in D3 will also cause measurement errors.

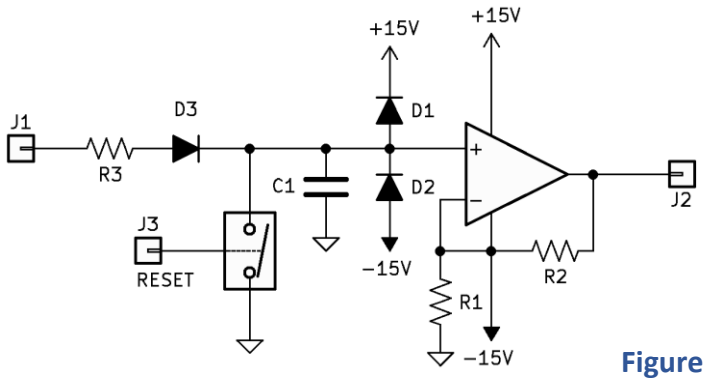

Figure 6

An additional consideration in all of the previous circuits concerns frequency response. While some of the sensors cited above are outputting signals that don't change quickly (i.e., low rate of repetition or low frequency), some may have high rep-rates or rapid slew rates. On signals with rapid slew rates, even if the rep-rate is slow, the signal's frequency spectrum is wide and the amplifier circuitry must have wide frequency response. If the clamp diodes have relatively high junction capacitance, their capacitance and the input resistor (R3, Figure 2) create a low pass filter and limits overall high frequency response. Worse yet, excessive capacitance at the transconductance op-amp's summing junction (op-amp's minus input, Figure 3) can cause excess signal overshoot (ringing) or oscillation.

An excellent solution to the problem of diode leakage is to use diodes specifically designed to exhibit ultra-low leakage current. The **Linear Integrated Systems** PAD Series of diodes will exhibit immediate improvement in the circuits shown in the preceding figures. A 1N4148 has a typical reverse leakage of 25nA at 25°C with an applied reverse voltage of 20V. The PAD1 diode has a typical reverse leakage of 1pA at 25°C with an applied reverse voltage of 20V.

Similarly, the solution to junction capacitance problems can be addressed with the PAD Series of diodes. Typical junction capacitance for a 1N4148 is 4pF. For the PAD1, typical junction capacitance is 0.5pF

Additional improvements in performance can be realized by adding a differential pair of junction FETs at the input of the op-amp. Shown in Figure 7, the JFETs are a matched pair in a single package, the **Linear Integrated Systems** LSK389.

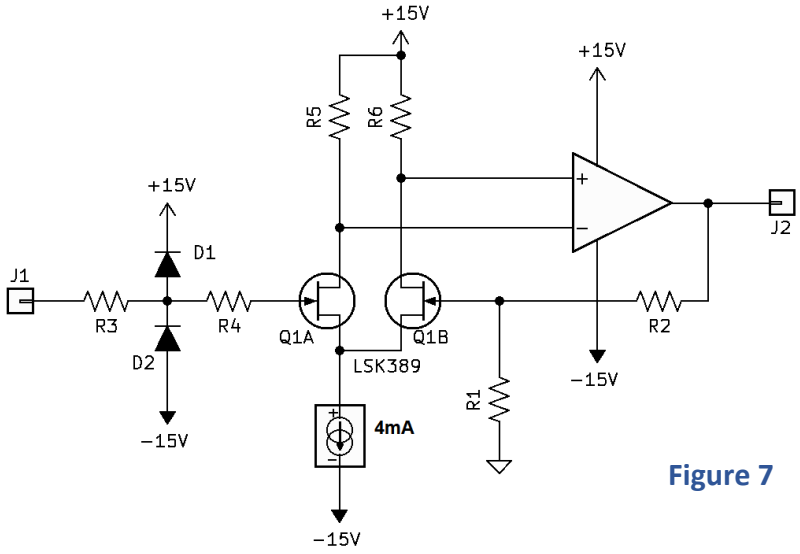

Figure 7

For a more detailed look at a real-world application, see Figure 8. This is a wideband amplifier having ±5000 VDC supply rails for the output stage. It is used in an electron energy separation device for an electron-beam machine. The output stage is unique. Where one might expect to see a complimentary pair of high-voltage transistors and suitable level shifting circuitry to drive them, instead there is a pair of specialty opto-couplers. The OC-100-HG devices are made by **Voltage Multipliers, Inc.** They consist of a pair of LEDs that illuminate photodiodes that have a reverse voltage rating of 10 kV. Current gain is about 0.01% (the ratio of LED forward current to diode photocurrent). This seems low, but as part of an amplifier comprised of an op-amp and discrete transistors, it is entirely acceptable. Overall, the closed loop gain is 60 dB.

The driving circuitry for the LEDs is a balanced 40 dB non-inverting differential current amplifier steered by a low offset voltage FET input op-amp (U1). The voltage swing at the output of the op-amp (and thus the drive current to the subsequent current mirror stages) is clamped to about ±5.7 V. The clamp circuitry is made up of the Zener diodes D6 and D8 plus the PAD1 pico-amp diodes D5 and D7. The Zener diodes are 5.1 V devices; the additional diode drop voltage produces the ±5.7 V clamp. Resistors R5 and R7 force sufficient current through D6 and D8 when clamping to produce a sharp knee in the characteristic Zener V-I curve. D5 and D7 isolate the clamp circuit from the op-amp's sensitive summing node when not clamping. The clamp limits the output stage drive current to the opto-coupler LEDs to about 1 A (peak) and the high-voltage output currents to less than 10 mA.

Matched **Linear Integrated Systems** dual bipolar transistors (LS312 and LS352) are used in the cascaded precision current mirror stages. These complimentary current mirrors allow a single potentiometer (R20) to adjust currents to both the upper and lower high voltage output stage.

Additional protection for the op-amp is provided by PAD1 diodes D3 and D4. As with D5 and D7 (above), these diodes present no discernable parasitic load and minimize interaction with the summing node during normal operating conditions. However, in the event of a high voltage arc, unpredictable voltages may appear at the summing node of the op-amp via the capacitive elements in the feedback network (C3 and C2).

Even with such low capacitance values, arcing transients have such rapid rise times that fairly high voltages would be present at the op-amp's summing node if D3 and D4 were not present.

One final note on this design: This circuit uses an extremely high value feedback resistor (R4, 1.0 GΩ). Compensation of a high voltage amplifier with 60 dB of gain with such a high value of feedback resistor is difficult. Instead of trying to tweak the overall high frequency characteristics of the amplifier with capacitors in the femto-farad range, a far more practical method is used. A ratioed capacitive reactance divider network made up of R2, C1, R3, C3, R24, and the much more practical adjustable trimmer capacitor C2 allows for easy compensation. See Reference 2 again for helpful information on working with extremely high value resistors.

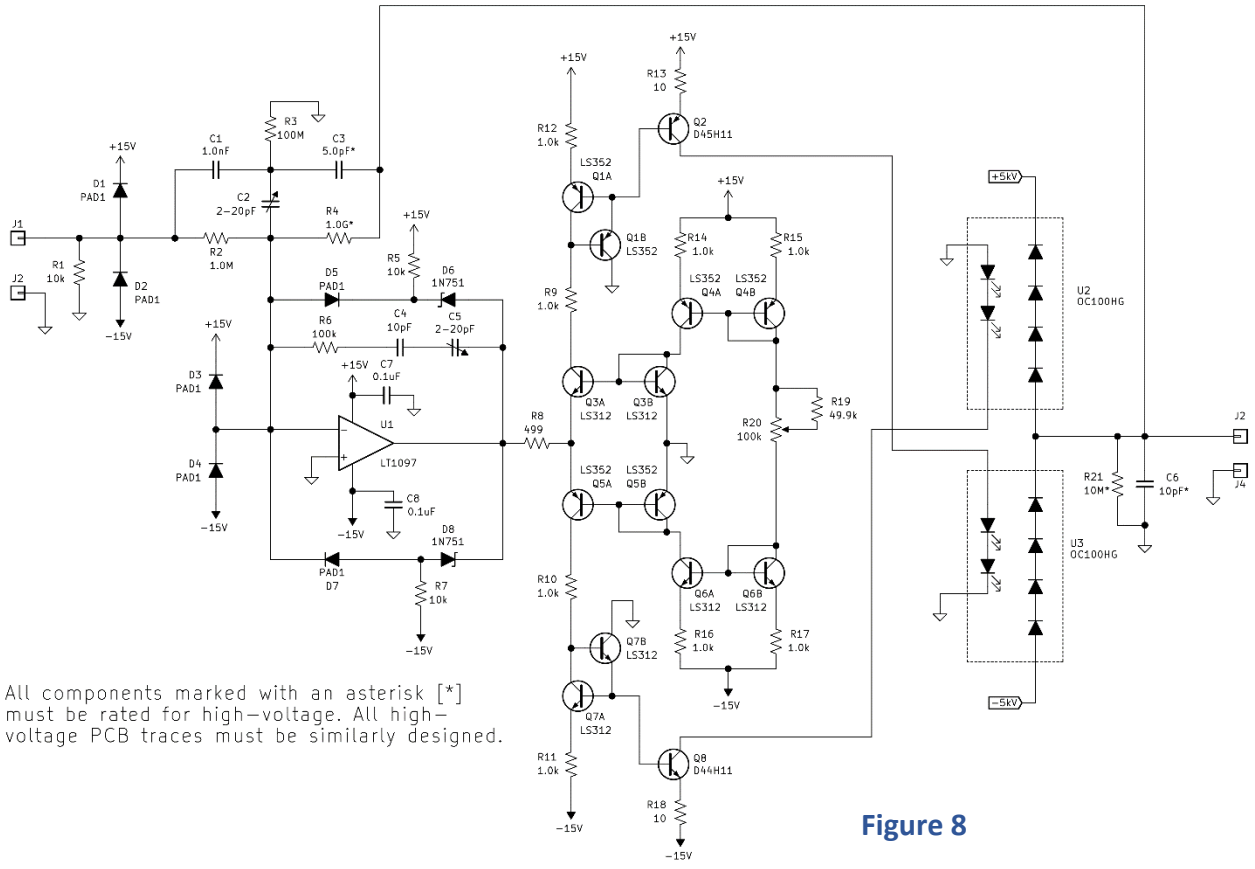

Figure 8

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Human-Body Model and Electrostatic Discharge (ESD) Tests

Comparison of Test Methods for Human Body Model (HBM) Electrostatic Discharge (ESD)

The ESD Association and JEDEC Publish New Revision to Standard for Electrostatic Discharge Sensitivity Testing

2. Design Femtoampere Circuits with Low Leakage, part 1, part 2

LINEAR SYSTEMS

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Linear Systems' Current Regulating Diodes

Abstract: Many analog circuit designs have the need for current regulation. Examples include circuits that process signals from sensors, circuits that amplify, and voltage reference or regulators. Current regulation can be referred to as a current source or a Norton device/equivalent circuit (cf. Thevenin equivalent circuit).

Common circuits to produce a constant current through a load of varying resistance are shown in Figure 1. In Figure 1a, R3 represents the load resistance that has a constant current passing through it from the +15V supply rail. The magnitude of that current is set by resistor R2 and by the control voltage presented to the positive input of the op-amp from R1. Note that the control voltage could be from an external source and could be a varying (AC) control signal. Also note that this configuration is sometimes called a current sink since the current is flowing down into the collector of the NPN transistor.

This circuit can be thought of as a simple amplifier with an emitter follower output stage (i.e., a unity voltage gain amplifier). Thus, the control voltage is replicated across R2. Ignoring the base current in the transistor and using Ohm's Law, the control voltage produces an emitter current that is replicated as the transistor's collector current. It will be constant across a range of resistance and is limited by the supply voltage for the circuit. This limitation is referred to as the circuit's voltage compliance – if the resistance is too large, the current source "runs out" of enough voltage to get the desired current.

To eliminate the small error caused by the previously neglected base current, the NPN transistor could be replaced by an N-channel MOSFET which effectively has no gate current for steady-state or slowly changing gate voltages.

An inversion of that circuit is shown in Figure 1b in which R6 is the varying load resistance, R5 and the control voltage from R4 set the current, and the load resistance connects to the circuit common or ground rather than the +15V source.

These types of current sources/sinks are fairly common, with slight variations to improve performance. As drawn, these are simplified schematics without supply bypass capacitors or frequency compensation components shown.

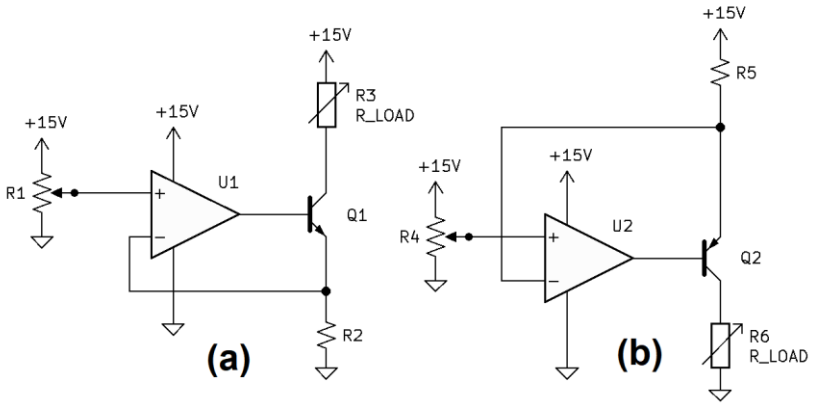

Figure 1

In some circuit configurations, a constant current device is needed that does not have the complexity of that which is shown in Figure 1. For example, in the simplified schematic of a discrete transistor amplifier shown in Figure 2 (using the **Linear Integrated Systems** matched pair NPN and PNP transistors LS312 and LS352), it would not be practical to add such complex circuitry for the current sources represented by I1, I2, and I3. These current sources are simple two-terminal devices that can be placed in various parts of the circuitry, even in locations that are not directly connected to ground or the power supply rail.

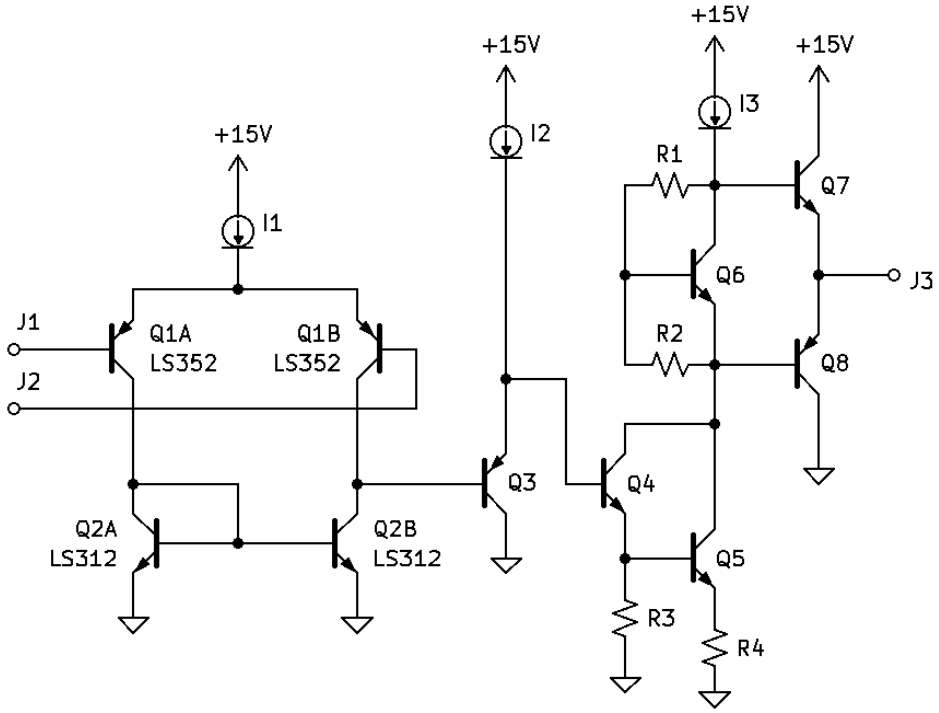

Figure 2

What is a two-terminal constant current device? Like the constant current circuits in Figure 1, it causes a constant current to flow through it regardless of the applied voltage or load resistance (+V and R1, respectively, in Figure 3). As before, the voltage compliance considerations must be observed (and the voltage must not exceed the breakdown voltage of the constant current device).

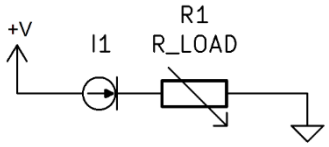

Figure 3

Two terminal constant current devices are commercially available, such as the **LIS** J500 series of devices. These devices are marketed as diodes (since outwardly they have two terminals) but are actually depletion mode N-channel junction FETs (N-JFET) plus a resistor to set the constant current level.

A depletion mode FET is made from a bar of silicon with electrical contacts near each end of the bar, forming a conduction channel. These metallic contacts are referred to as ohmic contacts as they are simple connections as opposed to silicon junction contacts (contacts made of P or N layers of doped silicon). The gate contact however *is* a doped silicon contact (represented as a diode in the FET symbol). See Figure 4.

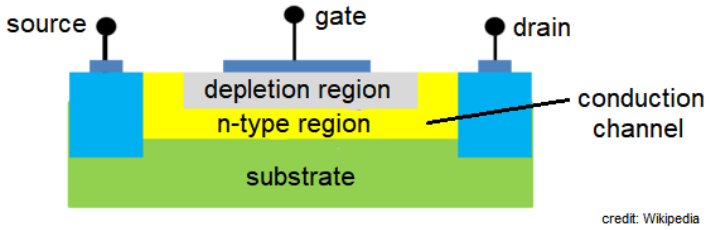

Figure 4

When used as an amplifying device, the gate voltage is more negative than the potential of the silicon bar near the diode area. No current flows through the diode (ignoring leakage currents) since it's reverse biased. However, the potential of the voltage on the gate causes the conductance through the silicon bar to vary due to the gate voltage's electrical field. The channel is depleted of charge carriers. The higher the negative voltage on the gate, the greater the electrical field and the narrower the conduction channel through the silicon bar.

This phenomenon of *field effect* varies the conductance of the channel. With no gate voltage, the channel acts as a low value resistance; with a sufficiently high negative voltage, the channel is completely depleted of charge carriers (i.e., is pinched off) and acts as a very high resistance. The ratio of the current flow through the JFET (measured at a particular drain-to-source voltage) and the gate voltage is the transconductance or transadmittance, measured in mhos (the reciprocal of resistance or impedance, measured in ohms). Transconductance is a DC characteristic related to resistance; transadmittance is an AC characteristic related to impedance.

If an N-JFET is connected as shown in Figure 5 with a positive voltage applied to terminal 1 and some load resistance to terminal 2 (which is then connected to ground), some current will flow downward. That current causes a voltage drop in the R-set resistor which puts the gate voltage at a somewhat more negative voltage than the source. This increases the channel resistance and reduces the magnitude of the current. An equilibrium point is reached based on the value of the R-set resistance and the transconductance of the JFET. Within the voltage compliance considerations as previously described, the device will provide a constant current to varying loads.

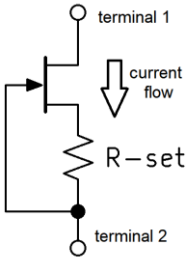

Figure 5

Because the constant current diode is a two-terminal device, the load could be placed above the diode with terminal 2 connecting to ground – or the diode could be placed in the midst of circuitry with no direct connection to power or ground.

To the extent that the current regulator diode is accurate, variations in the resistance of the load won't cause any variation in the current, implying good load regulation characteristics. Similarly, variations in the applied voltage won't cause the current through the load resistance to vary, implying good line regulation characteristics.

Specific Uses

1. Zener diodes and voltage reference diodes. These are commonly used to provide a reference voltage for various sensor circuits or for ADCs and DACs. The Zener or reference diode could receive its excitation voltage from the power supply via a resistor as shown in Figure 6a. One might assume that the nature of such voltage references would imply good line and load regulation. Sometimes the regulation is good enough, but for precision applications, the line regulation characteristics of a Zener diode leave much to be desired. An improvement can be realized by using a constant current diode like one of the J500 series devices (D2 in Figure 6b).

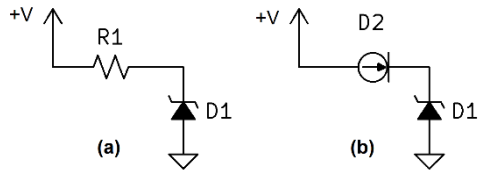

Figure 6

2. Discrete transistor amplifiers. See the circuitry in Figure 2, above, or in Figure 7, below. In Figure 7, the constant current source shared by the differential input FETs (LSK389) forces a total of 4 mA through the two FETs to keep them both in their linear operating range. This current is steered back and forth between the two FETs depending on the input voltage at J1 and the equal magnitude but opposite phase [angle] voltage the fed back from the output.

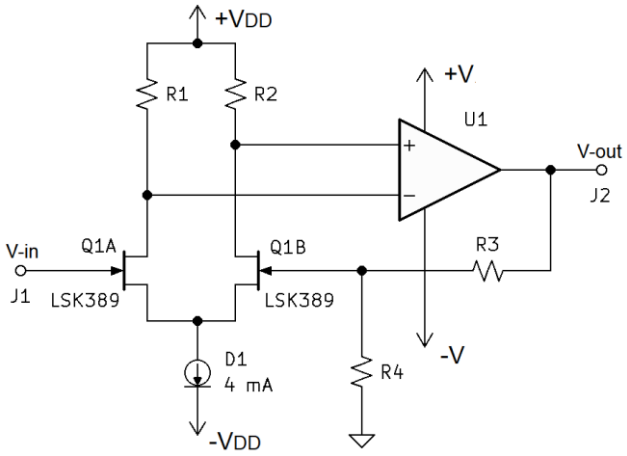

Figure 7

3. Current source plus current mirror. Figure 8 shows a circuit similar to that which appears in Figure 2 and represents a typical sub-circuit. This uses a constant current diode (D1) to force a reference current through the left half of a current mirror (Q1A). That current is matched as I_{LOAD} in the right half of the current mirror (Q1B) and through the Z_{LOAD}. Z_{LOAD} represents the following amplification or frequency shaping stages used in typical sensor circuitry. Note that Q1A and Q1B are fabricated on the same silicon chip and are therefore matched devices (matched V_{BE} and β). This is essential to ensure that the current mirror works as designed.

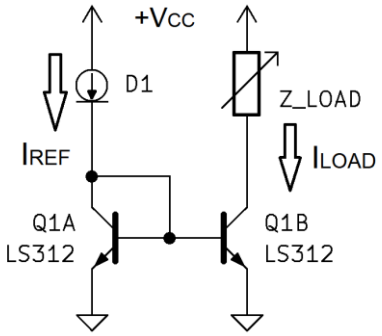

Figure 8

This configuration helps to isolate the constant current diode from the (perhaps) unpredictable resistance or impedance variations of the load.

In cases where the load current must be some multiple of the reference current, multiple matched transistors (fabricated on the same chip) are used. Figure 9a shows an example where I_{LOAD} is 5X I_{REF}. Figure 9b shows an example where I_{LOAD} is 1.5X I_{REF}.

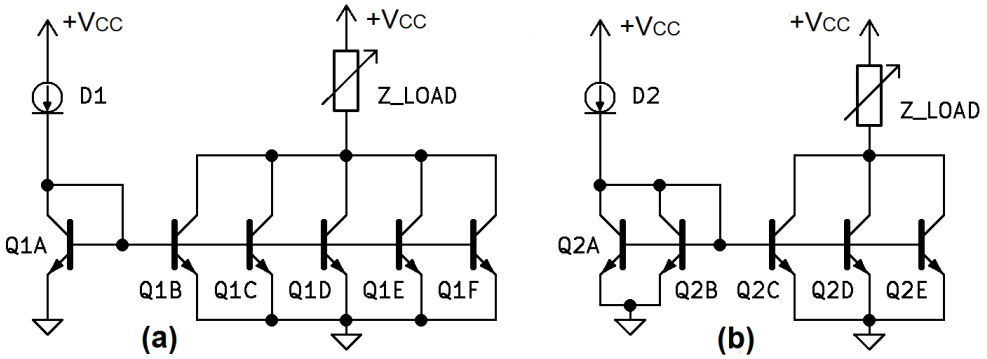

Figure 9

These circuits might see usage as part of the biasing circuitry for an amplifier; as an excitation source for LEDs or sensors; as a charging circuit for super capacitors or batteries; or as a current calibrator for photodiodes or other sensors (temperature, pressure, flow volume, etc.).

Conclusion: There are multiple uses for constant current diodes such as the Linear Integrated Systems J500 devices. Properly applied, they will simplify analog circuit designs for voltage reference circuits, amplifier circuits, and sensor signal processors.

LINEAR SYSTEMS

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SOLVING THE NOISE PUZZLE WITH LOW-NOISE MATCHED BIPOLAR TRANSISTOR PAIRS

LS310 & LS350

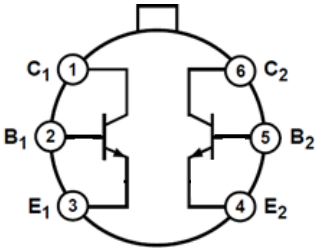
Noise is one of the more important aspects of circuit design. Lower noise in audio amplifier design means better quality audio. Low-noise in instrument design means more reliable and accurate measurements at lower voltage and current levels. And low-noise in current source designs means less noise injected into the electronic system.

One of the most basic approaches to reduce noise in an amplifier is to use low-noise components. This would include low-noise bipolar transistors and low-valued resistors. Although one can use low-noise operational amplifiers in the design of low-noise circuits or low-noise current sources it is often not done. This is because lower noise can be often be obtained with a well-thought out discrete design. And that's because discrete transistors offer much more design customization capability for specific circuit applications – like optimized collector biasing. One must remember that monolithic chip designs are built for the most part for general purpose applications. It is hard to tailor a specific op amp or current source chip for a specific source resistance, specific power consumption requirement and a specific bandwidth that will lower the overall noise – that is unless you add-on more compensation components.

When to Select a Matched Low-Noise Bipolar Transistor

Bipolar transistors offer significant lower noise at lower source resistance levels and lower collector currents than JFETs. As a rule of thumb, a low-noise bipolar transistor should be chosen over a JFET when the source resistance is less than 10K ohms or when the active current (drain or collector) is less than 0.5 ma. Because the LS310 (NPN) and LS350 (PNP) Series are tightly matched low-noise bipolar pairs they are ideal for low-noise applications that have two or more transistors and for designing ultra-low-noise differential circuit topologies. In a differential arrangement common mode signal line noise is canceled out because of the architecture leaving only the ultra-low-noise of the LS310 or LS350 to stand by itself or to be further optimized.

For differential applications, these bipolar transistors include vbe matching in the order of 0.2mV, good differential current gain matching, low base current differential and low voltage and current differential change with temperature. For both single and dual ended applications the devices feature an equivalent noise voltage between 700pV and 7.5nV typical, current gain between 100 and 1000 and a current gain bandwidth product specified at 200 MHz minimum.



Note:

1. **Substrate is connected to case on TO-78 package.**
2. **Substrate is normally connected to the most negative circuit potential, but can be floated.**

Figure 1: The LS310 and LS350 NPN and PNP Matched Bipolar Transistors are often used for low-noise amplifier design and as a replacement part for low-noise aftermarket and legacy bipolar transistor products. The LS310 comes as tested bare die and in several different package types: PDIP 8L RoHS, TO-71 6L RoHS, TO-78 6L RoHS, SOIC 8L RoHS, SOT-23 6L RoHS and DFN 8L RoHS.

Design for Noise Checklist

Low-noise components and the lowest possible resistor values are often at the top of a Design for Noise checklist. However, there are several other Design-for-Noise items that need to be checked if you want to ensure a noise-free success. This includes a noise optimized collector bias level and the overall layout of the design (avoid long leads). Other check list items include noise coming through the power lines or that being picked up over the airways. There is also temperature. Noise, random fluctuation of electrons, increases with temperature. Also remember there is bandwidth to consider. Circuits with lower bandwidth will have less noise. So, it is prudent to have narrowband input filters and to design amplifiers to have precisely defined low and high cutoff frequencies. Add to this list the source resistance, the input noise current and noise voltage specification of the bipolar transistor and for the most part you should be on your way.

Noise and Resistance

Because noise increases with increased resistance values, Design for Noise means using resistors that are as low in value as possible, especially if they are in a noise gain signal path. The thermal noise (Johnson Noise) equation for a resistor, below, indicates that noise voltage increases with temperature, the resistor value and the bandwidth of the circuit design. Specifically, this equation gives the root mean square voltage in volts across a resistor as a function of temperature (Degrees Kelvin) bandwidth(delta f), and resistance (R). K is Boltzmann's constant.

Equation 1: Thermal Noise Voltage of a Resistor, Johnson Noise

$$e_N = \sqrt{4kTR_s\Delta f} \ \ V$$

One will see the Johnson noise equation in various forms in the study of thermal noise. It is sometimes expressed in terms of Volts squared, at room temperature=300 K, and with the numerical value of the Boltzmann constant, k, factored in to simplify noise calculations.

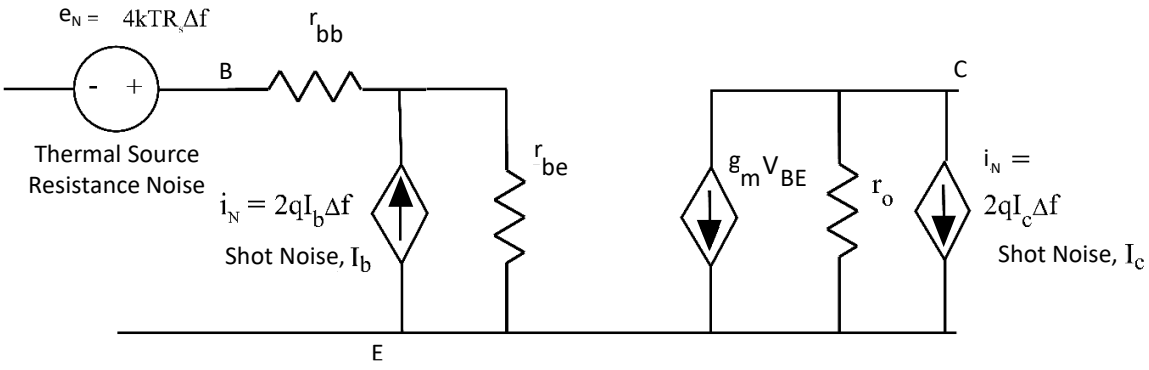
Equation 2: Root Mean Square Thermal Noise Voltage of a Resistor at Room Temperature

$$(e_n)^2 = 1.66X10^{-20}(R_s\Delta f) \ \ V^2$$

It is the above two equations along with the fundamental noise equation, equation 3, discussed later, that are most dominant in bipolar circuit noise calculations. Other equations can be used to factor in flicker noise, combination and recombination noise and burst noise. These basic equations indicate that circuits that have a lower bandwidth and lower resistor values will inherently have lower noise.

Shown below is one common bipolar noise model. It includes the thermal noise from the source resistance (of which the base spreading resistance can be added). It also includes the base current shot noise and the collector current shot noise dependent current sources. This model is often used for a quick analysis of noise in bipolar circuits (Fronczak).

Figure 2: Bipolar Noise Model

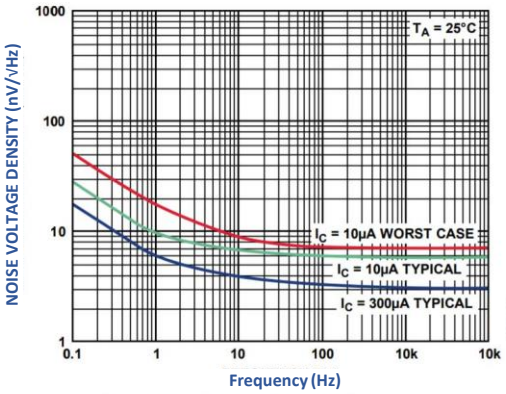


Often the bandwidth, delta f, is taken out of the equation. This results in the term often seen in data sheets, where input voltage noise has units of Volts per square root Hertz. These equations represent the noise voltage density and not the root mean square noise voltage. They give the noise per 1 Hz bandwidth. Although these equations are useful, they do not directly give the noise voltage as a function of bandwidth.

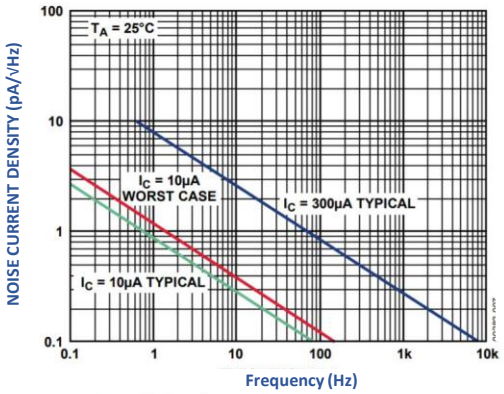
Bipolar Noise Specifications

In the realm of the bipolar transistor itself, the main consideration is the equivalent input noise voltage and equivalent input noise current – the lower the better. These two specifications are often given on data sheets as min typ or max specifications or graphed on a chart of noise voltage versus frequency versus collector current. The specifications and charts in themselves imply design guidelines. Noise in bipolar transistors is highest at low frequencies and drops dramatically with increased frequency. As well, voltage noise decreases with higher collector currents and current noise increases with higher collector currents. Because the input current noise flows through the source resistor and the base spreading resistor, the effect of increasing the collector current to reduce current noise is offset with an increase in noise voltage from the higher noise current flowing through the source and base spreading resistor.

Figure 3: Noise Voltage and Noise Current Density as a Function of Frequency and Collector Current



Noise Voltage Density vs. Frequency



Noise Current Density vs. Frequency

Source Resistance and Noise

Source resistance is one of the major factors that affect noise. Because input current noise flows through the source resistance driving the circuit, input current noise is multiplied by the source resistor to obtain the input voltage noise. As collector current rises, input current or base current must rise since collector current and base current are related through beta.

The fundamental noise equation for a bipolar transistor, equation 3 below, illustrates the effect of the value of source resistance on equivalent input voltage noise. The source resistance is in the base shot noise and the thermal noise terms of the equation. The equation also indicates that temperature and collector current play a role in noise. This equation is expressed in units of Volts squared per Hertz (the bandwidth, delta f, would have to be multiplied by the equation to give the noise in Volts squared. The he square root would then have to be taken to give the noise voltage in Volts).

Equation 3: Fundamental Bipolar Voltage Noise Density, Volts Squared Per Hertz

$$e_N^2 = \frac{2k^2T^2}{qI_c} + \frac{2qI_cr_s^2}{h_{FE}} + 4kTr_s$$

Equation 4: Fundamental Bipolar Voltage Noise Density, Volts Squared Per Hertz

$$e_N^2 = \frac{2k^2T^2}{qI_c} + \frac{2qI_cr_s^2}{h_{FE}} + 4kTr_s$$

The equation suggests that to obtain the lowest possible noise there is an optimal value of collector current for a given value of source resistance. From calculus, taking the derivative of the above equation with respect to the collector current and setting the result equal to zero, gives the optimal value of collector current for a noise minimum, equation 4.

Equation 5: Optimum Collector Current for Minimum Noise and Given Source Resistor

$$I_{copt} = \frac{kT}{q}\sqrt{\frac{h_{FE}}{r_s}} = 0.025\sqrt{\frac{h_{FE}}{r_s}}$$

The above equation can be used for a specific temperature using degrees Kelvin. Or the simplified form can be used for room temperature of 300 degrees Kelvin. In the equation, q, is the charge of an electron, 1.6 X 10^-19 and k is Boltzmann's constant, 1.381X10^-23.

If the base spreading resistance(r_{bb}) of the bipolar transistor is significantly high enough it should be included as part of the source resistance in equation 4. For the LS31X series, rbb is in the order of 30 Ohms at a nominal bias level. At lower levels of collector bias it can increase up to 1000 ohms.

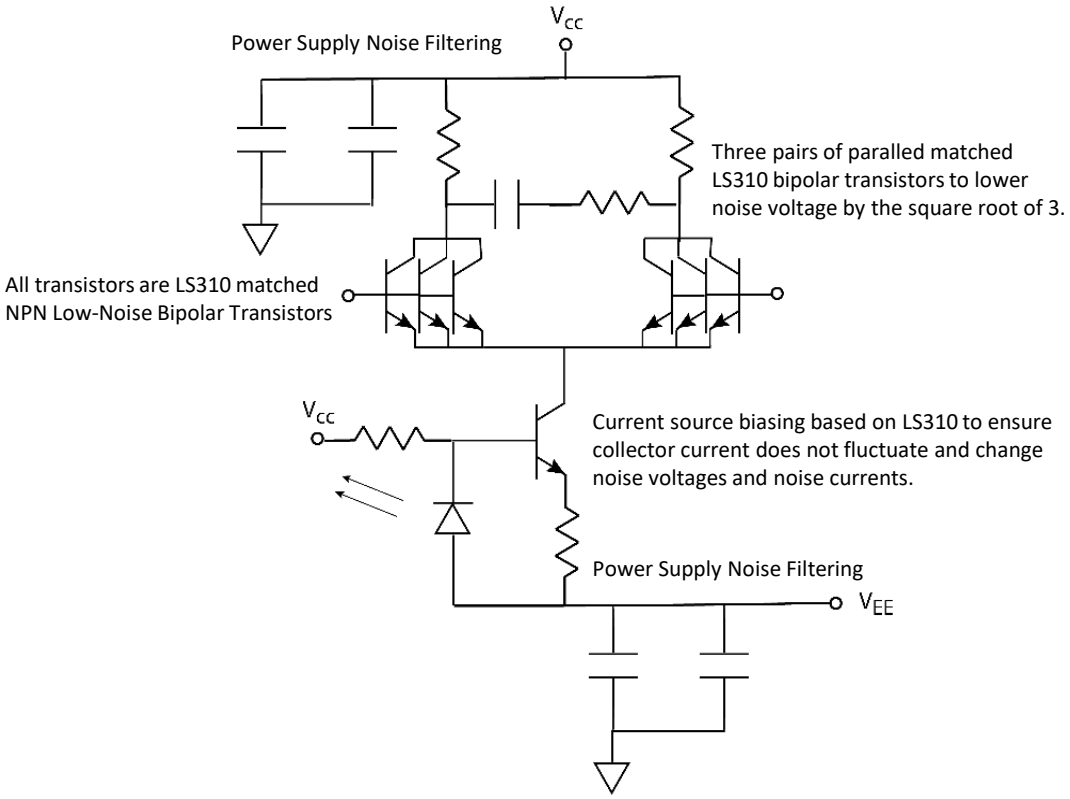
In analyzing equation 4, it should be borne in mind that hfe (or Beta) increases with both collector current(to a point) and temperature. There is a peak hfe associated with collector current, after which hfe decreases with increasing collector current. For the LS310 series, the LS310, 311, 312, and 313 nominal hfe ranges from 100 to 1000.

Building Ultra-Low-Noise Amplifiers, Current Sources, Multipliers and More

Low-noise discrete bipolar designs are commonly used to build ultra-low-noise preamplifiers, low-noise microphone preamplifiers, digitally programmed current pumps (DAC with Wilson Current Source) cascode current sources, current matching circuits, multipliers, power meters, strain gauge instrumentation amplifiers, thermocouple amplifiers and a wide range of analog mathematical circuits.

Shown below is an ultra-low-noise discrete bipolar preamplifier that can be designed for a voltage noise level below 0.5 nV per square root Hertz. The design uses paralleled LS310s to reduce the input voltage noise (paralleling bipolar transistors reduces the base spreading resistance by a factor equal to the square root of the number of transistors paralleled, in this case the square root of three). This reduces the input voltage noise as related to the shot current noise of the base. For ultra-low-noise and ultra-low power, the circuit can be biased using the optimum Ic value calculated from equation 4, given above. The current source in the schematic is based on a red LED.

Figure 4: Noise Optimized Differential Amplifier Based on LS310 Paralleled Resistors and Current Source



Conclusion

Depending on the specific parameters of the transistor used, a wide range of low-value collector bias currents can be used to obtain both low-noise and low power circuits Knowing what the source resistance is and the value of hfe lets one calculate the optimum noise collector bias current. It also allows one to optimize for the lowest power consumption.

It should be remembered that input current noise increases with higher collector current, but voltage noise decreases with higher collector current. This tradeoff is mitigated through the selection of a lower source resistance, if possible. Paralleling bipolar transistors allow for reduced noise voltage, but low source resistances should be used to compensate for an increase in input noise current. Finally, one should use characteristic curves for the voltage noise and the current noise of a specific transistor for frequency, hfe (beta), collector current and temperature. This simplifies the noise analysis task in that actual noise effects of operating points can be determined without calculation or simulation.

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Radiation Sensor Design and Applications: The 3N163

By Mark Stansberry

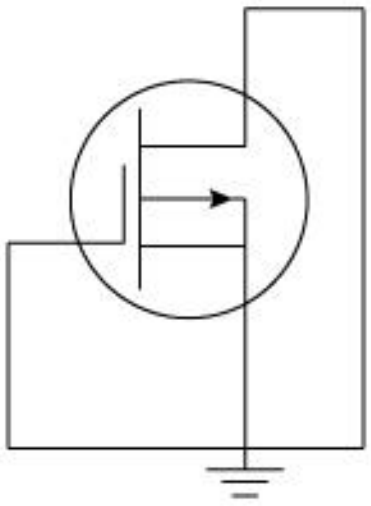
Radiation Sensor Design and Applications: The 3N163

Wireless real-time radiation sensor networks offer the general public and those that work in high radiation areas greater protection against radiation hazards. Combined with real-time localized and global heat mapping of radiation levels, these radiation networks will help give government and environmental agencies the ability to understand the radiation landscape and respond quickly to radiation changes before they become life-threatening.

Low-cost, low-power and no-power radiation sensors, also known as RADFETS (Radiation Field Effect Transistors) or dosimeters, are necessary for the implementation of these networks. The RADFET is unique because it does not need a power source to detect radiation. The RADFET is also unique in that it records the amount of actual radiation exposure. The RADFET, as a non-volatile analog memory device, stores the level of radiation exposure as a change in threshold voltage. RADFET's are relatively simple circuits, consisting of only a PMOS transistor. The LS 3N163 PMOS transistor can be used to design a RADFETs to meet different design requirements like cost, sensitivity, linearity and power. The ability to optimize a RADFET for these different design requirements give network designers the ability to construct wireless radiation sensor networks that can also be optimized for cost and performance on a wide scale.

Radiation Detector Principles

PMOS (P-Channel) MOSFET radiation detectors work on the principle that electron-hole pairs form when radiation or an ionizing particle strikes the MOSFET. This in turn results in shifts to the threshold voltage and drain current parameters of the MOSFET device. Because the change in threshold voltage with radiation exposure is highly linear in a PMOS device, PMOS devices such as the LS 3N163 are commonly used as a radiation detector. In a typical application, the LS 3N163 is operated in unbiased mode (no-power mode) and exposed to radiation. The change in threshold voltage is then measured and the corresponding radiation exposure level determined. In another application, where higher levels of sensitivity are needed, the LS 3N163 is operated in biased mode (power mode).



P-Channel Transistor in No-Power Radiation Detection Mode

Figure 1 - Simple RADFET gate, substrate, drain and source connections

Radiation Sensor Parameters

Central to the design of a radiation sensor are sensitivity and sensitivity loss. Sensitivity is defined as the change in threshold voltage shift per accumulated radiation dose (measured in SI-Gray Units, 1 Gy = 1 J/kg = 100 rad)

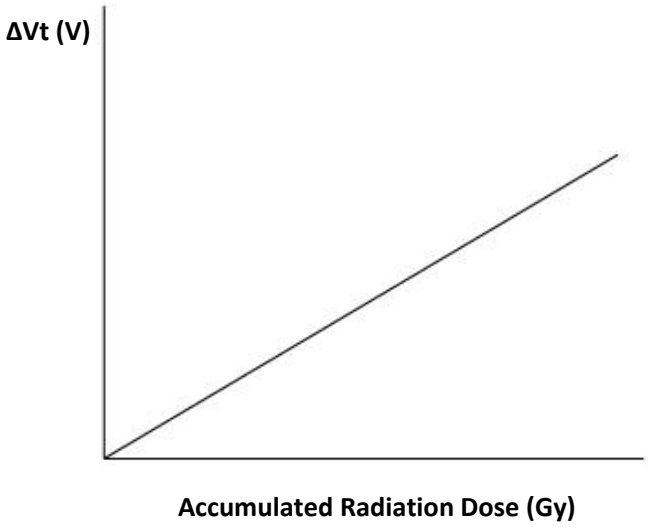


Figure 2: Threshold voltage shift in P-Channel transistors as a function of radiation dose

Sensitivity loss on the other hand, is the loss of sensitivity as a result of previous exposure to radiation events. Sensitivity loss levels can be in the order of 1 percent per kGy of radiation energy exposure (10). This requires that the detectors be recalibrated so as to accurately measure the radiation dose. Alternatively, because of the low-cost of the LS 3n163, the devices can be deposed when sensitivity falls below required levels.

Improving Sensitivity

Different design techniques have been studied to increase the radiation sensitivity levels of the LS 3N163 and other MOSFET devices. It has been shown that the biasing of the MOSFET effects sensitivity. Sensitivity to radiation is higher in the biased mode than the unbiased mode (non-power mode).

Data on sensitivity to 6MV photon beams data showed that the 3N163 has a sensitivity of 33 mV/Gy in the unbiased mode and 62 mV/Gy in the biased mode (9). In that study one and two-stacked transistor, biased and unstacked configurations were analyzed. Stacking PMOS transistors increases the effective oxide thickness of gate oxide, increasing its sensitivity.

Emerging Applications

Energy harvesters, used to convert vibrations to electrical energy, have been used to provide power to radiation sensors (2). In these applications, energy harvesters are used to power the read circuitry that measures the threshold voltage shift in the radiation sensor. Because wireless technology is ubiquitous, vibration energy is pervasive in factories and all types of vehicles, and the cost of RADFETs is low, the implementation of real-time wireless radiation sensors is a reality. These wireless networks are expected to be hierarchical. Cost-efficient, high performance networks could include radiation detectors with varying degrees of sensitivity based on biased and unbiased designs.

Citations

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URL:
https://ore.exeter.ac.uk/repository/bitstream/handle/10871/25316/ieee%20sensors%202016_radfet_20160615_camera-ready.pdf?sequence=1

(3) A Commercial off-the-shelf pMOS Transistor as X-ray and Heavy Ion Detector
URL: http://iopscience.iop.org/article/10.1088/1742-6596/630/1/012012/pdf

(4) Response to ionizing radiation of different biased and stacked pMOS structures
URL: http://www.sciencedirect.com/science/article/pii/S0924424716308470

(5) Techniques to increase the sensitivity for dosimetry sensors
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(7) Radiation Detection: Selecting The Right Equipment For The Job
URL: http://www.raesystems.com/customer-care/resource-center/true-stories/radiation-detection-selecting-right-equipment-job

(8) 3N163 Data Sheet, I-V Curves and Electrical Characteristics
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(9) Response to ionizing radiation of different biased and stacked pMOS structures
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LINEAR SYSTEMS

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A Guide to Using FETs for Voltage Controlled Circuits

Introduction

Linear Integrated Systems manufactures a variety of FETs (Field Effect Transistors). In particular they have a variety of matched dual products. There are advantages in having matched devices. For example, if you are building a two-channel stereo audio product, having two or four devices in the same package allows for the two audio channels to be more closely matched.

This paper will explore using FETs in voltage controlled circuits.

Several approaches will be shown:

1. Using FETs as voltage controlled resistors.
2. Using FETs as voltage controlled amplifiers and active mixers.
3. Using FETs as voltage controlled phase shifters for processing music.
4. Using FETs as voltage controlled band pass filters.

We will also explore ways to reduce nonlinearities or distortions and automatically bias the FETs.

FET Voltage Controlled Resistors

Figure 1 shows a typical current-voltage relationship of an N-Channel FET.

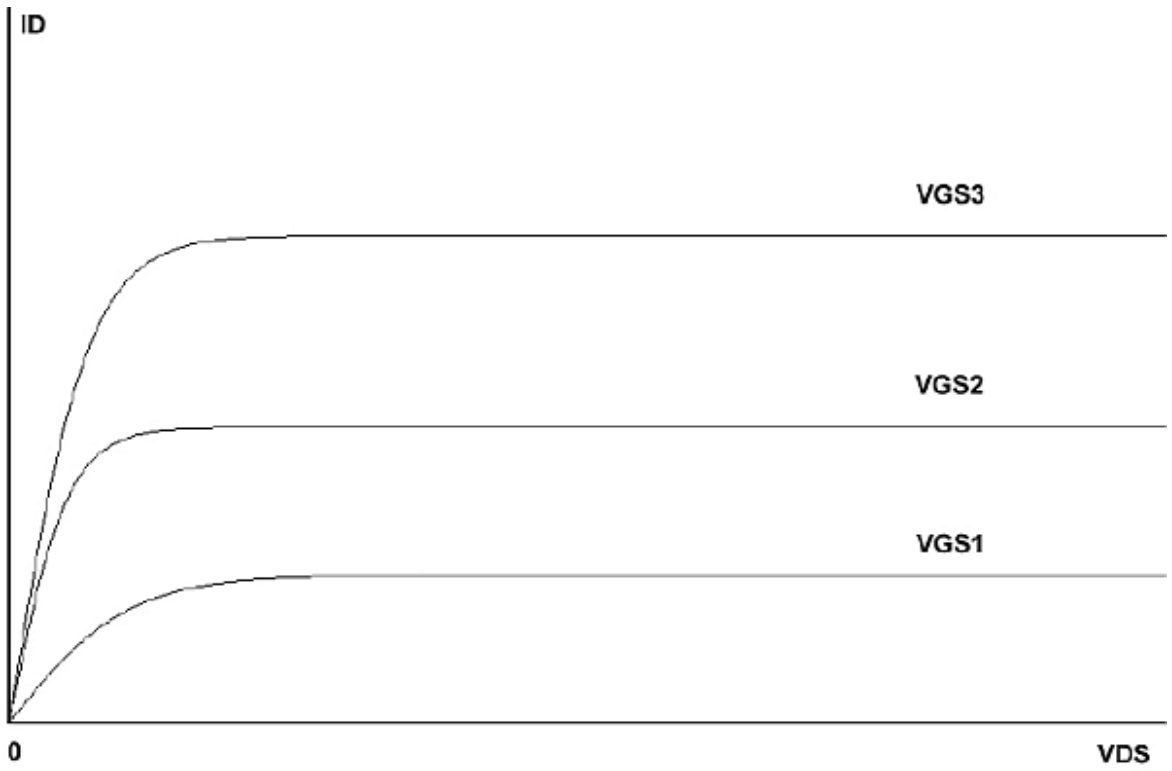

Figure 1: A typical N-Channel FET I/V curve for different gate-to-source voltages, VGS1, VGS2, and VGS3.

A FET has basically two regions:

The **saturation region**, which includes each of the horizontally flat portions where the FET acts as a voltage-controlled current source and the other region that includes the sloped “curved portions” is the **triode or ohmic region** where the FET can operate as a voltage-controlled resistor. If we look carefully we will notice that the triode region in Figure 1 is shown for drain to source voltages (VDS) that are non-negative.

Note: The triode or ohmic region in an FET is sometimes known as the linear region. The FET operating as a voltage-controlled resistor (VCR) works in this region. Preferably, there is no DC voltage across the FET’s drain and source terminals in the VCR mode.

If we extend the VDS voltage range to include slightly negative voltages for a particular gate-to-source voltage, we see that there is still a resistive effect. See Figure 2.

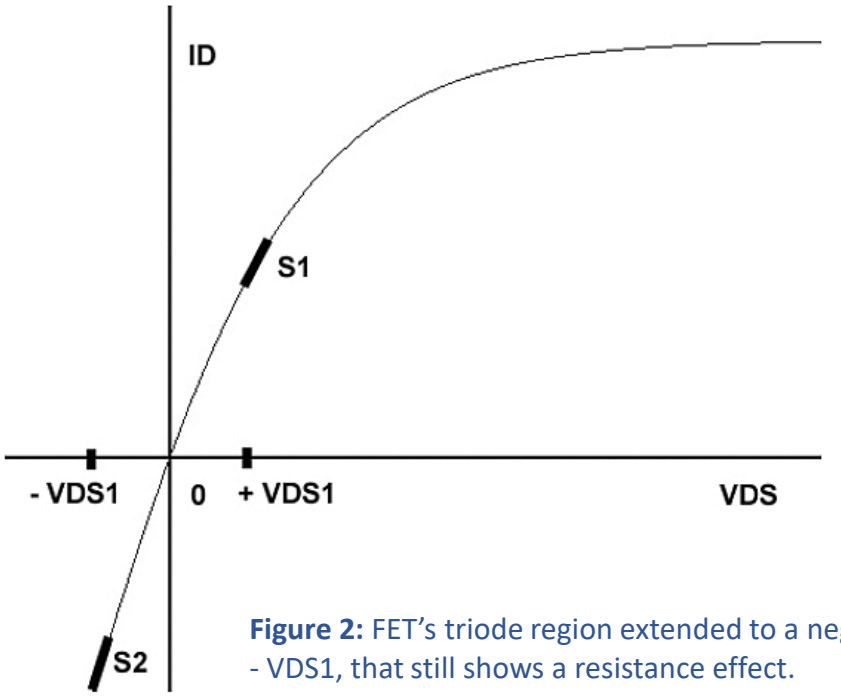

Figure 2: FET’s triode region extended to a negative VDS voltage, - VDS1, that still shows a resistance effect.

The slope is defined as:

Slope = ΔI_D/
ΔVDS = g_{ds} = conductance between the drain and source.

And the resistance across the drain and source is the reciprocal of the conductance,

R_{ds} = 1 / g_{ds} = ΔV_{DS}/ΔID

As we look at the two slopes that denote g_{ds}, S1 and S2, we will see that they are approximately the same. But if we look very closely, they actually are slightly different with the S2's slope being steeper than slope S1. A steeper slope yields a higher conductance, which results in a lower resistance. For example, the resistance around the high sloped region around S2 or – VDS1 is lower than the resistance around S1 or + VDS1. The gradual change in resistance from +VDS1 to – VDS1 results in distortion. Fortunately, the distortion can be kept small.

For instance, with small AC signals (e.g., < 500 mV peak to peak) across the drain and source, the harmonic distortion can be "reasonably" low. As an example, if the AC signal voltage across the drain and source is between -250 mV and +250 mV, then the harmonic distortion will be "small", typically < 3%.

At this point, one may ask if are there specific FETs made just for voltage controlled resistor applications? The answer is yes (e.g., VCR11), but it turns out that virtually any other FET (e.g., JFET and MOSFET) can be used as a voltage controlled resistor.

Basic Voltage Controlled Resistor (VCR) Circuits

One of the simplest uses of a voltage controlled resistor is an electronically controlled attenuator or "volume control". The basic circuit forms a voltage divider as shown in Figures 3, 4, 5, and 6.

In each of these circuits, the drain and source terminals of the FETs (Q1, Q2, Q3, and Q4) provide a voltage controlled resistance. For frequencies greater than 20 Hz, C1's impedance can be considered as an AC short circuit. Let's look at Figure 3 below:

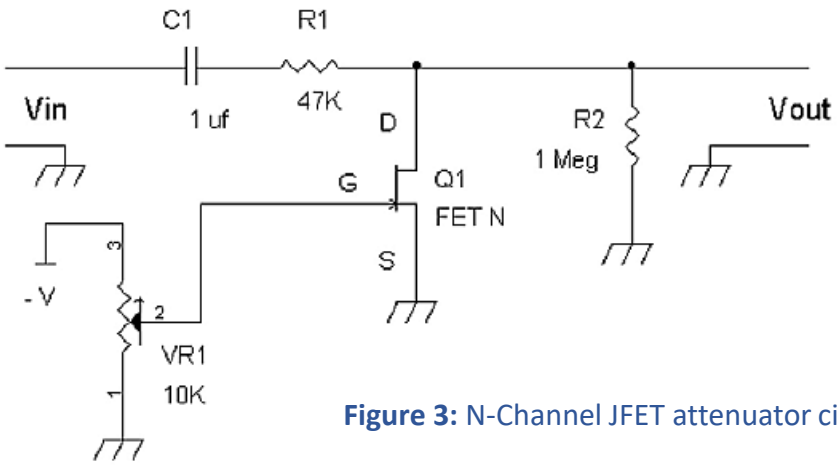

Figure 3: N-Channel JFET attenuator circuit.

In Figure 3, maximum attenuation is achieved by setting Q1's gate voltage to 0 volt or ground. R2 is to establish a DC path to ground for Q1's drain. It can be omitted if C1 is replaced with a wire, and the input signal source has no appreciable DC offset voltage (e.g., < 10 mV DC), and the input signal source has a DC path to ground.

Minimum attenuation (e.g., a "pass through") happens when the negative voltage at Q1's gate causes Q1 to be in cut-off (e.g., the gate voltage → Vp, the pinch off voltage).

The attenuator's transfer function is then:

V_{out}/V_{in} = [R_{ds} || R2] / [R1 + (R_{ds} || R2)]

Note that R_{ds} is the drain to source resistance for a given gate to source voltage.

If R_{ds} << R2, then

$\frac{Vout}{Vin}$ = [R_{ds}] / [R1 + Rds]

For example, if Rds = 10KΩ then

V_{out}/V_{in} = [10KΩ] / [47KΩ + 10KΩ] = 10KΩ/57KΩ = 10/57 = 0.1754

The drain current for a ***"depletion mode"*** N-Channel JFET is given via "Microelectronic Circuits" by Sedra and Smith:

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \quad (1)$$

I_{DSS} = drain current when Vgs = 0. This "maximum" drain current is given in the specification sheet.

Vgs = gate to source voltage that is a non-positive voltage for an N-Channel device.

Vp = pinch off voltage or cut off voltage. This is the voltage applied to the gate and source to provide zero drain current. The pinch off voltage, $Vp \leq 0$ volt for an N-Channel JFET, is given in the specification sheet. Also, then *Vgs* = *Vp*, the drain to source resistance is infinite because there is no current flow into the drain of the FET.

Vds = drain to source voltage. This can be the AC voltage across drain and source such as Vout in Figures 3, 4, 5, and 6.

Equations (1) through (5) are valid only when $Vp \leq Vgs \leq 0$ volt for an N-Channel JFET in the ohmic, triode, or linear region.

The conductance, g_{ds}, is given by taking the derivative of I_d with respect to V_{ds}.

$$g_{ds} = \frac{d}{dVds} I_{DSS}\left[2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \quad (2)$$

$$g_{ds} = I_{DSS}\left[-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right) - 2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right)\right] \quad (3)$$

The resistance, R_{ds} is then the reciprocal of the conductance, g_{ds}

$$R_{ds} = 1/g_{ds} = 1/\left\{I_{DSS}\left[-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right) - 2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right)\right]\right\} \quad (4)$$

Equation 4 shows that R_{ds} is non-linear resistor based on the fixed parameters I_{DSS}, Vp, and a fixed gate to source voltage Vgs with a dependence on the (AC signal's) voltage across the drain and source, Vds.

For a first approximation for small signals across the drain and source, where $Vds \rightarrow 0$, the resistance looks linear because the

$$\text{term: } -2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right) \rightarrow 0$$

This Leads to:

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\} \qquad (5)$$

Equation (5) then is a function of fixed parameters, I_{DSS}, Vp, and the fixed gate to source voltage Vgs. The voltage controlled "linear" resistance is then set by the Vgs voltage.

For example, if Vp = -1.5 volts, Vgs = - 1.0 volt, and I_{DSS} = 0.005 A = 5 mA, then

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\} = 1/\{0.005A\,[\,-2\,(\tfrac{1}{-1.5v})(\,1\,-\tfrac{-1.0v}{-1.5v}\,)]\} = 454\Omega = R_{ds}$$

From equation (5), if we set Vgs = *Vp*, then the drain to source resistance will be infinite (e.g., open circuit):

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\}$$

$$R_{ds} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vp}{Vp}\,)]\} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\,1\,)]\}$$

$$R_{ds} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,0\,)]\} \rightarrow (1/0)\Omega \rightarrow \text{infinite ohms}$$

$$R_{ds} \rightarrow \text{infinite ohms for } Vgs = Vp$$

Now let's look at what happens when we want minimum resistance by setting Vgs = 0 volt for an N-Channel JFET.

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\} = R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{0v}{Vp}\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1-0\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})]\}$$

Or better yet for *Vgs* = 0 volt, this reduces to an easier form:

$R_{ds} = Vp/[-2I_{DSS}]$

For example, if again Vp = -1.5 volts and I_{DSS} = 0.005 A = 5 mA, with Vgs = 0 volt

R_{ds} = -1.5 v/[-2(0.005 A)] = -1.5 v/[-0.01 A] = 1.5 v/0.01 A = 150Ω

R_{ds} = 150Ω

Figure 4 shows a P-Channel FET attenuator circuit. It works similarly to Figure 3, except that the gate's control voltage is positive to cut off Q2 for a minimum attenuation. Again, we get maximum attenuation when the gate voltage is zero or grounded.

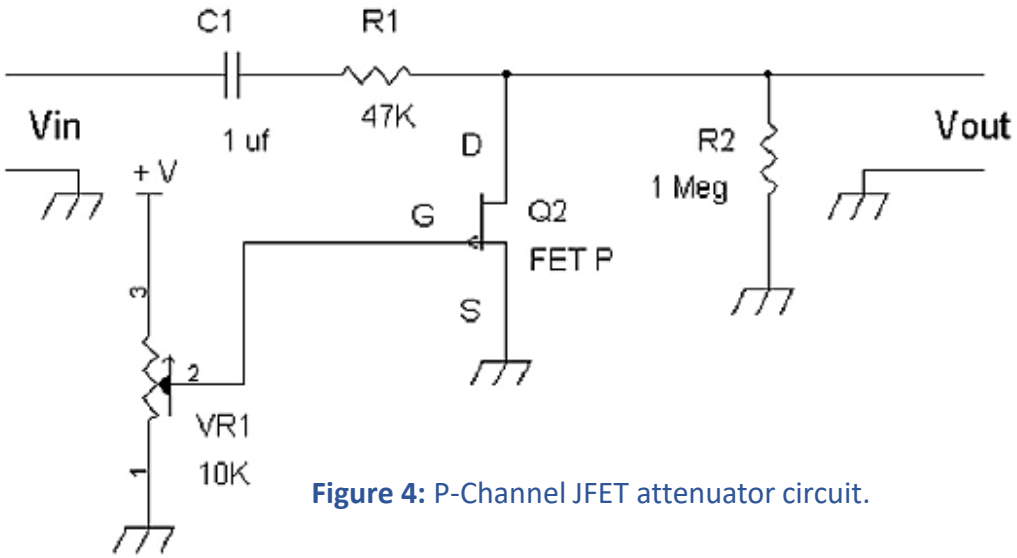

Figure 4: P-Channel JFET attenuator circuit.

In Figure 5 MOSFETs have also been used as voltage controlled resistors. Because most MOSFETs today tend to be "***enhancement mode"***, this means that the required biasing at the gate is a positive voltage to turn on the drain current to lower its R_{ds}. Thus, if the gate voltage is 0 volts, the MOSFET is turned off.

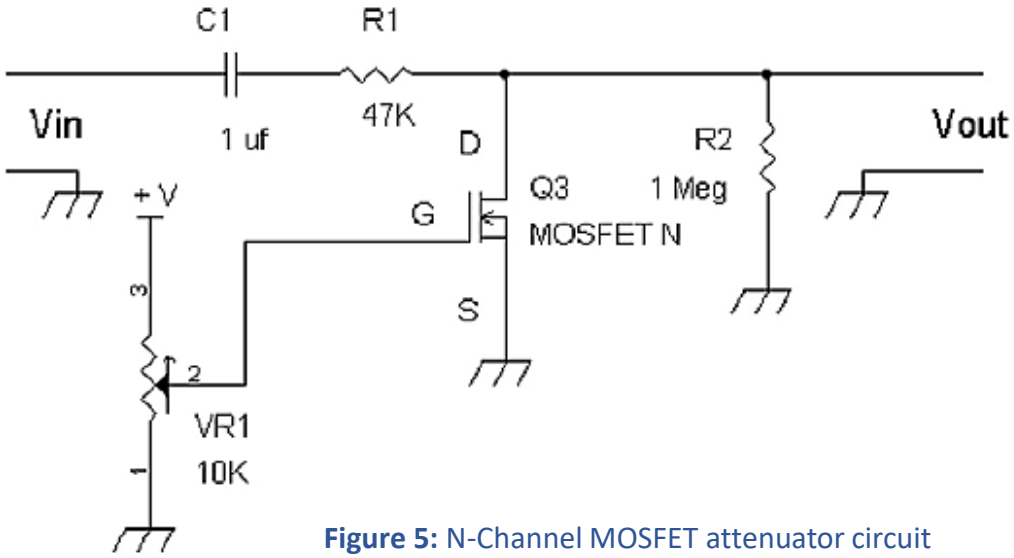

Figure 5: N-Channel MOSFET attenuator circuit

With an N-Channel enhancement mode device, Q3, at zero volts the attenuator passes the input signal to Vout with minimum attenuation. If VR1 is set to a positive voltage greater than the ***threshold voltage***, V_{th}, Q3's drain to source resistance will start to drop. Note that the threshold voltage, $V_{th} > 0$ volt for an N-Channel MOSFET.

From "Analysis and Design of Analog Integrated Circuits" by Gray and Meyer, the drain current of an N-Channel MOSFET is characterized by equation (6):

$$I_d = \frac{k'}{2}\frac{W}{L}\left[2(V_{gs} - V_{th})V_{ds} - (V_{ds})(V_{ds})\right] \qquad (6)$$

Where:

$k' = \mu_n C_{ox}$

$C_{ox} = \varepsilon_{ox} / t_{ox}$

W = width of the MOS device

L = channel length of the MOS device

It should be noted that most discrete MOSFET spec sheets will not list $k' = \mu_n C_{ox}$, $C_{ox} = \varepsilon_{ox} / t_{ox}$ W and L. Instead, they will give a plot of typical IV curves and threshold voltage ranges.

If we look at equation (1) for an N-Channel JFET, we will see that equation (6) is very similar. Note that they both include a " - (Vds)(Vds)" term, which results in a nonlinear resistance.

To reiterate, the N-Channel JFET's equation is:

$$I_d = I_{DSS}\left[2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \qquad (1)$$

Figure 6 shows a P-Channel MOSFET voltage controlled resistor circuit.

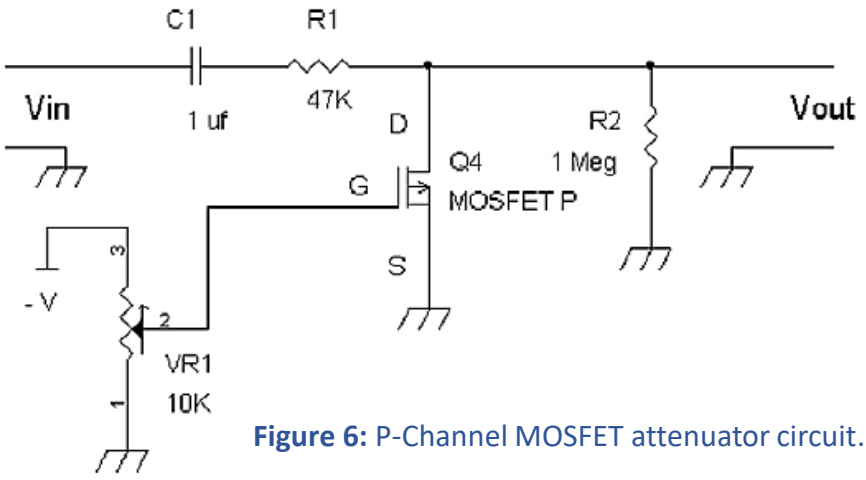

Figure 6: P-Channel MOSFET attenuator circuit.

With a P-Channel enhancement mode device, Q4, at zero volts the attenuator passes the input signal to Vout with minimum attenuation. If VR1 is set to a more negative voltage than the threshold voltage, V_{th}, Q4's drain to source resistance will start to drop. Note the threshold voltage for the P-Channel MOSFET is a negative voltage (e.g., $V_{th} < 0$ volt).

Generally, the attenuator circuits shown in Figures 5 and 6 will allow for reasonably small harmonic distortion for small signals, < 500 mV peak to peak at Vout. If there is distortion, second order harmonic distortion will be dominant.

A Balanced or Push Pull Voltage Controlled Resistor (VCR) Circuit

We can further linearize or reduce substantially second order distortion by making a push-pull circuit as shown in Figure 7. In particular, having a dual matched FET (e.g., VCR11N, LSK489, LSK389, etc.) allows for even order distortion cancellation.

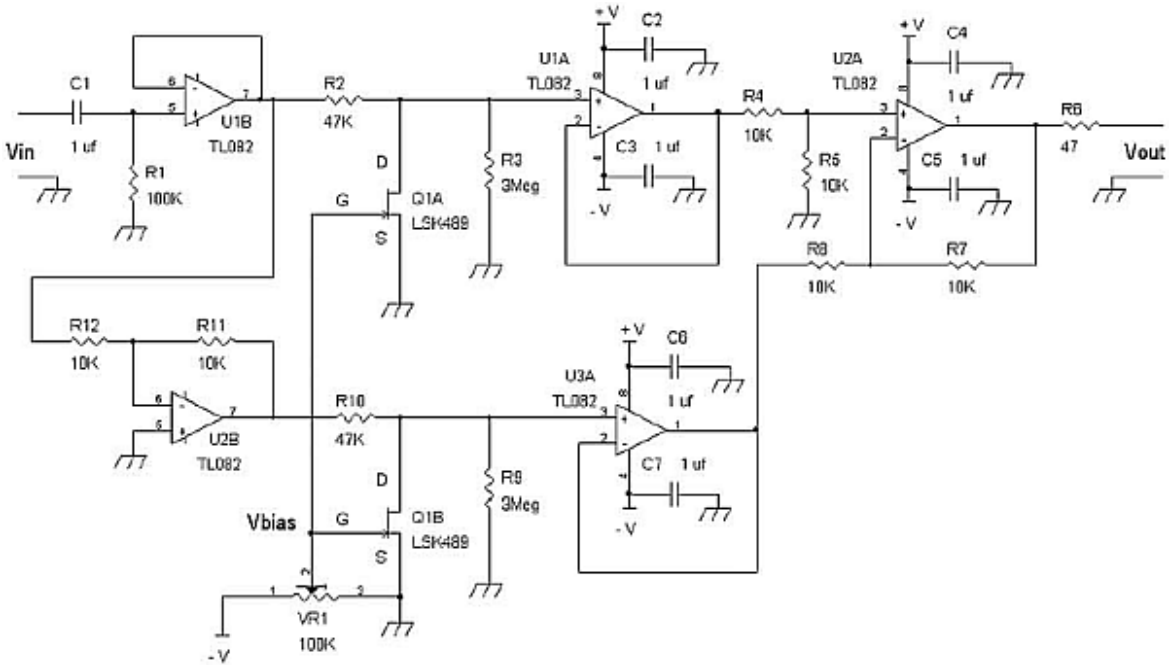

Figure 7: N-Channel balanced configuration example for lowering distortion using a dual matched FET, LSK489, Q1A and Q1B.

A push pull or balanced VCR attenuator circuit cancels or reduces the second order distortion. In Figure 7, U1B buffers the input signal Vin, and drives the first voltage controlled attenuator circuit with Q1A (one half of the dual FET package). Vbias, which is shown as a variable DC negative voltage varies Q1A's drain to source resistance to provide a voltage controlled voltage divider circuit via series resistor R2. Voltage follower amplifier U1A buffers Q1A's drain terminal's voltage controlled attenuated signal. Note that FET input op amps such as TL082, TL062, LF353, AD712, etc. are generally used with high impedance input resistors such as R3 and R9.

Op amp circuit R12, R11, and U2B form an inverting amplifier that sends an out of phase signal to the second voltage controlled attenuator circuit via R10. Q1B's gate has the same Vbias signal that allows for matched attenuation characteristics across the drains and sources of Q1A and Q1B. Voltage follower U3A buffers the voltage controlled attenuated out of phase signal via Q1B's drain. A differential amplifier formed by U2A, R4, R5, R7, and R8 subtracts the outputs from U1A and U3A to cancel out second order distortion via Vout. See below for more details.

At this point, there are second order distortions at both Q1A's and Q1B's drain that are in phase. The reason is that second order distortion implies an x^2 function.

But observe that squaring a negative signal and squaring a positive signal gives the same result. That is

$(- x)^2 = (+ x)^2$

The output signals can be characterized as the following:

a_1 = linear **voltage divider** coefficient
a_2 = second order distortion coefficient

For the non-inverting signal, U1A pin 1 = a_1 Vin + $a_2 (Vin)^2$

For the inverting signal, U3A pin 1 = a_1 (- Vin) + a_2 $(- Vin)^2$

Note that: $(Vin)^2 = (- Vin)^2$

So, we have for the inverting signal,

U3A pin 1 = - a_1 Vin + $a_2 (Vin)^2$

Differential amplifier U2A performs a subtraction of the non-inverting and inverting signals from U1A pin 1 and U3A pin 1, we have:

a_1 Vin + $a_2 (Vin)^2$ - [- a_1 Vin + $a_2 (Vin)^2$] = a_1 Vin + $a_2 (Vin)^2$ + a_1 Vin - $a_2 (Vin)^2$ =

a_1 Vin + a_1 Vin + $a_2 (Vin)^2$ - $a_2 (Vin)^2$ = 2a_1 Vin + 0 $(Vin)^2$ = 2a_1 Vin

Note that $a_2 (Vin)^2$ - $a_2 (Vin)^2$ = 0

Thus, the output of differential amplifier circuit U2A pin 1 = 2a_1 Vin, and note the absence of the second order distortion term. What this means is that we get a voltage controlled attenuated signal amplified by 2, and without the second order distortion.

Note that Figure 7 shows an N-Channel JFET example, but the basic principle of push pull or balanced operation can be applied to P-Channel JFET, N-Channel MOSFET, and P-Channel MOSFET voltage controlled attenuator circuits shown in Figures 4, 5, and 6 respectively.

Alternatively, we can apply feedback to the basic voltage controlled resistor circuit to substantially remove second order distortion. When we apply this feedback, ***the output signal distorts symmetrically***. This implies mostly odd order distortion products.

Figures 8 through 15 show examples, but we can examine Figure 8 first in Part 2 of this series.

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