

# LINEAR SYSTEMS

Over Three Decades of Quality Through Innovation

## LSK489

### LOW NOISE LOW CAPACITANCE MONOLITHIC DUAL N-CANNEL JFET AMPLIFIER

#### FEATURES

ULTRA LOW NOISE	$e_n = 1.8nV/\sqrt{Hz}$
LOW INPUT CAPACITANCE	$C_{iss} = 4pF$

#### Features

- Reduced Noise due to process improvement
- Monolithic Design
- High slew rate
- Low offset/drift voltage
- Low gate leakage  $I_{gss}$  &  $I_g$
- High CMRR 102 dB

#### Benefits

- Tight differential voltage match vs. current
- Improved op amp speed settling time accuracy
- Minimum Input Error trimming error voltage
- Lower intermodulation distortion

#### Applications

- Wide band differential Amps
- High speed temperature compensated single ended input amplifier amps
- High speed comparators
- Impedance Converters

#### Description

The LSK 489 series of high performance monolithic dual JFETs features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications. The SST series SO-8 package provided ease of manufacturing and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape and reel options for compatibility with automatic assembly methods. (See packaging data)

#### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

@ 25 °C (unless otherwise stated)

#### Maximum Temperatures

Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C

#### Maximum Power Dissipation, TA = 25°C

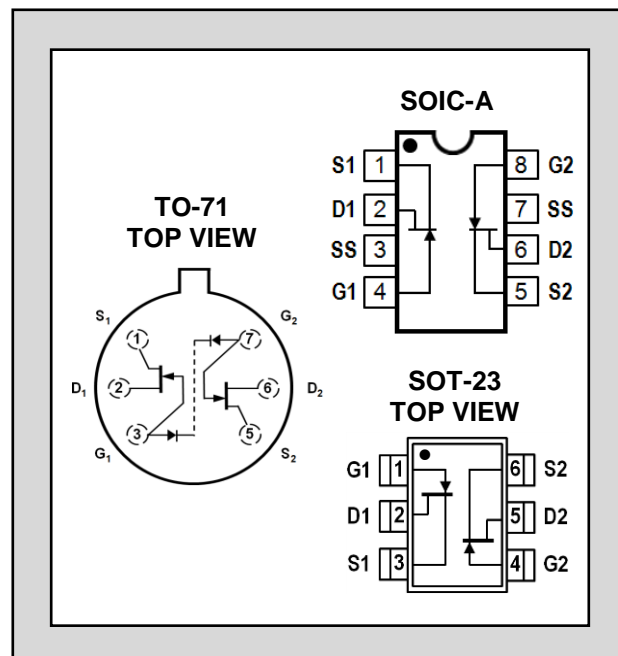
Continuous Power Dissipation, per side <sup>4</sup>	300mW
Power Dissipation, total <sup>5</sup>	500mW

#### Maximum Currents

Gate Forward Current	$I_{G(F)} = 10mA$
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#### Maximum Voltages

Gate to Source	$V_{GSO} = 60V$
Gate to Drain	$V_{GDO} = 60V$



\* For equivalent single version, see LSK189

**MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)**

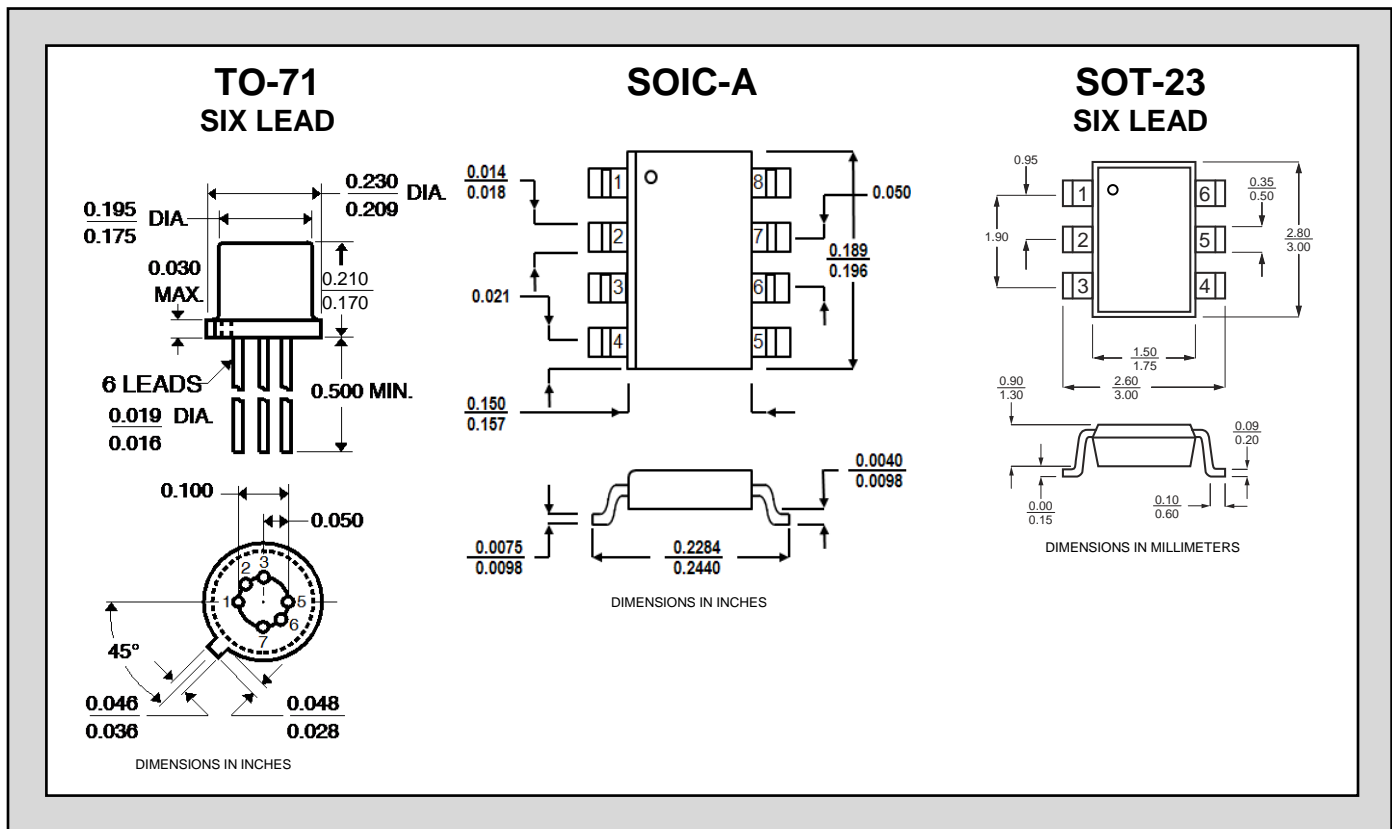
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{GS1} - V_{GS2} $	Differential Gate to Source Cutoff Voltage			20	mV	$V_{DS} = 10V, I_D = 1mA$
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9		1.0		$V_{DS} = 10V, V_{GS} = 0V$
CMRR	<b>COMMON MODE REJECTION RATIO</b> $-20 \log  \Delta V_{GS1-2}/\Delta V_{DS} $	95	102		dB	$V_{DS} = 10V \text{ to } 20V, I_D = 200\mu A$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$e_n$	Noise Voltage		2.0		nV/ $\sqrt{Hz}$	$V_{DS} = 15V, I_D = 2.0mA, f = 1kHz, NBW = 1Hz$
$e_n$	Noise Voltage		3.5		nV/ $\sqrt{Hz}$	$V_{DS} = 15V, I_D = 2.0mA, f = 10Hz, NBW = 1Hz$
$C_{ISS}$	Common Source Input Capacitance		4	8	pF	$V_{DS} = 15V, I_D = 500\mu A, f = 1MHz$
$C_{RSS}$	Common Source Reverse Transfer Capacitance			3	pF	

**ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)**

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$BV_{GSS}$	Gate to Source Breakdown Voltage	-60			V	$V_{DS} = 0, I_D = -1nA$
$V_{(BR)G1-G2}$	Gate to Gate Breakdown Voltage	$\pm 30$	$\pm 45$		V	$I_G = \pm 1\mu A, I_D = I_S = 0A$ (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.5		-3.5	V	$V_{DS} = 15V, I_D = 1nA$
$V_{GS}$	Gate to Source Operating Voltage	-0.5		-3.5	V	$V_{DS} = 15V, I_D = 500\mu A$
$I_{DSS}^2$	Drain to Source Saturation Current	2.5	5	15	mA	$V_{DG} = 15V, V_{GS} = 0$
$I_G$	Gate Operating Current		-2	-25	pA	$V_{DG} = 15V, I_D = 200\mu A$ $T_A = 125^\circ C$
			-0.8	-10	nA	
$I_{GSS}$	Gate to Source Leakage Current			-100	pA	$V_{DG} = -15V, V_{DS} = 0$
$G_{fs}$	Full Conductance Transconductance	1500			$\mu S$	$V_{DG} = 15V, V_{GS} = 0, f = 1kHz$
$G_{fs}$	Transconductance	1000	1500		$\mu S$	$V_{DG} = 15V, I_D = 500\mu A$
$G_{OS}$	Full Output Conductance			40	$\mu S$	$V_{DG} = 15V, V_{GS} = 0$
$G_{OS}$	Output Conductance		1.8	2.7	$\mu S$	$V_{DG} = 15V, I_D = 200\mu A$
NF	Noise Figure			0.5	dB	$V_{DS} = 15V, V_{GS} = 0, R_G = 10M\Omega, f = 100Hz, NBW = 6Hz$

PACKAGE DIMENSIONS

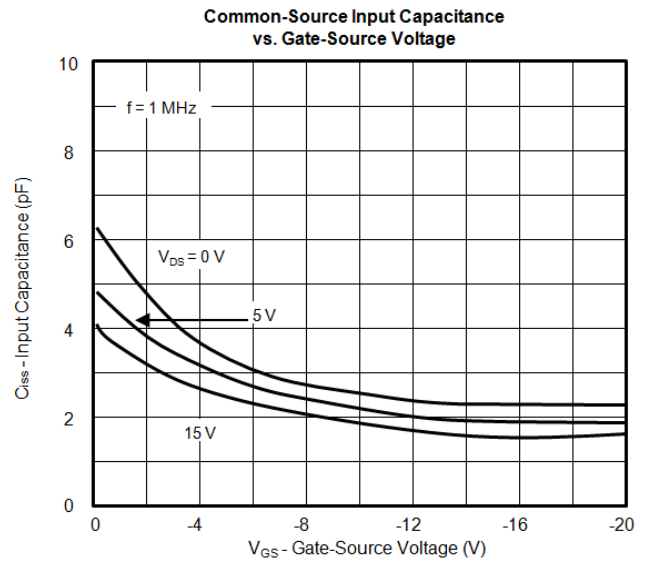
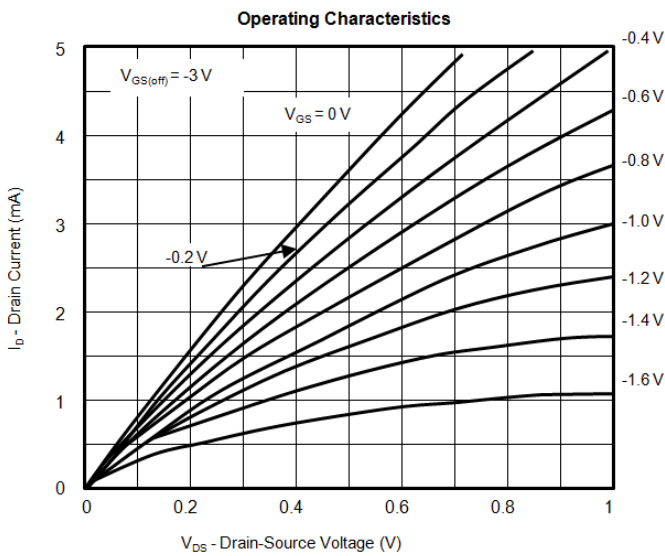
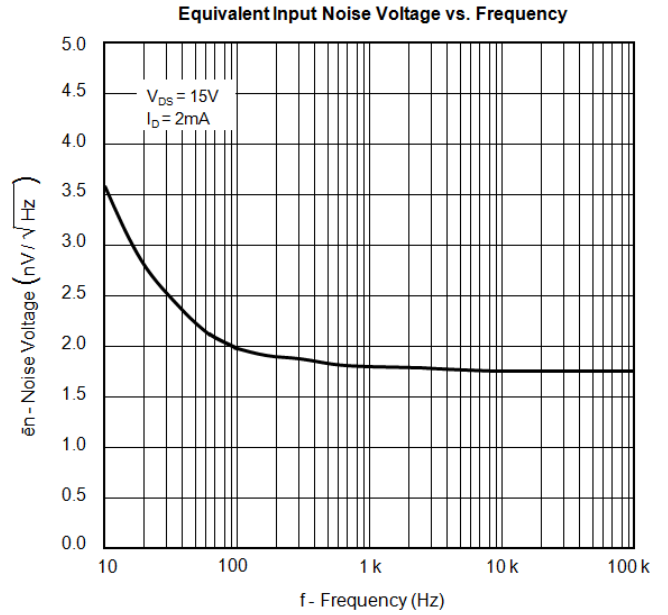
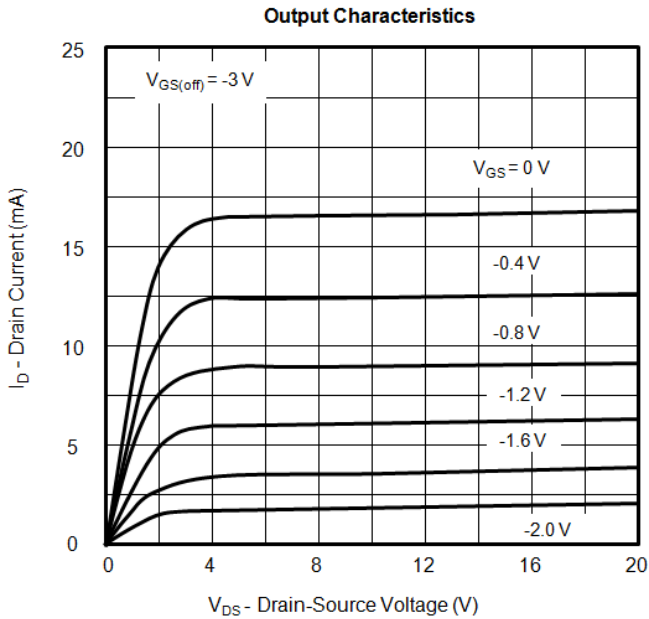
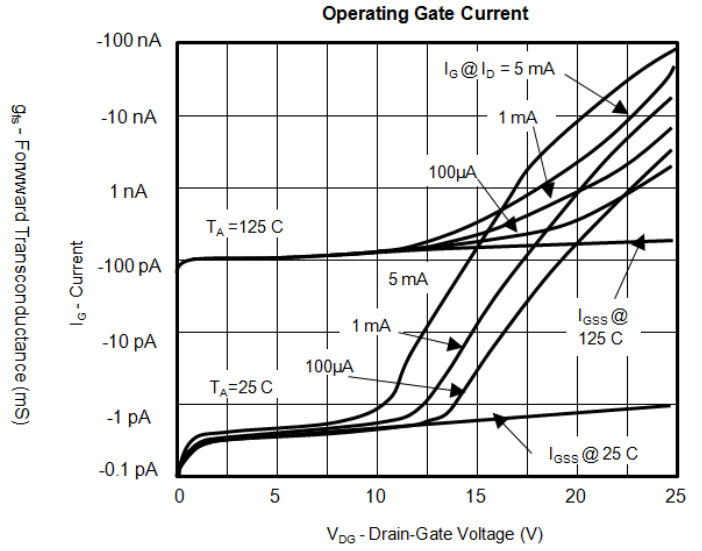
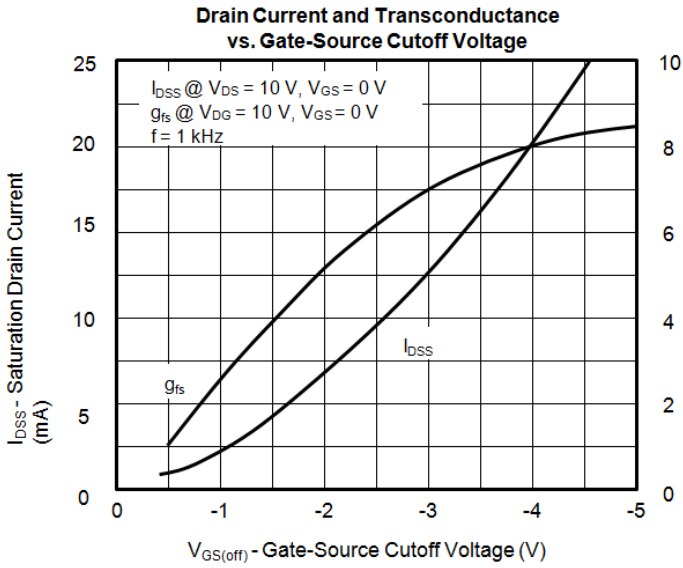


**NOTES**

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width  $\leq 2_{ms}$ .
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

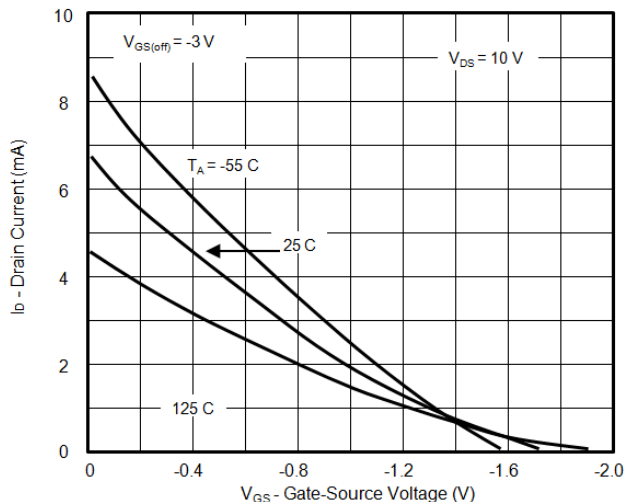
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# Typical Characteristics

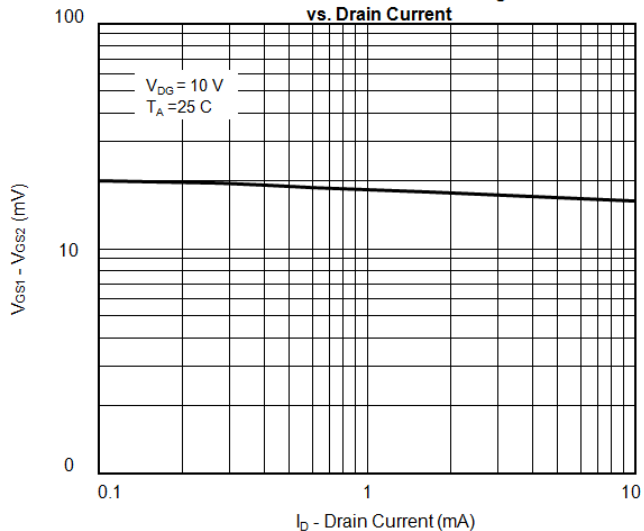


# Typical Characteristics (Cont'd)

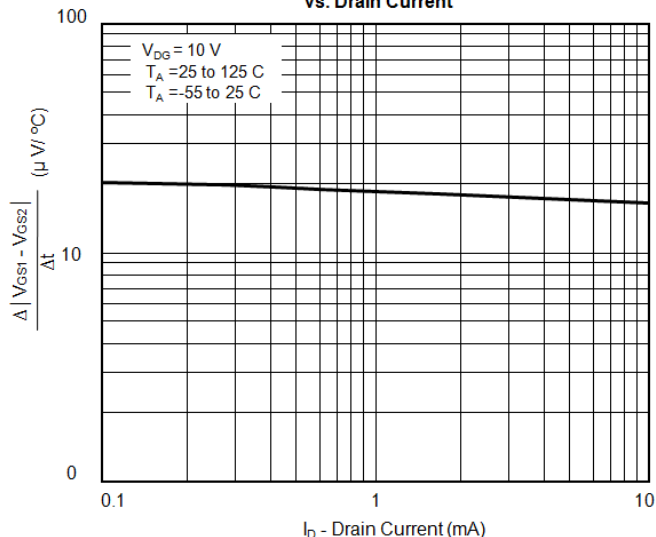
**Transfer Characteristics**



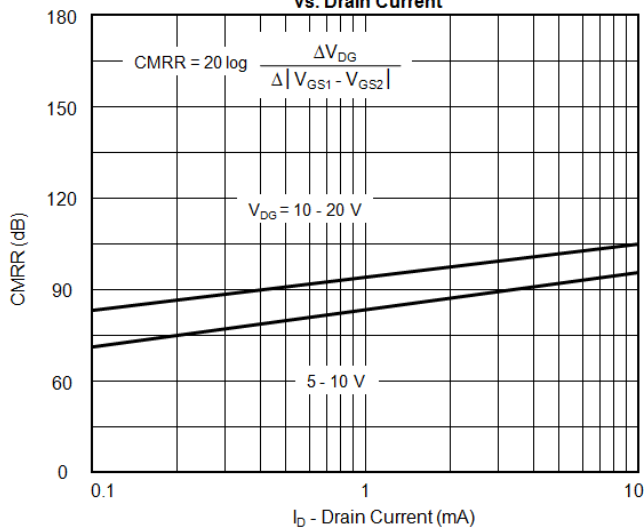
**Gate-Source Differential Voltage vs. Drain Current**



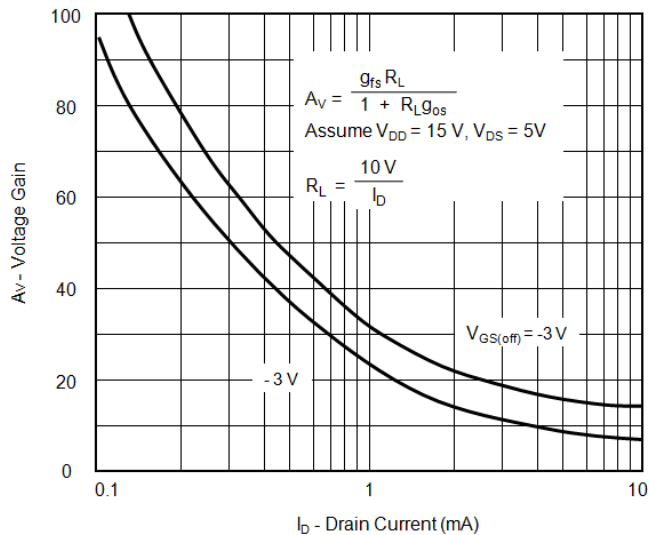
**Voltage Differential with Temperature vs. Drain Current**



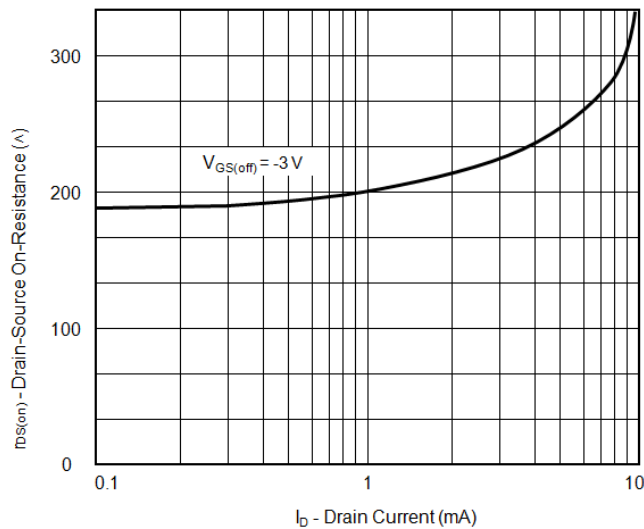
**Common Mode Rejection Ratio vs. Drain Current**



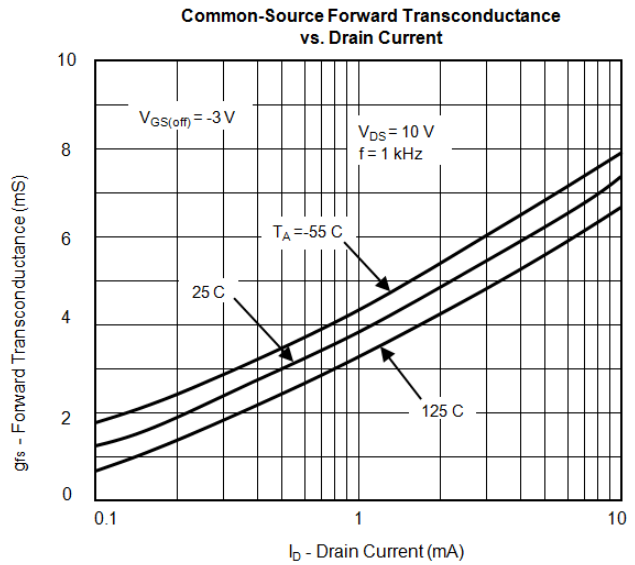
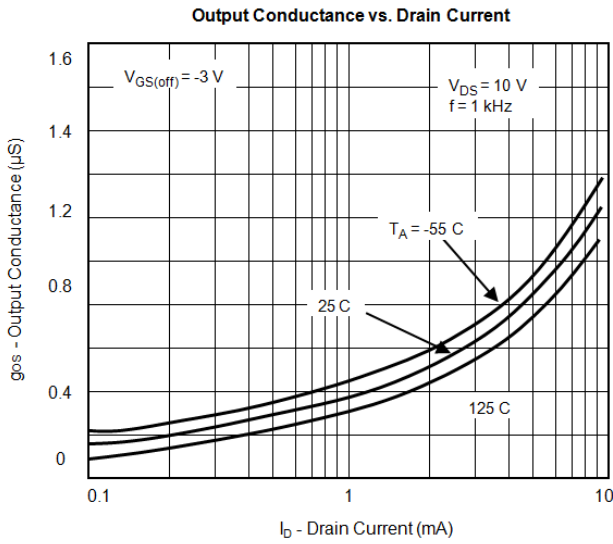
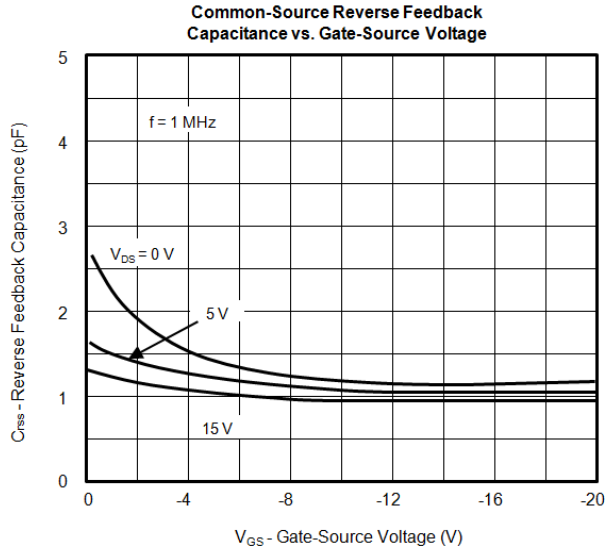
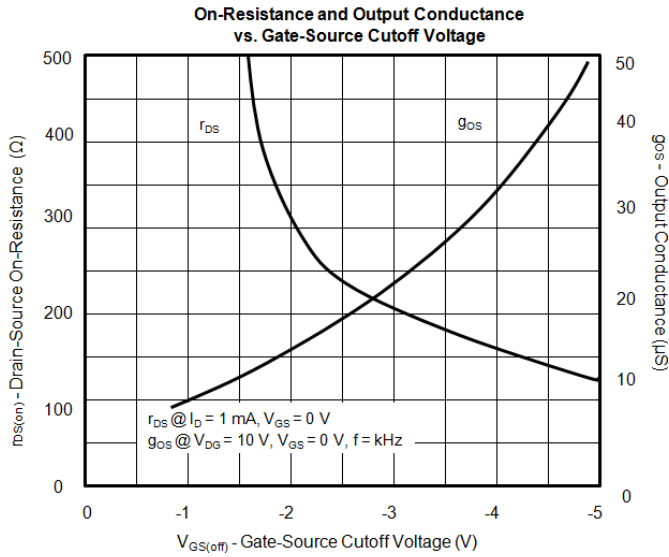
**Circuit Voltage Gain vs. Drain Current**



**On-Resistance vs. Drain Current**



# Typical Characteristics (Cont'd)



Linear Integrated Systems (LIS), established in 1987, is third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company Founder John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.